32-bit RISC Microcontroller

# TXZ+ Family
# TMPM3H Group(1)

## Reference Manual
## Input/Output Ports
## (PORT-M3H(1))

**Revision 1.2**

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Toshiba Electronic Devices & Storage Corporation

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## Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [ ] defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

## Terms and Abbreviations

Some of abbreviations used in this document are as follows:

| | |
|---|---|
| JTAG | Joint Test Action Group |
| SW | Serial Wire |

# 1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

| Function classification | Function | Description |
|---|---|---|
| Port | - | Programmable pull-up /Programmable pull-down /Open-drain output are possible. |
| Peripheral function pins | Clock Output | SCOUT pin |
| | External Interrupt | Interrupt pin has a noise filter(Filter width 30ns Typ.). |
| | 32-bit Timer Event Counter | External trigger Input pin. Timer output pin. |
| | Real Time Clock | 1Hz clock output pin |
| | Serial Peripheral Interface | Chip select input for slave operation 1 pin, Chip select 2 pins, Serial data of transmission pin, Serial data reception pin, Serial clock input/output pin |
| | Asynchronous Serial Communication Circuit | Data input pin, Data output 2 pins, Request to send signal pin, Receivable input pin. |
| | $I^2C$ Interface | SCL signal pin, SDA signal pin |
| | $EI^2C$ Interface | SCL signal pin, SDA signal pin |
| | Remote Control Signal preprocessor | Remote control data entry pin |
| | Analog to Digital Convertor | Analog input pin |
| | Digital to Analog Convertor | DAC output pin |
| | Advanced Programmable Motor Control Circuit | X/Y/Z phase output pins, U/V/W phase output pins, EMG detection input pin, OVV detection input pin |
| | Advanced Encoder Input Circuit | Encoder input pins |
| | Trigger Input | External trigger input pins |
| | Digital LCD | Segment pins, Common pins |
| Debug pins | JTAG | JTAG Test Mode Selection pin, JTAG Serial clock input pin, JTAG Serial data output pin, JTAG Serial data input pin, JTAG Test reset input pin |
| | SW | Serial wire data input/output pin, Serial wire clock input pin, Serial wire viewer output pin |
| | Trace | Trace clock output pin, Trace data output 4pins |
| Control pins | High speed clock | High speed resonator connection pin, External clock input |
| | Low speed clock | Low speed resonator connection pin |
| | BOOT mode control | BOOT mode control pin |

# 2. Function

## 2.1. Clock Supply

When PORT is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB])***, fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to Reference manual "Clock Control and Operation Mode".

# 3. Signal Connection List

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

**Table 3.1 Signal Connection List: UART ch0,1**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| Asynchronous Serial Communication Circuit | UT0TXDA | PA1 | 27 | 23 | 26 | 17 | 19 | 16 | 14 |
| | | PA2 | 26 | 22 | 25 | 16 | 18 | 15 | 13 |
| | | PM1 | 35 | 31 | 34 | 24 | 26 | 19 | - |
| | | PM2 | 34 | 30 | 33 | 23 | 25 | 18 | - |
| | UT0TXDB | PA0 | 28 | 24 | 27 | 18 | 20 | 17 | 15 |
| | | PM0 | 36 | 32 | 35 | 25 | 27 | 20 | 16 |
| | UT0RXD | PA2 | 26 | 22 | 25 | 16 | 18 | 15 | 13 |
| | | PA1 | 27 | 23 | 26 | 17 | 19 | 16 | 14 |
| | | PM2 | 34 | 30 | 33 | 23 | 25 | 18 | - |
| | | PM1 | 35 | 31 | 34 | 24 | 26 | 19 | - |
| | UT0CTS_N | PM3 | 33 | 29 | 32 | 22 | 24 | - | - |
| | | PM4 | 32 | 28 | 31 | 21 | 23 | - | - |
| | UT0RTS_N | PM4 | 32 | 28 | 31 | 21 | 23 | - | - |
| | | PM3 | 33 | 29 | 32 | 22 | 24 | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Asynchronous Serial Communication Circuit | UT1TXDA | PJ1 | 105 | 92 | 95 | 72 | 74 | 57 | 45 |
| | | PJ2 | 106 | 93 | 96 | 73 | 75 | 58 | 46 |
| | | PK1 | 111 | 98 | 101 | 78 | 80 | 63 | 51 |
| | | PK2 | 112 | 99 | 102 | 79 | 81 | 64 | 52 |
| | UT1TXDB | PJ0 | 104 | 91 | 94 | 71 | 73 | 56 | 44 |
| | | PK0 | 110 | 97 | 100 | 77 | 79 | 62 | 50 |
| | UT1RXD | PJ2 | 106 | 93 | 96 | 73 | 75 | 58 | 46 |
| | | PJ1 | 105 | 92 | 95 | 72 | 74 | 57 | 45 |
| | | PK2 | 112 | 99 | 102 | 79 | 81 | 64 | 52 |
| | | PK1 | 111 | 98 | 101 | 78 | 80 | 63 | 51 |
| | UT1CTS_N | PJ3 | 107 | 94 | 97 | 74 | 76 | 59 | 47 |
| | | PJ4 | 108 | 95 | 98 | 75 | 77 | 60 | 48 |
| | | PK3 | 113 | 100 | 103 | 80 | 82 | 65 | 53 |
| | | PK4 | 114 | 101 | 104 | 81 | 83 | 66 | 54 |
| | UT1RTS_N | PJ4 | 108 | 95 | 98 | 75 | 77 | 60 | 48 |
| | | PJ3 | 107 | 94 | 97 | 74 | 76 | 59 | 47 |
| | | PK4 | 114 | 101 | 104 | 81 | 83 | 66 | 54 |
| | | PK3 | 113 | 100 | 103 | 80 | 82 | 65 | 53 |

**Table 3.2 Signal Connection List: UART ch2,3**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| Asynchronous Serial Communication Circuit | UT2TXDA | PB2 | 39 | 35 | 38 | 28 | 30 | 23 | 19 |
| | | PB3 | 40 | 36 | 39 | 29 | 31 | 24 | 20 |
| | | PL0 | 47 | 41 | 44 | 34 | 36 | 26 | 21 |
| | | PL1 | 48 | 42 | 45 | 35 | 37 | 27 | 22 |
| | UT2RXD | PB3 | 40 | 36 | 39 | 29 | 31 | 24 | 20 |
| | | PB2 | 39 | 35 | 38 | 28 | 30 | 23 | 19 |
| | | PL1 | 48 | 42 | 45 | 35 | 37 | 27 | 22 |
| | | PL0 | 47 | 41 | 44 | 34 | 36 | 26 | 21 |
| | UT2CTS_N | PB4 | 41 | 37 | 40 | 30 | 32 | 25 | - |
| | | PB5 | 42 | 38 | 41 | 31 | 33 | - | - |
| | | PL2 | 49 | 43 | 46 | 36 | 38 | 28 | 23 |
| | | PL3 | 50 | 44 | 47 | 37 | 39 | 29 | 24 |
| | UT2RTS_N | PB5 | 42 | 38 | 41 | 31 | 33 | - | - |
| | | PB4 | 41 | 37 | 40 | 30 | 32 | 25 | - |
| | | PL3 | 50 | 44 | 47 | 37 | 39 | 29 | 24 |
| | | PL2 | 49 | 43 | 46 | 36 | 38 | 28 | 23 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Asynchronous Serial Communication Circuit | UT3TXDA | PA7 | 21 | 17 | 20 | 11 | 13 | 10 | 10 |
| | | PA6 | 22 | 18 | 21 | 12 | 14 | 11 | 11 |
| | | PG3 | 16 | 12 | 15 | - | - | - | - |
| | | PG2 | 15 | 11 | 14 | - | - | - | - |
| | UT3TXDB | PG4 | 17 | 13 | 16 | - | - | - | - |
| | UT3RXD | PA6 | 22 | 18 | 21 | 12 | 14 | 11 | 11 |
| | | PA7 | 21 | 17 | 20 | 11 | 13 | 10 | 10 |
| | | PG2 | 15 | 11 | 14 | - | - | - | - |
| | | PG3 | 16 | 12 | 15 | - | - | - | - |

**Table 3.3 Signal Connection List: UART ch4,5,6,7**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| Asynchronous Serial Communication Circuit | UT4TXDA | PC3 | 86 | 73 | 76 | 57 | 59 | 47 | 38 |
| | | PC4 | 87 | 74 | 77 | 58 | 60 | 48 | 39 |
| | | PV6 | 81 | - | - | - | - | - | - |
| | | PV7 | 82 | - | - | - | - | - | - |
| | UT4TXDB | PC2 | 85 | 72 | 75 | 56 | 58 | 46 | - |
| | | PV5 | 80 | - | - | - | - | - | - |
| | UT4RXD | PC4 | 87 | 74 | 77 | 58 | 60 | 48 | 39 |
| | | PC3 | 86 | 73 | 76 | 57 | 59 | 47 | 38 |
| | | PV7 | 82 | - | - | - | - | - | - |
| | | PV6 | 81 | - | - | - | - | - | - |
| | UT4CTS_N | PC5 | 88 | 75 | 78 | 59 | 61 | 49 | - |
| | | PC6 | 89 | 76 | 79 | 60 | 62 | 50 | - |
| | UT4RTS_N | PC6 | 89 | 76 | 79 | 60 | 62 | 50 | - |
| | | PC5 | 88 | 75 | 78 | 59 | 61 | 49 | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Asynchronous Serial Communication Circuit | UT5TXDA | PN3 | 100 | 87 | 90 | 67 | 69 | 52 | 41 |
| | | PN2 | 101 | 88 | 91 | 68 | 70 | 53 | 42 |
| | UT5TXDB | PN4 | 99 | 86 | 89 | 66 | 68 | 51 | 40 |
| | UT5RXD | PN2 | 101 | 88 | 91 | 68 | 70 | 53 | 42 |
| | | PN3 | 100 | 87 | 90 | 67 | 69 | 52 | 41 |
| | UT5CTS_N | PN1 | 102 | 89 | 92 | 69 | 71 | 54 | 43 |
| | | PN0 | 103 | 90 | 93 | 70 | 72 | 55 | - |
| | UT5RTS_N | PN0 | 103 | 90 | 93 | 70 | 72 | 55 | - |
| | | PN1 | 102 | 89 | 92 | 69 | 71 | 54 | 43 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Asynchronous Serial Communication Circuit | UT6TXDA | PK6 | 116 | 103 | 106 | 83 | 85 | 68 | 56 |
| | | PK5 | 115 | 102 | 105 | 82 | 84 | 67 | 55 |
| | UT6TXDB | PK7 | 117 | 104 | 107 | 84 | 86 | 69 | - |
| | UT6RXD | PK5 | 115 | 102 | 105 | 82 | 84 | 67 | 55 |
| | | PK6 | 116 | 103 | 106 | 83 | 85 | 68 | 56 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Asynchronous Serial Communication Circuit | UT7TXDA | PR1 | 91 | 78 | 81 | 62 | 64 | - | - |
| | | PR0 | 90 | 77 | 80 | 61 | 63 | - | - |
| | UT7TXDB | PR2 | 92 | 79 | 82 | 63 | 65 | - | - |
| | UT7RXD | PR0 | 90 | 77 | 80 | 61 | 63 | - | - |
| | | PR1 | 91 | 78 | 81 | 62 | 64 | - | - |

**Table 3.4 Signal Connection List: I2C/EI2C/TSPI ch0,1**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| I²C Interface | I2C0SCL | PC0 | 83 | 70 | 73 | 54 | 56 | 44 | 36 |
| | I2C0SDA | PC1 | 84 | 71 | 74 | 55 | 57 | 45 | 37 |
| | I2C1SCL | PA4 | 24 | 20 | 23 | 14 | 16 | 13 | - |
| | I2C1SDA | PA5 | 23 | 19 | 22 | 13 | 15 | 12 | - |
| | I2C2SCL | PL0 | 47 | 41 | 44 | 34 | 36 | 26 | 21 |
| | I2C2SDA | PL1 | 48 | 42 | 45 | 35 | 37 | 27 | 22 |
| | I2C3SCL | PT1 | 61 | 51 | 54 | - | - | - | - |
| | I2C3SDA | PT0 | 62 | 52 | 55 | - | - | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| I²C Interface Version A | EI2C0SCL | PC0 | 83 | 70 | 73 | 54 | 56 | 44 | 36 |
| | EI2C0SDA | PC1 | 84 | 71 | 74 | 55 | 57 | 45 | 37 |
| | EI2C1SCL | PA4 | 24 | 20 | 23 | 14 | 16 | 13 | - |
| | EI2C1SDA | PA5 | 23 | 19 | 22 | 13 | 15 | 12 | - |
| | EI2C2SCL | PL0 | 47 | 41 | 44 | 34 | 36 | 26 | 21 |
| | EI2C2SDA | PL1 | 48 | 42 | 45 | 35 | 37 | 27 | 22 |
| | EI2C3SCL | PT1 | 61 | 51 | 54 | - | - | - | - |
| | EI2C3SDA | PT0 | 62 | 52 | 55 | - | - | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Serial Peripheral Interface | TSPI0SCK | PM0 | 36 | 32 | 35 | 25 | 27 | 20 | 16 |
| | | PA0 | 28 | 24 | 27 | 18 | 20 | 17 | 15 |
| | TSPI0TXD | PM1 | 35 | 31 | 34 | 24 | 26 | 19 | - |
| | | PA1 | 27 | 23 | 26 | 17 | 19 | 16 | 14 |
| | TSPI0RXD | PM2 | 34 | 30 | 33 | 23 | 25 | 18 | - |
| | | PA2 | 26 | 22 | 25 | 16 | 18 | 15 | 13 |
| | TSPI0CS0 | PM3 | 33 | 29 | 32 | 22 | 24 | - | - |
| | | PA3 | 25 | 21 | 24 | 15 | 17 | 14 | 12 |
| | TSPI0CS1 | PM4 | 32 | 28 | 31 | 21 | 23 | - | - |
| | | PA4 | 24 | 20 | 23 | 14 | 16 | 13 | - |
| | TSPI0CSIN | PM3 | 33 | 29 | 32 | 22 | 24 | - | - |
| | | PA3 | 25 | 21 | 24 | 15 | 17 | 14 | 12 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Serial Peripheral Interface | TSPI1SCK | PB2 | 39 | 35 | 38 | 28 | 30 | 23 | - |
| | TSPI1TXD | PB3 | 40 | 36 | 39 | 29 | 31 | 24 | - |
| | TSPI1RXD | PB4 | 41 | 37 | 40 | 30 | 32 | 25 | - |
| | TSPI1CS0 | PB5 | 42 | 38 | 41 | 31 | 33 | - | - |
| | TSPI1CS1 | PB6 | 43 | 39 | 42 | 32 | 34 | - | - |
| | TSPI1CSIN | PB5 | 42 | 38 | 41 | 31 | 33 | - | - |

**Table 3.5 Signal Connection List: TSPI ch2,3,4/T32A ch0**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| Serial Peripheral Interface | TSPI2SCK | PP0 | 63 | 53 | 56 | 41 | 43 | 31 | - |
| | | PT2 | 60 | 50 | 53 | - | - | - | - |
| | TSPI2TXD | PP1 | 64 | 54 | 57 | 42 | 44 | 32 | - |
| | | PT3 | 59 | 49 | 52 | - | - | - | - |
| | TSPI2RXD | PP2 | 65 | 55 | 58 | 43 | 45 | 33 | - |
| | | PT4 | 58 | - | - | - | - | - | - |
| | TSPI2CS0 | PT1 | 61 | 51 | 54 | - | - | - | - |
| | TSPI2CS1 | PT0 | 62 | 52 | 55 | - | - | - | - |
| | TSPI2CSIN | PT1 | 61 | 51 | 54 | - | - | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Serial Peripheral Interface | TSPI3SCK | PP5 | 120 | 107 | 110 | 87 | 89 | 72 | - |
| | TSPI3TXD | PP4 | 119 | 106 | 109 | 86 | 88 | 71 | - |
| | TSPI3RXD | PP3 | 118 | 105 | 108 | 85 | 87 | 70 | - |
| | TSPI3CS0 | PP6 | 121 | 108 | 111 | 88 | 90 | 73 | - |
| | TSPI3CS1 | PP7 | 122 | 109 | 112 | 89 | 91 | - | - |
| | TSPI3CSIN | PP6 | 121 | 108 | 111 | 88 | 90 | 73 | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Serial Peripheral Interface | TSPI4SCK | PH4 | 76 | 66 | 69 | - | - | - | - |
| | TSPI4TXD | PH5 | 77 | 67 | 70 | - | - | - | - |
| | TSPI4RXD | PH6 | 78 | 68 | 71 | - | - | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| 32-bit Timer Event Counter | T32A00OUTA | PA0 | 28 | 24 | 27 | 18 | 20 | 17 | 15 |
| | | PM0 | 36 | 32 | 35 | 25 | 27 | 20 | 16 |
| | T32A00OUTB | PA3 | 25 | 21 | 24 | 15 | 17 | 14 | 12 |
| | | PM3 | 33 | 29 | 32 | 22 | 24 | - | - |
| | T32A00OUTC | PA0 | 28 | 24 | 27 | 18 | 20 | 17 | 15 |
| | | PM0 | 36 | 32 | 35 | 25 | 27 | 20 | 16 |
| | T32A00INA0 | PA1 | 27 | 23 | 26 | 17 | 19 | 16 | 14 |
| | | PM1 | 35 | 31 | 34 | 24 | 26 | 19 | - |
| | T32A00INA1 | PA2 | 26 | 22 | 25 | 16 | 18 | 15 | 13 |
| | | PM2 | 34 | 30 | 33 | 23 | 25 | 18 | - |
| | T32A00INB0 | PA4 | 24 | 20 | 23 | 14 | 16 | 13 | - |
| | | PM4 | 32 | 28 | 31 | 21 | 23 | - | - |
| | T32A00INB1 | PA5 | 23 | 19 | 22 | 13 | 15 | 12 | - |
| | | PM5 | 31 | 27 | 30 | 20 | 22 | - | - |
| | T32A00INC0 | PA1 | 27 | 23 | 26 | 17 | 19 | 16 | 14 |
| | | PM1 | 35 | 31 | 34 | 24 | 26 | 19 | - |
| | T32A00INC1 | PA2 | 26 | 22 | 25 | 16 | 18 | 15 | 13 |
| | | PM2 | 34 | 30 | 33 | 23 | 25 | 18 | - |

**Table 3.6 Signal Connection List: T32A ch1,2**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| 32-bit Timer Event Counter | T32A01OUTA | PB0 | 37 | 33 | 36 | 26 | 28 | 21 | 17 |
| | | PP0 | 63 | 53 | 56 | 41 | 43 | 31 | - |
| | T32A01OUTB | PB3 | 40 | 36 | 39 | 29 | 31 | 24 | 20 |
| | T32A01OUTC | PB0 | 37 | 33 | 36 | 26 | 28 | 21 | 17 |
| | | PP0 | 63 | 53 | 56 | 41 | 43 | 31 | - |
| | T32A01INA0 | PB1 | 38 | 34 | 37 | 27 | 29 | 22 | 18 |
| | | PP1 | 64 | 54 | 57 | 42 | 44 | 32 | - |
| | T32A01INA1 | PB2 | 39 | 35 | 38 | 28 | 30 | 23 | 19 |
| | | PP2 | 65 | 55 | 58 | 43 | 45 | 33 | - |
| | T32A01INB0 | PB4 | 41 | 37 | 40 | 30 | 32 | 25 | - |
| | T32A01INB1 | PB5 | 42 | 38 | 41 | 31 | 33 | - | - |
| | T32A01INC0 | PB1 | 38 | 34 | 37 | 27 | 29 | 22 | 18 |
| | | PP1 | 64 | 54 | 57 | 42 | 44 | 32 | - |
| | T32A01INC1 | PB2 | 39 | 35 | 38 | 28 | 30 | 23 | 19 |
| | | PP2 | 65 | 55 | 58 | 43 | 45 | 33 | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| 32-bit Timer Event Counter | T32A02OUTA | PC0 | 83 | 70 | 73 | 54 | 56 | 44 | 36 |
| | | PR0 | 90 | 77 | 80 | 61 | 63 | - | - |
| | T32A02OUTB | PC3 | 86 | 73 | 76 | 57 | 59 | 47 | 38 |
| | T32A02OUTC | PC0 | 83 | 70 | 73 | 54 | 56 | 44 | 36 |
| | | PR0 | 90 | 77 | 80 | 61 | 63 | - | - |
| | T32A02INA0 | PC1 | 84 | 71 | 74 | 55 | 57 | 45 | 37 |
| | | PR1 | 91 | 78 | 81 | 62 | 64 | - | - |
| | T32A02INA1 | PC2 | 85 | 72 | 75 | 56 | 58 | 46 | - |
| | | PR2 | 92 | 79 | 82 | 63 | 65 | - | - |
| | T32A02INB0 | PC4 | 87 | 74 | 77 | 58 | 60 | 48 | 39 |
| | T32A02INB1 | PC5 | 88 | 75 | 78 | 59 | 61 | 49 | - |
| | T32A02INC0 | PC1 | 84 | 71 | 74 | 55 | 57 | 45 | 37 |
| | | PR1 | 91 | 78 | 81 | 62 | 64 | - | - |
| | T32A02INC1 | PC2 | 85 | 72 | 75 | 56 | 58 | 46 | - |
| | | PR2 | 92 | 79 | 82 | 63 | 65 | - | - |

**Table 3.7 Signal Connection List: T32A ch3,4,5**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| 32-bit Timer Event Counter | T32A03OUTA | PJ0 | 104 | 91 | 94 | 71 | 73 | 56 | 44 |
| | T32A03OUTB | PJ3 | 107 | 94 | 97 | 74 | 76 | 59 | 47 |
| | T32A03OUTC | PJ0 | 104 | 91 | 94 | 71 | 73 | 56 | 44 |
| | T32A03INA0 | PJ1 | 105 | 92 | 95 | 72 | 74 | 57 | 45 |
| | T32A03INA1 | PJ2 | 106 | 93 | 96 | 73 | 75 | 58 | 46 |
| | T32A03INB0 | PJ4 | 108 | 95 | 98 | 75 | 77 | 60 | 48 |
| | T32A03INB1 | PJ5 | 109 | 96 | 99 | 76 | 78 | 61 | 49 |
| | T32A03INC0 | PJ1 | 105 | 92 | 95 | 72 | 74 | 57 | 45 |
| | T32A03INC1 | PJ2 | 106 | 93 | 96 | 73 | 75 | 58 | 46 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| 32-bit Timer Event Counter | T32A04OUTA | PK2 | 112 | 99 | 102 | 79 | 81 | 64 | 52 |
| | T32A04OUTB | PK5 | 115 | 102 | 105 | 82 | 84 | 67 | 55 |
| | T32A04OUTC | PK2 | 112 | 99 | 102 | 79 | 81 | 64 | 52 |
| | T32A04INA0 | PK3 | 113 | 100 | 103 | 80 | 82 | 65 | 53 |
| | T32A04INA1 | PK4 | 114 | 101 | 104 | 81 | 83 | 66 | 54 |
| | T32A04INB0 | PK6 | 116 | 103 | 106 | 83 | 85 | 68 | 56 |
| | T32A04INB1 | PK7 | 117 | 104 | 107 | 84 | 86 | 69 | - |
| | T32A04INC0 | PK3 | 113 | 100 | 103 | 80 | 82 | 65 | 53 |
| | T32A04INC1 | PK4 | 114 | 101 | 104 | 81 | 83 | 66 | 54 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| 32-bit Timer Event Counter | T32A05OUTA | PN0 | 103 | 90 | 93 | 70 | 72 | 55 | - |
| | T32A05OUTB | PN3 | 100 | 87 | 90 | 67 | 69 | 52 | 41 |
| | T32A05OUTC | PN0 | 103 | 90 | 93 | 70 | 72 | 55 | |
| | T32A05INA0 | PN1 | 102 | 89 | 92 | 69 | 71 | 54 | 43 |
| | T32A05INA1 | PN2 | 101 | 88 | 91 | 68 | 70 | 53 | 42 |
| | T32A05INB0 | PN4 | 99 | 86 | 89 | 66 | 68 | 51 | 40 |
| | T32A05INB1 | PN5 | 98 | 85 | 88 | 65 | 67 | - | - |
| | T32A05INC0 | PN1 | 102 | 89 | 92 | 69 | 71 | 54 | 43 |
| | T32A05INC1 | PN2 | 101 | 88 | 91 | 68 | 70 | 53 | 42 |

**Table 3.8 Signal Connection List: T32A ch6,7**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| 32-bit Timer Event Counter | T32A06OUTA | PL5 | 52 | 46 | 49 | 39 | 41 | - | - |
| | | PT5 | 57 | - | - | - | - | - | - |
| | T32A06OUTB | PL2 | 49 | 43 | 46 | 36 | 38 | 28 | 23 |
| | | PT2 | 60 | 50 | 53 | - | - | - | - |
| | T32A06OUTC | PL5 | 52 | 46 | 49 | 39 | 41 | - | - |
| | | PT5 | 57 | - | - | - | - | - | - |
| | T32A06INA0 | PL6 | 53 | 47 | 50 | 40 | 42 | - | - |
| | | PT6 | 56 | - | - | - | - | - | - |
| | T32A06INA1 | PL7 | 54 | 48 | 51 | - | - | - | - |
| | | PT7 | 55 | - | - | - | - | - | - |
| | T32A06INB0 | PL3 | 50 | 44 | 47 | 37 | 39 | 29 | 24 |
| | | PT3 | 59 | 49 | 52 | - | - | - | - |
| | T32A06INB1 | PL4 | 51 | 45 | 48 | 38 | 40 | 30 | 25 |
| | | PT4 | 58 | - | - | - | - | - | - |
| | T32A06INC0 | PL6 | 53 | 47 | 50 | 40 | 42 | - | - |
| | | PT6 | 56 | - | - | - | - | - | - |
| | T32A06INC1 | PL7 | 54 | 48 | 51 | - | - | - | - |
| | | PT7 | 55 | - | - | - | - | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| 32-bit Timer Event Counter | T32A07OUTA | PG2 | 15 | 11 | 14 | - | - | - | - |
| | T32A07OUTB | PG5 | 18 | 14 | 17 | - | - | - | - |
| | T32A07OUTC | PG2 | 15 | 11 | 14 | - | - | - | - |
| | T32A07INA0 | PG3 | 16 | 12 | 15 | - | - | - | - |
| | T32A07INA1 | PG4 | 17 | 13 | 16 | - | - | - | - |
| | T32A07INB0 | PG6 | 19 | 15 | 18 | - | - | - | - |
| | T32A07INB1 | PG7 | 20 | 16 | 19 | - | - | - | - |
| | T32A07INC0 | PG3 | 16 | 12 | 15 | - | - | - | - |
| | T32A07INC1 | PG4 | 17 | 13 | 16 | - | - | - | - |

**Table 3.9 Signal Connection List: ADC/DAC**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| 12-bit Analog to Digital Convertor | AINA00 | PD0 | 6 | 6 | 9 | 6 | 8 | 5 | 5 |
| | AINA01 | PD1 | 5 | 5 | 8 | 5 | 7 | 4 | 4 |
| | AINA02 | PD2 | 4 | 4 | 7 | 4 | 6 | 3 | 3 |
| | AINA03 | PD3 | 3 | 3 | 6 | 3 | 5 | - | - |
| | AINA04 | PE0 | 2 | 2 | 5 | 2 | 4 | 2 | 2 |
| | AINA05 | PE1 | 1 | 1 | 4 | 1 | 3 | 1 | 1 |
| | AINA06 | PE2 | 144 | 128 | 3 | 100 | 2 | 80 | 64 |
| | AINA07 | PE3 | 143 | 127 | 2 | 99 | 1 | 79 | 63 |
| | AINA08 | PE4 | 142 | 126 | 1 | 98 | 100 | 78 | 62 |
| | AINA09 | PE5 | 141 | 125 | 128 | 97 | 99 | 77 | 61 |
| | AINA10 | PE6 | 140 | 124 | 127 | 96 | 98 | 76 | 60 |
| | AINA11 | PF0 | 139 | 123 | 126 | 95 | 97 | 75 | 59 |
| | AINA12 | PF1 | 138 | 122 | 125 | 94 | 96 | 74 | 58 |
| | AINA13 | PF2 | 137 | 121 | 124 | 93 | 95 | - | - |
| | AINA14 | PF3 | 136 | 120 | 123 | 92 | 94 | - | - |
| | AINA15 | PF4 | 135 | 119 | 122 | 91 | 93 | - | - |
| | AINA16 | PF5 | 134 | 118 | 121 | 90 | 92 | - | - |
| | AINA17 | PF6 | 133 | 117 | 120 | - | - | - | - |
| | AINA18 | PF7 | 132 | 116 | 119 | - | - | - | - |
| | AINA19 | PD4 | 131 | - | - | - | - | - | - |
| | AINA20 | PD5 | 130 | - | - | - | - | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| 8-bit Digital to Analog Convertor | DAC0 | PG0 | 9 | 9 | 12 | 9 | 11 | 8 | 8 |
| | DAC1 | PG1 | 10 | 10 | 13 | 10 | 12 | 9 | 9 |

**Table 3.10 Signal Connection List: INT**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| Exception | INT00 | PC0 | 83 | 70 | 73 | 54 | 56 | 44 | 36 |
| | INT01 | PC1 | 84 | 71 | 74 | 55 | 57 | 45 | 37 |
| | INT02 | PC2 | 85 | 72 | 75 | 56 | 58 | 46 | - |
| | INT03 | PB1 | 38 | 34 | 37 | 27 | 29 | 22 | 18 |
| | INT04 | PJ4 | 108 | 95 | 98 | 75 | 77 | 60 | 48 |
| | INT05 | PK1 | 111 | 98 | 101 | 78 | 80 | 63 | 51 |
| | INT06 | PH3 | 74 | 64 | 67 | 52 | 54 | 42 | 34 |
| | INT07 | PA6 | 22 | 18 | 21 | 12 | 14 | 11 | 11 |
| | INT08 | PL3 | 50 | 44 | 47 | 37 | 39 | 29 | 24 |
| | INT09 | PM2 | 34 | 30 | 33 | 23 | 25 | 18 | - |
| | INT10 | PN3 | 100 | 87 | 90 | 67 | 69 | 52 | 41 |
| | INT11 | PA7 | 21 | 17 | 20 | 11 | 13 | 10 | 10 |
| | INT12 | PL4 | 51 | 45 | 48 | 38 | 40 | 30 | 25 |
| | INT13 | PK7 | 117 | 104 | 107 | 84 | 86 | 69 | - |
| | INT14 | PP3 | 118 | 105 | 108 | 85 | 87 | 70 | 57 |
| | INT15 | PM6 | 30 | 26 | 29 | 19 | 21 | - | - |
| | INT16 | PB7 | 44 | 40 | 43 | 33 | 35 | - | - |
| | INT17 | PV2 | 125 | 112 | 115 | - | - | - | - |
| | INT18 | PV3 | 126 | 113 | 116 | - | - | - | - |
| | INT19 | PH4 | 76 | 66 | 69 | - | - | - | - |
| | INT20 | PH5 | 77 | 67 | 70 | - | - | - | - |
| | INT21 | PH6 | 78 | 68 | 71 | - | - | - | - |
| | INT22 | PH7 | 79 | 69 | 72 | - | - | - | - |
| | INT23 | PT0 | 62 | 52 | 55 | - | - | - | - |
| | INT24 | PT1 | 61 | 51 | 54 | - | - | - | - |
| | INT25 | PT2 | 60 | 50 | 53 | - | - | - | - |
| | INT26 | PT3 | 59 | 49 | 52 | - | - | - | - |
| | INT27 | PG2 | 15 | 11 | 14 | - | - | - | - |
| | INT28 | PG3 | 16 | 12 | 15 | - | - | - | - |
| | INT29 | PT7 | 55 | - | - | - | - | - | - |
| | INT30 | PU0 | 45 | - | - | - | - | - | - |
| | INT31 | PU1 | 46 | - | - | - | - | - | - |
| | INT32 | PF3 | 136 | 120 | 123 | 92 | 94 | - | - |
| | INT33 | PF2 | 137 | 121 | 124 | 93 | 95 | - | - |

**Table 3.11 Signal Connection List: A-PMD/A-ENC/TRGSEL/REM/RTC**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced Programmable Motor Control Circuit | UO0 | PJ0 | 104 | 91 | 94 | 71 | 73 | 56 | 44 |
| | XO0 | PJ1 | 105 | 92 | 95 | 72 | 74 | 57 | 45 |
| | VO0 | PJ2 | 106 | 93 | 96 | 73 | 75 | 58 | 46 |
| | YO0 | PJ3 | 107 | 94 | 97 | 74 | 76 | 59 | 47 |
| | WO0 | PJ4 | 108 | 95 | 98 | 75 | 77 | 60 | 48 |
| | ZO0 | PJ5 | 109 | 96 | 99 | 76 | 78 | 61 | 49 |
| | EMG0 | PK0 | 110 | 97 | 100 | 77 | 79 | 62 | 50 |
| | OVV0 | PK1 | 111 | 98 | 101 | 78 | 80 | 63 | 51 |
| | PMD0DBG | PP6 | 121 | 108 | 111 | 88 | 90 | 73 | - |
| Advanced Encoder Input Circuit | ENC0A | PA0 | 28 | 24 | 27 | 18 | 20 | 17 | 15 |
| | ENC0B | PA1 | 27 | 23 | 26 | 17 | 19 | 16 | 14 |
| | ENC0Z | PA2 | 26 | 22 | 25 | 16 | 18 | 15 | 13 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Product Information (Trigger Selector) | TRGIN0 | PB1 | 38 | 34 | 37 | 27 | 29 | 22 | 18 |
| | TRGIN1 | PA3 | 25 | 21 | 24 | 15 | 17 | 14 | 12 |
| | TRGIN2 | PN3 | 100 | 87 | 90 | 67 | 69 | 52 | 41 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Remote Control Signal preprocessor | RXIN0 | PB1 | 38 | 34 | 37 | 27 | 29 | 22 | 18 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Real Time Clock | RTCOUT | PC2 | 85 | 72 | 75 | 56 | 58 | 46 | - |

**Table 3.12 Signal Connection List: DLCD**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| LCD Display Control Circuit | DCOM0 | PC3 | 86 | 73 | 76 | 57 | 59 | 47 | - |
| | DCOM1 | PC2 | 85 | 72 | 75 | 56 | 58 | 46 | - |
| | DCOM2 | PC1 | 84 | 71 | 74 | 55 | 57 | 45 | - |
| | DCOM3 | PC0 | 83 | 70 | 73 | 54 | 56 | 44 | - |
| | SEG00 | PV3 | 126 | 113 | 116 | - | - | - | - |
| | SEG01 | PV2 | 125 | 112 | 115 | - | - | - | - |
| | SEG02 | PV1 | 124 | 111 | 114 | - | - | - | - |
| | SEG03 | PV0 | 123 | 110 | 113 | - | - | - | - |
| | SEG04 | PP7 | 122 | 109 | 112 | 89 | 91 | - | - |
| | SEG05 | PP6 | 121 | 108 | 111 | 88 | 90 | 73 | - |
| | SEG06 | PP5 | 120 | 107 | 110 | 87 | 89 | 72 | - |
| | SEG07 | PP4 | 119 | 106 | 109 | 86 | 88 | 71 | - |
| | SEG08 | PP3 | 118 | 105 | 108 | 85 | 87 | 70 | - |
| | SEG09 | PK7 | 117 | 104 | 107 | 84 | 86 | 69 | - |
| | SEG10 | PK6 | 116 | 103 | 106 | 83 | 85 | 68 | - |
| | SEG11 | PK5 | 115 | 102 | 105 | 82 | 84 | 67 | - |
| | SEG12 | PK4 | 114 | 101 | 104 | 81 | 83 | 66 | - |
| | SEG13 | PK3 | 113 | 100 | 103 | 80 | 82 | 65 | - |
| | SEG14 | PK2 | 112 | 99 | 102 | 79 | 81 | 64 | - |
| | SEG15 | PK1 | 111 | 98 | 101 | 78 | 80 | 63 | - |
| | SEG16 | PK0 | 110 | 97 | 100 | 77 | 79 | 62 | - |
| | SEG17 | PJ5 | 109 | 96 | 99 | 76 | 78 | 61 | - |
| | SEG18 | PJ4 | 108 | 95 | 98 | 75 | 77 | 60 | - |
| | SEG19 | PJ3 | 107 | 94 | 97 | 74 | 76 | 59 | - |
| | SEG20 | PJ2 | 106 | 93 | 96 | 73 | 75 | 58 | - |
| | SEG21 | PJ1 | 105 | 92 | 95 | 72 | 74 | 57 | - |
| | SEG22 | PJ0 | 104 | 91 | 94 | 71 | 73 | 56 | - |
| | SEG23 | PN0 | 103 | 90 | 93 | 70 | 72 | 55 | - |
| | SEG24 | PN1 | 102 | 89 | 92 | 69 | 71 | 54 | - |
| | SEG25 | PN2 | 101 | 88 | 91 | 68 | 70 | 53 | - |
| | SEG26 | PN3 | 100 | 87 | 90 | 67 | 69 | 52 | - |
| | SEG27 | PN4 | 99 | 86 | 89 | 66 | 68 | 51 | - |
| | SEG28 | PN5 | 98 | 85 | 88 | 65 | 67 | - | - |
| | SEG29 | PR7 | 97 | 84 | 87 | - | - | - | - |
| | SEG30 | PR6 | 96 | 83 | 86 | - | - | - | - |
| | SEG31 | PR5 | 95 | 82 | 85 | - | - | - | - |
| | SEG32 | PR4 | 94 | 81 | 84 | - | - | - | - |
| | SEG33 | PR3 | 93 | 80 | 83 | 64 | 66 | - | - |
| | SEG34 | PR2 | 92 | 79 | 82 | 63 | 65 | - | - |
| | SEG35 | PR1 | 91 | 78 | 81 | 62 | 64 | - | - |

**Table 3.13 Signal Connection List: DLCD/ JTAG/SW/TRACE/Control Pin/IO**

| Related reference manual | Function pin name | Port name | M3HQ (LQFP144) | M3HP (LQFP128-1414) | M3HP (LQFP128-1420) | M3HN (LQFP100) | M3HN (QFP100) | M3HM (LQFP80) | M3HL (LQFP64) |
|---|---|---|---|---|---|---|---|---|---|
| LCD Display Control Circuit | SEG36 | PR0 | 90 | 77 | 80 | 61 | 63 | - | - |
| | SEG37 | PC6 | 89 | 76 | 79 | 60 | 62 | 50 | - |
| | SEG38 | PC5 | 88 | 75 | 78 | 59 | 61 | 49 | - |
| | SEG39 | PC4 | 87 | 74 | 77 | 58 | 60 | 48 | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Debug Interface | TMS | PL4 | 51 | 45 | 48 | 38 | 40 | 30 | 25 |
| | TCK | PL3 | 50 | 44 | 47 | 37 | 39 | 29 | 24 |
| | TDO | PL2 | 49 | 43 | 46 | 36 | 38 | 28 | 23 |
| | TDI | PL1 | 48 | 42 | 45 | 35 | 37 | 27 | 22 |
| | TRST_N | PL0 | 47 | 41 | 44 | 34 | 36 | 26 | 21 |
| | SWDIO | PL4 | 51 | 45 | 48 | 38 | 40 | 30 | 25 |
| | SWCLK | PL3 | 50 | 44 | 47 | 37 | 39 | 29 | 24 |
| | SWV | PL2 | 49 | 43 | 46 | 36 | 38 | 28 | 23 |
| | TRACECLK | PM0 | 36 | 32 | 35 | 25 | 27 | 20 | - |
| | TRACEDATA0 | PM1 | 35 | 31 | 34 | 24 | 26 | 19 | - |
| | TRACEDATA1 | PM2 | 34 | 30 | 33 | 23 | 25 | 18 | - |
| | TRACEDATA2 | PM3 | 33 | 29 | 32 | 22 | 24 | - | - |
| | TRACEDATA3 | PM4 | 32 | 28 | 31 | 21 | 23 | - | - |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Clock Control and Operation Mode | SCOUT | PB0 | 37 | 33 | 36 | 26 | 28 | 21 | 17 |
| | X1 | PH0 | 70 | 60 | 63 | 48 | 50 | 38 | 30 |
| | X2 | PH1 | 71 | 61 | 64 | 49 | 51 | 39 | 31 |
| | XT1 | PH2 | 73 | 63 | 66 | 51 | 53 | 41 | 33 |
| | XT2 | PH3 | 74 | 64 | 67 | 52 | 54 | 42 | 34 |
| | EHCLKIN | PH0 | 70 | 60 | 63 | 48 | 50 | 38 | 30 |
| Flash Memory | BOOT_N | PB0 | 37 | 33 | 36 | 26 | 28 | 21 | 17 |
| **Related reference manual** | **Function pin name** | **Port name** | **M3HQ (LQFP144)** | **M3HP (LQFP128-1414)** | **M3HP (LQFP128-1420)** | **M3HN (LQFP100)** | **M3HN (QFP100)** | **M3HM (LQFP80)** | **M3HL (LQFP64)** |
| Input Output Port | N/A | PM7 | 29 | 25 | 28 | - | - | - | - |
| | | PU2 | 14 | - | - | - | - | - | - |
| | | PU3 | 13 | - | - | - | - | - | - |
| | | PU4 | 12 | - | - | - | - | - | - |
| | | PU5 | 11 | - | - | - | - | - | - |
| | | PV4 | 127 | - | - | - | - | - | - |
| | | PW0 | 68 | 58 | 61 | 46 | 48 | 36 | 28 |

# 4. Registers

The following registers should be set appropriately to use the ports.

Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

"x" and "n" in the following table show a port name and a function number, respectively.

| Register name | | Type | Setting value | Description |
|---|---|---|---|---|
| ***[PxDATA]*** | Data Register | R/W | 0 or 1 | Read from and write to a port. |
| ***[PxCR]*** | Output Control Register | R/W | 0: Output disabled<br>1: Output enabled | Output control. |
| ***[PxFRn]*** | Function Register n | R/W | 0: PORT<br>1: Function | Function setting.<br>When this register is set to “1”, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled. |
| ***[PxOD]*** | Open-Drain Control Register | R/W | 0: CMOS<br>1: Open-drain | Programmable open drain control.<br>The programmable open-drain is a pseudo open-drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** = 1. |
| ***[PxPUP]*** | Pull-up Control Register | R/W | 0: Pull-up disabled<br>1: Pull-up enabled | Programmable pull-up control. |
| ***[PxPDN]*** | Pull-down Control Register | R/W | 0: Pull-down disabled<br>1: Pull-down enabled | Programmable pull-down control. |
| ***[PxIE]*** | Input Control Register | R/W | 0: Input disabled<br>1: Input enabled | Input control.<br>It takes up to 100ns that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled. |

## 4.1. List of Register

When the bit which is assigned to no functions is read, 0 is returned. The write to the bit is ignored.

**Table 4.1 Ports Base Address**

| Peripheral function | | Channel/unit | Base address |
|---|---|---|---|
| Input/output ports | PA | - | 0x400C0000 |
| | PB | - | 0x400C0100 |
| | PC | - | 0x400C0200 |
| | PD | - | 0x400C0300 |
| | PE | - | 0x400C0400 |
| | PF | - | 0x400C0500 |
| | PG | - | 0x400C0600 |
| | PH | - | 0x400C0700 |
| | PJ | - | 0x400C0800 |
| | PK | - | 0x400C0900 |
| | PL | - | 0x400C0A00 |
| | PM | - | 0x400C0B00 |
| | PN | - | 0x400C0C00 |
| | PP | - | 0x400C0D00 |
| | PR | - | 0x400C0E00 |
| | PT | - | 0x400C0F00 |
| | PU | - | 0x400C1000 |
| | PV | - | 0x400C1100 |
| | PW | - | 0x400C1200 |

**Table 4.2 Register List (1/4)**

| Register name | Address (Base+) | Port A | Port B | Port C | Port D | Port E |
|---|---|---|---|---|---|---|
| Data Register | 0x0000 | *[PADATA]* | *[PBDATA]* | *[PCDATA]* | *[PDDATA]* | *[PEDATA]* |
| Output Control Register | 0x0004 | *[PACR]* | *[PBCR]* | *[PCCR]* | *[PDCR]* | *[PECR]* |
| Function Register 1 | 0x0008 | *[PAFR1]* | *[PBFR1]* | *[PCFR1]* | - | - |
| Function Register 2 | 0x000C | *[PAFR2]* | *[PBFR2]* | *[PCFR2]* | - | - |
| Function Register 3 | 0x0010 | *[PAFR3]* | *[PBFR3]* | *[PCFR3]* | - | - |
| Function Register 4 | 0x0014 | *[PAFR4]* | *[PBFR4]* | *[PCFR4]* | - | - |
| Function Register 5 | 0x0018 | *[PAFR5]* | *[PBFR5]* | *[PCFR5]* | - | - |
| Function Register 6 | 0x001C | *[PAFR6]* | *[PBFR6]* | *[PCFR6]* | - | - |
| Open-Drain Control Register | 0x0028 | *[PAOD]* | *[PBOD]* | *[PCOD]* | *[PDOD]* | *[PEOD]* |
| Pull-up Control Register | 0x002C | *[PAPUP]* | *[PBPUP]* | *[PCPUP]* | *[PDPUP]* | *[PEPUP]* |
| Pull-down Control Register | 0x0030 | *[PAPDN]* | *[PBPDN]* | *[PCPDN]* | *[PDPDN]* | *[PEPDN]* |
| Input Control Register | 0x0038 | *[PAIE]* | *[PBIE]* | *[PCIE]* | *[PDIE]* | *[PEIE]* |

Note: Do not access the addresses described as "-"

**Table 4.3 Register List (2/4)**

| Register name | Address (Base+) | Port F | Port G | Port H | Port J | Port K |
|---|---|---|---|---|---|---|
| Data Register | 0x0000 | *[PFDATA]* | *[PGDATA]* | *[PHDATA]* | *[PJDATA]* | *[PKDATA]* |
| Output Control Register | 0x0004 | *[PFCR]* | *[PGCR]* | *[PHCR]* | *[PJCR]* | *[PKCR]* |
| Function Register 1 | 0x0008 | - | *[PGFR1]* | *[PHFR1]* | *[PJFR1]* | *[PKFR1]* |
| Function Register 2 | 0x000C | - | *[PGFR2]* | - | *[PJFR2]* | *[PKFR2]* |
| Function Register 3 | 0x0010 | - | *[PGFR3]* | - | *[PJFR3]* | *[PKFR3]* |
| Function Register 4 | 0x0014 | - | *[PGFR4]* | - | *[PJFR4]* | *[PKFR4]* |
| Function Register 5 | 0x0018 | - | - | - | *[PJFR5]* | *[PKFR5]* |
| Function Register 6 | 0x001C | - | - | - | *[PJFR6]* | *[PKFR6]* |
| Open-Drain Control Register | 0x0028 | *[PFOD]* | *[PGOD]* | *[PHOD]* | *[PJOD]* | *[PKOD]* |
| Pull-up Control Register | 0x002C | *[PFPUP]* | *[PGPUP]* | *[PHPUP]* | *[PJPUP]* | *[PKPUP]* |
| Pull-down Control Register | 0x0030 | *[PFPDN]* | *[PGPDN]* | *[PHPDN]* | *[PJPDN]* | *[PKPDN]* |
| Input Control Register | 0x0038 | *[PFIE]* | *[PGIE]* | *[PHIE]* | *[PJIE]* | *[PKIE]* |

Note: Do not access the addresses described as "-"

**Table 4.4 Register List (3/4)**

| Register name | Address (Base+) | Port L | Port M | Port N | Port P | Port R |
|---|---|---|---|---|---|---|
| Data Register | 0x0000 | *[PLDATA]* | *[PMDATA]* | *[PNDATA]* | *[PPDATA]* | *[PRDATA]* |
| Output Control Register | 0x0004 | *[PLCR]* | *[PMCR]* | *[PNCR]* | *[PPCR]* | *[PRCR]* |
| Function Register 1 | 0x0008 | *[PLFR1]* | *[PMFR1]* | *[PNFR1]* | *[PPFR1]* | *[PRFR1]* |
| Function Register 2 | 0x000C | *[PLFR2]* | *[PMFR2]* | *[PNFR2]* | *[PPFR2]* | *[PRFR2]* |
| Function Register 3 | 0x0010 | *[PLFR3]* | *[PMFR3]* | *[PNFR3]* | *[PPFR3]* | *[PRFR3]* |
| Function Register 4 | 0x0014 | *[PLFR4]* | *[PMFR4]* | *[PNFR4]* | *[PPFR4]* | *[PRFR4]* |
| Function Register 5 | 0x0018 | *[PLFR5]* | *[PMFR5]* | *[PNFR5]* | - | - |
| Function Register 6 | 0x001C | - | *[PMFR6]* | *[PNFR6]* | *[PPFR6]* | *[PRFR6]* |
| Open-Drain Control Register | 0x0028 | *[PLOD]* | *[PMOD]* | *[PNOD]* | *[PPOD]* | *[PROD]* |
| Pull-up Control Register | 0x002C | *[PLPUP]* | *[PMPUP]* | *[PNPUP]* | *[PPPUP]* | *[PRPUP]* |
| Pull-down Control Register | 0x0030 | *[PLPDN]* | *[PMPDN]* | *[PNPDN]* | *[PPPDN]* | *[PRPDN]* |
| Input Control Register | 0x0038 | *[PLIE]* | *[PMIE]* | *[PNIE]* | *[PPIE]* | *[PRIE]* |

Note: Do not access the addresses described as "-"

**Table 4.5 Register List (4/4)**

| Register name | Address (Base+) | Port T | Port U | Port V | Port W |
|---|---|---|---|---|---|
| Data Register | 0x0000 | *[PTDATA]* | *[PUDATA]* | *[PVDATA]* | *[PWDATA]* |
| Output Control Register | 0x0004 | *[PTCR]* | *[PUCR]* | *[PVCR]* | *[PWCR]* |
| Function Register 1 | 0x0008 | *[PTFR1]* | - | *[PVFR1]* | - |
| Function Register 2 | 0x000C | *[PTFR2]* | - | *[PVFR2]* | - |
| Function Register 3 | 0x0010 | *[PTFR3]* | - | - | - |
| Function Register 4 | 0x0014 | *[PTFR4]* | - | - | - |
| Function Register 5 | 0x0018 | - | - | - | - |
| Function Register 6 | 0x001C | - | - | *[PVFR6]* | - |
| Open-Drain Control Register | 0x0028 | *[PTOD]* | *[PUOD]* | *[PVOD]* | *[PWOD]* |
| Pull-up Control Register | 0x002C | *[PTPUP]* | *[PUPUP]* | *[PVPUP]* | *[PWPUP]* |
| Pull-down Control Register | 0x0030 | *[PTPDN]* | *[PUPDN]* | *[PVPDN]* | *[PWPDN]* |
| Input Control Register | 0x0038 | *[PTIE]* | *[PUIE]* | *[PVIE]* | *[PWIE]* |

Note: Do not access the addresses described as "-"

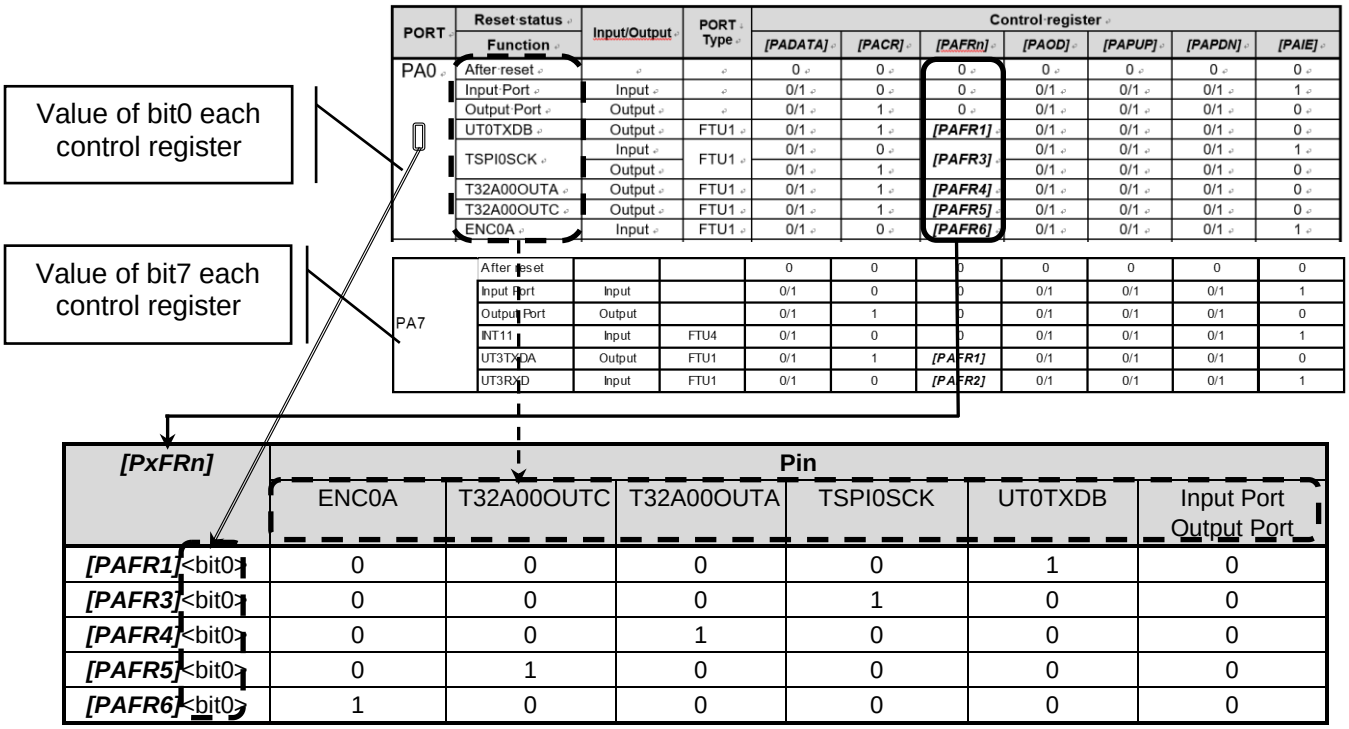
## 4.2. List of Port Functions and Settings

It is explained about viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the N/A in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.




| PORT | Function | Input/Output | PORT Type | [PADATA] | [PACR] | [PAFRn] | [PAOD] | [PAPUP] | [PAPDN] | [PAIE] |
|---|---|---|---|---|---|---|---|---|---|---|
| PA0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0TXDB | Output | FTU1 | 0/1 | 1 | [PAFR1] | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0SCK | Input | FTU1 | 0/1 | 0 | [PAFR3] | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTA | Output | FTU1 | 0/1 | 1 | [PAFR4] | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTC | Output | FTU1 | 0/1 | 1 | [PAFR5] | 0/1 | 0/1 | 0/1 | 0 |
| | ENC0A | Input | FTU1 | 0/1 | 0 | [PAFR6] | 0/1 | 0/1 | 0/1 | 1 |
| PA7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT11 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT3TXDA | Output | FTU1 | 0/1 | 1 | [PAFR1] | 0/1 | 0/1 | 0/1 | 0 |
| | UT3RXD | Input | FTU1 | 0/1 | 0 | [PAFR2] | 0/1 | 0/1 | 0/1 | 1 |

| [PxFRn] | Pin | | | | | |
|---|---|---|---|---|---|---|
| | ENC0A | T32A00OUTC | T32A00OUTA | TSPI0SCK | UT0TXDB | Input Port Output Port |
| [PAFR1]<bit0> | 0 | 0 | 0 | 0 | 1 | 0 |
| [PAFR3]<bit0> | 0 | 0 | 0 | 1 | 0 | 0 |
| [PAFR4]<bit0> | 0 | 0 | 1 | 0 | 0 | 0 |
| [PAFR5]<bit0> | 0 | 1 | 0 | 0 | 0 | 0 |
| [PAFR6]<bit0> | 1 | 0 | 0 | 0 | 0 | 0 |

Note: The register value after reset is the initial value before the clock is enabled.

### 4.2.1. Setting of Using Alternated Pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and enable output control register (***[PxCR]***<bit m>=1), then set the peripheral functions. If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), then set the peripheral functions.

To use peripheral functions such as $I^2C$, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), then set the peripheral function.

- When multiple functions are assigned to the same pin, please choose only one function for usage.
- When same function is assigned to multiple pins, please the function use exclusively.

## 4.2.2. PORT A

**Table 4.6 Port A Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PADATA]* | *[PACR]* | *[PAFRn]* | *[PAOD]* | *[PAPUP]* | *[PAPDN]* | *[PAIE]* |
| PA0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0TXDB | Output | FTU1 | 0/1 | 1 | ***[PAFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0SCK | Input | FTU1 | 0/1 | 0 | ***[PAFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTA | Output | FTU1 | 0/1 | 1 | ***[PAFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTC | Output | FTU1 | 0/1 | 1 | ***[PAFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | ENC0A | Input | FTU1 | 0/1 | 0 | ***[PAFR6]*** | 0/1 | 0/1 | 0/1 | 1 |
| PA1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0TXDA | Output | FTU1 | 0/1 | 1 | ***[PAFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT0RXD | Input | FTU1 | 0/1 | 0 | ***[PAFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI0TXD | Output | FTU2 | 0/1 | 1 | ***[PAFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00INA0 | Input | FTU1 | 0/1 | 0 | ***[PAFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A00INC0 | Input | FTU1 | 0/1 | 0 | ***[PAFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | ENC0B | Input | FTU1 | 0/1 | 0 | ***[PAFR6]*** | 0/1 | 0/1 | 0/1 | 1 |
| PA2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0RXD | Input | FTU1 | 0/1 | 0 | ***[PAFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT0TXDA | Output | FTU1 | 0/1 | 1 | ***[PAFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0RXD | Input | FTU1 | 0/1 | 0 | ***[PAFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A00INA1 | Input | FTU1 | 0/1 | 0 | ***[PAFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A00INC1 | Input | FTU1 | 0/1 | 0 | ***[PAFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | ENC0Z | Input | FTU1 | 0/1 | 0 | ***[PAFR6]*** | 0/1 | 0/1 | 0/1 | 1 |
| PA3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0CSIN | Input | FTU1 | 0/1 | 0 | ***[PAFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI0CS0 | Output | FTU1 | 0/1 | 1 | ***[PAFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTB | Output | FTU1 | 0/1 | 1 | ***[PAFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TRGIN1 | Input | FTU1 | 0/1 | 0 | ***[PAFR6]*** | 0/1 | 0/1 | 0/1 | 1 |
| PA4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | I2C1SCL | I/O | FTU1 | 0/1 | 1 | ***[PAFR1]*** | 1 | 0/1 | 0/1 | 1 |
| | EI2C1SCL | I/O | FTU12 | 0/1 | 1 | ***[PAFR2]*** | 1 | 0/1 | 0/1 | 1 |
| | TSPI0CS1 | Output | FTU1 | 0/1 | 1 | ***[PAFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00INB0 | Input | FTU1 | 0/1 | 0 | ***[PAFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PA5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | I2C1SDA | I/O | FTU1 | 0/1 | 1 | ***[PAFR1]*** | 1 | 0/1 | 0/1 | 1 |
| | EI2C1SDA | I/O | FTU12 | 0/1 | 1 | ***[PAFR2]*** | 1 | 0/1 | 0/1 | 1 |
| | T32A00INB1 | Input | FTU1 | 0/1 | 0 | ***[PAFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PA6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT07 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT3RXD | Input | FTU1 | 0/1 | 0 | ***[PAFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT3TXDA | Output | FTU1 | 0/1 | 1 | ***[PAFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| PA7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT11 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT3TXDA | Output | FTU1 | 0/1 | 1 | ***[PAFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT3RXD | Input | FTU1 | 0/1 | 0 | ***[PAFR2]*** | 0/1 | 0/1 | 0/1 | 1 |

### 4.2.3. PORT B

**Table 4.7 Port B Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PBDATA]* | *[PBCR]* | *[PBFRn]* | *[PBOD]* | *[PBPUP]* | *[PBPDN]* | *[PBIE]* |
| PB0 | During reset (BOOT_N) | Input | FTU6 | 0 | 0 | 0 | 0 | 0 (Note1) | 0 | N/A (Note1) |
| | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | N/A |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | N/A |
| | T32A01OUTA | Output | FTU1 | 0/1 | 1 | ***[PBFR4]*** | 0/1 | 0/1 | 0/1 | N/A |
| | T32A01OUTC | Output | FTU1 | 0/1 | 1 | ***[PBFR5]*** | 0/1 | 0/1 | 0/1 | N/A |
| | SCOUT | Output | FTU1 | 0/1 | 1 | ***[PBFR6]*** | 0/1 | 0/1 | 0/1 | N/A |
| PB1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT03 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | RXIN0 | Input | FTU1 | 0/1 | 0 | ***[PBFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A01INA0 | Input | FTU1 | 0/1 | 0 | ***[PBFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A01INC0 | Input | FTU1 | 0/1 | 0 | ***[PBFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TRGIN0 | Input | FTU1 | 0/1 | 0 | ***[PBFR6]*** | 0/1 | 0/1 | 0/1 | 1 |
| PB2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT2TXDA | Output | FTU1 | 0/1 | 1 | ***[PBFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT2RXD | Input | FTU1 | 0/1 | 0 | ***[PBFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI1SCK | Input | FTU1 | 0/1 | 0 | ***[PBFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| | T32A01INA1 | Input | FTU1 | 0/1 | 0 | ***[PBFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A01INC1 | Input | FTU1 | 0/1 | 0 | ***[PBFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| PB3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT2RXD | Input | FTU1 | 0/1 | 0 | ***[PBFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT2TXDA | Output | FTU1 | 0/1 | 1 | ***[PBFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI1TXD | Output | FTU2 | 0/1 | 1 | ***[PBFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A01OUTB | Output | FTU1 | 0/1 | 1 | ***[PBFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| PB4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT2CTS_N | Input | FTU1 | 0/1 | 0 | ***[PBFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT2RTS_N | Output | FTU1 | 0/1 | 1 | ***[PBFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI1RXD | Input | FTU1 | 0/1 | 0 | ***[PBFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A01INB0 | Input | FTU1 | 0/1 | 0 | ***[PBFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PB5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT2RTS_N | Output | FTU1 | 0/1 | 1 | ***[PBFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT2CTS_N | Input | FTU1 | 0/1 | 0 | ***[PBFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI1CS0 | Output | FTU1 | 0/1 | 1 | ***[PBFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A01INB1 | Input | FTU1 | 0/1 | 0 | ***[PBFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI1CSIN | Input | FTU1 | 0/1 | 0 | ***[PBFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| PB6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI1CS1 | Output | FTU1 | 0/1 | 1 | ***[PBFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| PB7 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | INT16 | Input | FTU4 | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |

Note1: During the reset period by the reset pin (RESET_N), the state of the BOOT_N pin can be input to PB0 with pull-up enabled and input enabled.

## 4.2.4. PORT C

**Table 4.8 Port C Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PCDATA]* | *[PCCR]* | *[PCFRn]* | *[PCOD]* | *[PCPUP]* | *[PCPDN]* | *[PCIE]* |
| PC0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT00 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | I2C0SCL | I/O | FTU1 | 0/1 | 1 | ***[PCFR1]*** | 1 | 0/1 | 0/1 | 1 |
| | EI2C0SCL | I/O | FTU12 | 0/1 | 1 | ***[PCFR2]*** | 1 | 0/1 | 0/1 | 1 |
| | T32A02OUTA | Output | FTU1 | 0/1 | 1 | ***[PCFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A02OUTC | Output | FTU1 | 0/1 | 1 | ***[PCFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | DCOM3 | Output | FTU1 | 0/1 | 1 | ***[PCFR6]*** | 0 | 0 | 0 | 0 |
| PC1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT01 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | I2C0SDA | I/O | FTU1 | 0/1 | 1 | ***[PCFR1]*** | 1 | 0/1 | 0/1 | 1 |
| | EI2C0SDA | I/O | FTU12 | 0/1 | 1 | ***[PCFR2]*** | 1 | 0/1 | 0/1 | 1 |
| | T32A02INA0 | Input | FTU1 | 0/1 | 0 | ***[PCFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A02INC0 | Input | FTU1 | 0/1 | 0 | ***[PCFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | DCOM2 | Output | FTU1 | 0/1 | 1 | ***[PCFR6]*** | 0 | 0 | 0 | 0 |
| PC2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT02 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT4TXDB | Output | FTU1 | 0/1 | 1 | ***[PCFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A02INA1 | Input | FTU1 | 0/1 | 0 | ***[PCFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A02INC1 | Input | FTU1 | 0/1 | 0 | ***[PCFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | RTCOUT | Output | FTU1 | 0/1 | 1 | ***[PCFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | DCOM1 | Output | FTU1 | 0/1 | 1 | ***[PCFR6]*** | 0 | 0 | 0 | 0 |
| PC3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT4TXDA | Output | FTU1 | 0/1 | 1 | ***[PCFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT4RXD | Input | FTU1 | 0/1 | 0 | ***[PCFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A02OUTB | Output | FTU1 | 0/1 | 1 | ***[PCFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | DCOM0 | Output | FTU1 | 0/1 | 1 | ***[PCFR6]*** | 0 | 0 | 0 | 0 |
| PC4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT4RXD | Input | FTU1 | 0/1 | 0 | ***[PCFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT4TXDA | Output | FTU1 | 0/1 | 1 | ***[PCFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A02INB0 | Input | FTU1 | 0/1 | 0 | ***[PCFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG39 | Output | FTU1 | 0/1 | 1 | ***[PCFR6]*** | 0 | 0 | 0 | 0 |
| PC5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT4CTS_N | Input | FTU1 | 0/1 | 0 | ***[PCFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT4RTS_N | Output | FTU1 | 0/1 | 1 | ***[PCFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A02INB1 | Input | FTU1 | 0/1 | 0 | ***[PCFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG38 | Output | FTU1 | 0/1 | 1 | ***[PCFR6]*** | 0 | 0 | 0 | 0 |
| PC6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT4RTS_N | Output | FTU1 | 0/1 | 1 | ***[PCFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT4CTS_N | Input | FTU1 | 0/1 | 0 | ***[PCFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG37 | Output | FTU1 | 0/1 | 1 | ***[PCFR6]*** | 0 | 0 | 0 | 0 |

### 4.2.5. PORT D

**Table 4.9 Port D Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PDDATA]* | *[PDCR]* | *[PDFRn]* | *[PDOD]* | *[PDPUP]* | *[PDPDN]* | *[PDIE]* |
| PD0 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA00 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PD1 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA01 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PD2 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA02 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PD3 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA03 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PD4 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA19 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PD5 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA20 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |

Note: When using analog input (AINAx), ***[PDCR]*** should be output disable "0",***[PDIE]*** should be input disable "0" , ***[PDPUP]*** should be pull-up disable "0" and ***[PDPDN]*** should be pull-down disable "0".

### 4.2.6. PORT E

**Table 4.10 Port E Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PEDATA]* | *[PECR]* | *[PEFRn]* | *[PEOD]* | *[PEPUP]* | *[PEPDN]* | *[PEIE]* |
| PE0 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA04 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PE1 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA05 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PE2 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA06 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PE3 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA07 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PE4 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA08 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PE5 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA09 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PE6 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA10 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |

Note: When using analog input (AINAx), ***[PECR]*** should be output disable "0",***[PEIE]*** should be input disable "0", ***[PEPUP]*** should be pull-up disable"0" and ***[PEPDN]*** should be pull-down disable "0".

## 4.2.7. PORT F

**Table 4.11 Port F Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PFDATA]* | *[PFCR]* | *[PFFRn]* | *[PFOD]* | *[PFPUP]* | *[PFPDN]* | *[PFIE]* |
| PF0 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA11 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PF1 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA12 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PF2 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | INT33 | Input | FTU4 | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | AINA13 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PF3 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | INT32 | Input | FTU4 | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | AINA14 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PF4 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA15 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PF5 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA16 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PF6 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA17 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PF7 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | AINA18 (Note) | Input | FTU5 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |

Note: When using analog input (AINAx), ***[PFCR]*** should be output disable "0",***[PFIE]*** should be input disable "0" , ***[PFPUP]*** should be pull-up disable "0" and ***[PFPDN]*** should be pull-down disable "0".

## 4.2.8. PORT G

**Table 4.12 Port G Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PGDATA]* | *[PGCR]* | *[PGFRn]* | *[PGOD]* | *[PGPUP]* | *[PGPDN]* | *[PGIE]* |
| PG0 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | DAC0 (Note) | Output | FTU13 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PG1 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | DAC1 (Note) | Output | FTU13 | 0/1 | 0 | N/A | 0/1 | 0 | 0 | 0 |
| PG2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT27 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT3RXD | Input | FTU1 | 0/1 | 0 | ***[PGFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT3TXDA | Output | FTU1 | 0/1 | 1 | ***[PGFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A07OUTA | Output | FTU1 | 0/1 | 1 | ***[PGFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A07OUTC | Output | FTU1 | 0/1 | 1 | ***[PGFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| PG3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT28 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT3TXDA | Output | FTU1 | 0/1 | 1 | ***[PGFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT3RXD | Input | FTU1 | 0/1 | 0 | ***[PGFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A07INA0 | Input | FTU1 | 0/1 | 0 | ***[PGFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A07INC0 | Input | FTU1 | 0/1 | 0 | ***[PGFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PG4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT3TXDB | Output | FTU1 | 0/1 | 1 | ***[PGFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A07INA1 | Input | FTU1 | 0/1 | 0 | ***[PGFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A07INC1 | Input | FTU1 | 0/1 | 0 | ***[PGFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PG5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A07OUTB | Output | FTU1 | 0/1 | 1 | ***[PGFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| PG6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A07INB0 | Input | FTU1 | 0/1 | 0 | ***[PGFR3]*** | 0 | 0/1 | 0/1 | 1 |
| PG7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A07INB1 | Input | FTU1 | 0/1 | 0 | ***[PGFR3]*** | 0/1 | 0/1 | 0/1 | 1 |

Note: When using analog output (DACx), ***[PGCR]*** should be output disable "0",***[PGIE]*** should be input disable "0" , ***[PGPUP]*** should be pull-up disable "0" and ***[PGPDN]*** should be pull-down disable "0".

## 4.2.9. PORT H

**Table 4.13 Port H Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PHDATA]* | *[PHCR]* | *[PHFRn]* | *[PHOD]* | *[PHPUP]* | *[PHPDN]* | *[PHIE]* |
| PH0 | After reset | | | 0 | N/A | N/A | N/A | N/A | 0 | 0 |
| | Input Port | Input | | 0/1 | N/A | N/A | N/A | N/A | 0/1 | 1 |
| | X1 | Input | FTU10 | 0/1 | N/A | N/A | N/A | N/A | 0 | 0 |
| | EHCLKIN | Input | FTU10 | 0/1 | N/A | N/A | N/A | N/A | 0 | 0/1 |
| PH1 | After reset | | | 0 | N/A | N/A | N/A | N/A | 0 | 0 |
| | Input Port | Input | | 0/1 | N/A | N/A | N/A | N/A | 0/1 | 1 |
| | X2 | Output | FTU10 | 0/1 | N/A | N/A | N/A | N/A | 0 | 0 |
| PH2 | After reset | | | 0 | N/A | N/A | N/A | N/A | 0 | 0 |
| | Input Port | Input | | 0/1 | N/A | N/A | N/A | N/A | 0/1 | 1 |
| | XT1 | Input | FTU11 | 0/1 | N/A | N/A | N/A | N/A | 0 | 0 |
| PH3 | After reset | | | 0 | N/A | N/A | N/A | N/A | 0 | 0 |
| | Input Port | Input | | 0/1 | N/A | N/A | N/A | N/A | 0/1 | 1 |
| | XT2 | Output | FTU11 | 0/1 | N/A | N/A | N/A | N/A | 0 | 0 |
| | INT06 | Input | FTU11 | 0/1 | N/A | N/A | N/A | N/A | 0/1 | 1 |
| PH4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT19 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI4SCK | Input | FTU1 | 0/1 | 0 | ***[PHFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| PH5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT20 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI4TXD | Output | FTU2 | 0/1 | 1 | ***[PHFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| PH6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT21 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI4RXD | Input | FTU1 | 0/1 | 0 | ***[PHFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| PH7 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | INT22 | Input | FTU4 | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |

## 4.2.10. PORT J

**Table 4.14 Port J Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PJDATA]* | *[PJCR]* | *[PJFRn]* | *[PJOD]* | *[PJPUP]* | *[PJPDN]* | *[PJIE]* |
| PJ0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1TXDB | Output | FTU1 | 0/1 | 1 | ***[PJFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A03OUTA | Output | FTU1 | 0/1 | 1 | ***[PJFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A03OUTC | Output | FTU1 | 0/1 | 1 | ***[PJFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UO0 | Output | FTU2 | 0/1 | 1 | ***[PJFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG22 | Output | FTU1 | 0/1 | 1 | ***[PJFR6]*** | 0 | 0 | 0 | 0 |
| PJ1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1TXDA | Output | FTU1 | 0/1 | 1 | ***[PJFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT1RXD | Input | FTU1 | 0/1 | 0 | ***[PJFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A03INA0 | Input | FTU1 | 0/1 | 0 | ***[PJFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A03INC0 | Input | FTU1 | 0/1 | 0 | ***[PJFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | XO0 | Output | FTU2 | 0/1 | 1 | ***[PJFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG21 | Output | FTU1 | 0/1 | 1 | ***[PJFR6]*** | 0 | 0 | 0 | 0 |
| PJ2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1RXD | Input | FTU1 | 0/1 | 0 | ***[PJFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT1TXDA | Output | FTU1 | 0/1 | 1 | ***[PJFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A03INA1 | Input | FTU1 | 0/1 | 0 | ***[PJFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A03INC1 | Input | FTU1 | 0/1 | 0 | ***[PJFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | VO0 | Output | FTU2 | 0/1 | 1 | ***[PJFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG20 | Output | FTU1 | 0/1 | 1 | ***[PJFR6]*** | 0 | 0 | 0 | 0 |
| PJ3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1CTS_N | Input | FTU1 | 0/1 | 0 | ***[PJFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT1RTS_N | Output | FTU1 | 0/1 | 1 | ***[PJFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A03OUTB | Output | FTU1 | 0/1 | 1 | ***[PJFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | YO0 | Output | FTU2 | 0/1 | 1 | ***[PJFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG19 | Output | FTU1 | 0/1 | 1 | ***[PJFR6]*** | 0 | 0 | 0 | 0 |
| PJ4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT04 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT1RTS_N | Output | FTU1 | 0/1 | 1 | ***[PJFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT1CTS_N | Input | FTU1 | 0/1 | 0 | ***[PJFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A03INB0 | Input | FTU1 | 0/1 | 0 | ***[PJFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | WO0 | Output | FTU2 | 0/1 | 1 | ***[PJFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG18 | Output | FTU1 | 0/1 | 1 | ***[PJFR6]*** | 0 | 0 | 0 | 0 |
| PJ5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A03INB1 | Input | FTU1 | 0/1 | 0 | ***[PJFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | ZO0 | Output | FTU2 | 0/1 | 1 | ***[PJFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG17 | Output | FTU1 | 0/1 | 1 | ***[PJFR6]*** | 0 | 0 | 0 | 0 |

## 4.2.11. PORT K

**Table 4.15 Port K Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PKDATA]* | *[PKCR]* | *[PKFRn]* | *[PKOD]* | *[PKPUP]* | *[PKPDN]* | *[PKIE]* |
| PK0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1TXDB | Output | FTU1 | 0/1 | 1 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | EMG0 | Input | FTU1 | 0/1 | 0 | ***[PKFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG16 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |
| PK1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT05 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT1TXDA | Output | FTU1 | 0/1 | 1 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT1RXD | Input | FTU1 | 0/1 | 0 | ***[PKFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | OVV0 | Input | FTU1 | 0/1 | 0 | ***[PKFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG15 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |
| PK2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1RXD | Input | FTU1 | 0/1 | 0 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT1TXDA | Output | FTU1 | 0/1 | 1 | ***[PKFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A04OUTA | Output | FTU1 | 0/1 | 1 | ***[PKFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A04OUTC | Output | FTU1 | 0/1 | 1 | ***[PKFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG14 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |
| PK3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1CTS_N | Input | FTU1 | 0/1 | 0 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT1RTS_N | Output | FTU1 | 0/1 | 1 | ***[PKFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A04INA0 | Input | FTU1 | 0/1 | 0 | ***[PKFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A04INC0 | Input | FTU1 | 0/1 | 0 | ***[PKFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG13 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |
| PK4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT1RTS_N | Output | FTU1 | 0/1 | 1 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT1CTS_N | Input | FTU1 | 0/1 | 0 | ***[PKFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A04INA1 | Input | FTU1 | 0/1 | 0 | ***[PKFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A04INC1 | Input | FTU1 | 0/1 | 0 | ***[PKFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG12 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |
| PK5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT6RXD | Input | FTU1 | 0/1 | 0 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT6TXDA | Output | FTU1 | 0/1 | 1 | ***[PKFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A04OUTB | Output | FTU1 | 0/1 | 1 | ***[PKFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG11 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |
| PK6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT6TXDA | Output | FTU1 | 0/1 | 1 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT6RXD | Input | FTU1 | 0/1 | 0 | ***[PKFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A04INB0 | Input | FTU1 | 0/1 | 0 | ***[PKFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG10 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PKDATA]* | *[PKCR]* | *[PKFRn]* | *[PKOD]* | *[PKPUP]* | *[PKPDN]* | *[PKIE]* |
| PK7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT13 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT6TXDB | Output | FTU1 | 0/1 | 1 | ***[PKFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A04INB1 | Input | FTU1 | 0/1 | 0 | ***[PKFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG09 | Output | FTU1 | 0/1 | 1 | ***[PKFR6]*** | 0 | 0 | 0 | 0 |

## 4.2.12. PORT L

**Table 4.16 Port L Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PLDATA]* | *[PLCR]* | *[PLFRn]* | *[PLOD]* | *[PLPUP]* | *[PLPDN]* | *[PLIE]* |
| PL0 | After reset (TRST_N) | Input | FTU3 (Note2) | 0 | 0 | ***[PLFR5]*** | 0 | 1 | 0 | 1 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT2TXDA | Output | FTU1 | 0/1 | 1 | ***[PLFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT2RXD | Input | FTU1 | 0/1 | 0 | ***[PLFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | I2C2SCL | I/O | FTU1 | 0/1 | 1 | ***[PLFR3]*** | 1 | 0/1 | 0/1 | 1 |
| | EI2C2SCL | I/O | FTU12 | 0/1 | 1 | ***[PLFR4]*** | 1 | 0/1 | 0/1 | 1 |
| PL1 | After reset (TDI) | Input | FTU1 | 0 | 0 | ***[PLFR5]*** | 0 | 1 | 0 | 1 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT2RXD | Input | FTU1 | 0/1 | 0 | ***[PLFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT2TXDA | Output | FTU1 | 0/1 | 1 | ***[PLFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | I2C2SDA | I/O | FTU1 | 0/1 | 1 | ***[PLFR3]*** | 1 | 0/1 | 0/1 | 1 |
| | EI2C2SDA | I/O | FTU12 | 0/1 | 1 | ***[PLFR4]*** | 1 | 0/1 | 0/1 | 1 |
| PL2 | After reset (TDO/SWV) | Output | FTU2 | 0 | 1(Note) | ***[PLFR5]*** | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT2CTS_N | Input | FTU1 | 0/1 | 0 | ***[PLFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT2RTS_N | Output | FTU1 | 0/1 | 1 | ***[PLFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06OUTB | Output | FTU1 | 0/1 | 1 | ***[PLFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| PL3 | After reset (TCK/SWCLK) | Input | FTU1 | 0 | 0 | ***[PLFR5]*** | 0 | 0 | 1 | 1 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT08 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT2RTS_N | Output | FTU1 | 0/1 | 1 | ***[PLFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT2CTS_N | Input | FTU1 | 0/1 | 0 | ***[PLFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INB0 | Input | FTU1 | 0/1 | 0 | ***[PLFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| PL4 | After reset (TMS/SWDIO) | I/O | FTU2 | 0 | 1(Note) | ***[PLFR5]*** | 0 | 1 | 0 | 1 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT12 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INB1 | Input | FTU1 | 0/1 | 0 | ***[PLFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| PL5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06OUTA | Output | FTU1 | 0/1 | 1 | ***[PLFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06OUTC | Output | FTU1 | 0/1 | 1 | ***[PLFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| PL6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06INA0 | Input | FTU1 | 0/1 | 0 | ***[PLFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INC0 | Input | FTU1 | 0/1 | 0 | ***[PLFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PL7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06INA1 | Input | FTU1 | 0/1 | 0 | ***[PLFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INC1 | Input | FTU1 | 0/1 | 0 | ***[PLFR4]*** | 0/1 | 0/1 | 0/1 | 1 |

Note1: When receive the command from TOOL, it becomes output

Note2: TXZ+ Family TMPM3H Group(1) products don't have the Noise filter.

## 4.2.13. PORT M

**Table 4.17 Port M Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PMDATA]* | *[PMCR]* | *[PMFRn]* | *[PMOD]* | *[PMPUP]* | *[PMPDN]* | *[PMIE]* |
| PM0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0TXDB | Output | FTU1 | 0/1 | 1 | ***[PMFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0SCK | Input | FTU1 | 0/1 | 0 | ***[PMFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | FTU1 | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTA | Output | FTU1 | 0/1 | 1 | ***[PMFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTC | Output | FTU1 | 0/1 | 1 | ***[PMFR5]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TRACECLK | Output | FTU1 | 0/1 | 1 | ***[PMFR6]*** | 0/1 | 0/1 | 0/1 | 0 |
| PM1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0TXDA | Output | FTU1 | 0/1 | 1 | ***[PMFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT0RXD | Input | FTU1 | 0/1 | 0 | ***[PMFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI0TXD | Output | FTU2 | 0/1 | 1 | ***[PMFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00INA0 | Input | FTU1 | 0/1 | 0 | ***[PMFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A00INC0 | Input | FTU1 | 0/1 | 0 | ***[PMFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TRACEDATA0 | Output | FTU1 | 0/1 | 1 | ***[PMFR6]*** | 0/1 | 0/1 | 0/1 | 0 |
| PM2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT09 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT0RXD | Input | FTU1 | 0/1 | 0 | ***[PMFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT0TXDA | Output | FTU1 | 0/1 | 1 | ***[PMFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0RXD | Input | FTU1 | 0/1 | 0 | ***[PMFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A00INA1 | Input | FTU1 | 0/1 | 0 | ***[PMFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A00INC1 | Input | FTU1 | 0/1 | 0 | ***[PMFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TRACEDATA1 | Output | FTU1 | 0/1 | 1 | ***[PMFR6]*** | 0/1 | 0/1 | 0/1 | 0 |
| PM3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0CTS_N | Input | FTU1 | 0/1 | 0 | ***[PMFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT0RTS_N | Output | FTU1 | 0/1 | 1 | ***[PMFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0CS0 | Output | FTU1 | 0/1 | 1 | ***[PMFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00OUTB | Output | FTU1 | 0/1 | 1 | ***[PMFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI0CSIN | Input | FTU1 | 0/1 | 0 | ***[PMFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TRACEDATA2 | Output | FTU1 | 0/1 | 1 | ***[PMFR6]*** | 0/1 | 0/1 | 0/1 | 0 |
| PM4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT0RTS_N | Output | FTU1 | 0/1 | 1 | ***[PMFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT0CTS_N | Input | FTU1 | 0/1 | 0 | ***[PMFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI0CS1 | Output | FTU1 | 0/1 | 1 | ***[PMFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00INB0 | Input | FTU1 | 0/1 | 0 | ***[PMFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | TRACEDATA3 | Output | FTU1 | 0/1 | 1 | ***[PMFR6]*** | 0/1 | 0/1 | 0/1 | 0 |
| PM5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A00INB1 | Input | FTU1 | 0/1 | 0 | ***[PMFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PM6 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | INT15 | Input | FTU4 | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| PM7 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |

## 4.2.14. PORT N

**Table 4.18 Port N Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PNDATA]* | *[PNCR]* | *[PNFRn]* | *[PNOD]* | *[PNPUP]* | *[PNPDN]* | *[PNIE]* |
| PN0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT5RTS_N | Output | FTU1 | 0/1 | 1 | ***[PNFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT5CTS_N | Input | FTU1 | 0/1 | 0 | ***[PNFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A05OUTA | Output | FTU1 | 0/1 | 1 | ***[PNFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A05OUTC | Output | FTU1 | 0/1 | 1 | ***[PNFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG23 | Output | FTU1 | 0/1 | 1 | ***[PNFR6]*** | 0 | 0 | 0 | 0 |
| PN1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT5CTS_N | Input | FTU1 | 0/1 | 0 | ***[PNFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT5RTS_N | Output | FTU1 | 0/1 | 1 | ***[PNFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A05INA0 | Input | FTU1 | 0/1 | 0 | ***[PNFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A05INC0 | Input | FTU1 | 0/1 | 0 | ***[PNFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG24 | Output | FTU1 | 0/1 | 1 | ***[PNFR6]*** | 0 | 0 | 0 | 0 |
| PN2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT5RXD | Input | FTU1 | 0/1 | 0 | ***[PNFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT5TXDA | Output | FTU1 | 0/1 | 1 | ***[PNFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A05INA1 | Input | FTU1 | 0/1 | 0 | ***[PNFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A05INC1 | Input | FTU1 | 0/1 | 0 | ***[PNFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG25 | Output | FTU1 | 0/1 | 1 | ***[PNFR6]*** | 0 | 0 | 0 | 0 |
| PN3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT10 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | UT5TXDA | Output | FTU1 | 0/1 | 1 | ***[PNFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT5RXD | Input | FTU1 | 0/1 | 0 | ***[PNFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A05OUTB | Output | FTU1 | 0/1 | 1 | ***[PNFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TRGIN2 | Input | FTU1 | 0/1 | 0 | ***[PNFR5]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG26 | Output | FTU1 | 0/1 | 1 | ***[PNFR6]*** | 0 | 0 | 0 | 0 |
| PN4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT5TXDB | Output | FTU1 | 0/1 | 1 | ***[PNFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A05INB0 | Input | FTU1 | 0/1 | 0 | ***[PNFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG27 | Output | FTU1 | 0/1 | 1 | ***[PNFR6]*** | 0 | 0 | 0 | 0 |
| PN5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A05INB1 | Input | FTU1 | 0/1 | 0 | ***[PNFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG28 | Output | FTU1 | 0/1 | 1 | ***[PNFR6]*** | 0 | 0 | 0 | 0 |

## 4.2.15. PORT P

**Table 4.19 Port P Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PPDATA]* | *[PPCR]* | *[PPFRn]* | *[PPOD]* | *[PPPUP]* | *[PPPDN]* | *[PPIE]* |
| PP0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI2SCK | Input | FTU1 | 0/1 | 0 | ***[PPFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| | T32A01OUTA | Output | FTU1 | 0/1 | 1 | ***[PPFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A01OUTC | Output | FTU1 | 0/1 | 1 | ***[PPFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| PP1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI2TXD | Output | FTU2 | 0/1 | 1 | ***[PPFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A01INA0 | Input | FTU1 | 0/1 | 0 | ***[PPFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A01INC0 | Input | FTU1 | 0/1 | 0 | ***[PPFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PP2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI2RXD | Input | FTU1 | 0/1 | 0 | ***[PPFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A01INA1 | Input | FTU1 | 0/1 | 0 | ***[PPFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A01INC1 | Input | FTU1 | 0/1 | 0 | ***[PPFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PP3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT14 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI3RXD | Input | FTU1 | 0/1 | 0 | ***[PPFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG08 | Output | FTU1 | 0/1 | 1 | ***[PPFR6]*** | 0 | 0 | 0 | 0 |
| PP4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI3TXD | Output | FTU2 | 0/1 | 1 | ***[PPFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG07 | Output | FTU1 | 0/1 | 1 | ***[PPFR6]*** | 0 | 0 | 0 | 0 |
| PP5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI3SCK | Input | FTU1 | 0/1 | 0 | ***[PPFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| | SEG06 | Output | FTU1 | 0/1 | 1 | ***[PPFR6]*** | 0 | 0 | 0 | 0 |
| PP6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI3CS0 | Output | FTU1 | 0/1 | 1 | ***[PPFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI3CSIN | Input | FTU1 | 0/1 | 0 | ***[PPFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | PMD0DBG | Output | FTU1 | 0/1 | 1 | ***[PPFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG05 | Output | FTU1 | 0/1 | 1 | ***[PPFR6]*** | 0 | 0 | 0 | 0 |
| PP7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI3CS1 | Output | FTU1 | 0/1 | 1 | ***[PPFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG04 | Output | FTU1 | 0/1 | 1 | ***[PPFR6]*** | 0 | 0 | 0 | 0 |

## 4.2.16. PORT R

**Table 4.20 Port R Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PRDATA]* | *[PRCR]* | *[PRFRn]* | *[PROD]* | *[PRPUP]* | *[PRPDN]* | *[PRIE]* |
| PR0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT7RXD | Input | FTU1 | 0/1 | 0 | ***[PRFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT7TXDA | Output | FTU1 | 0/1 | 1 | ***[PRFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A02OUTA | Output | FTU1 | 0/1 | 1 | ***[PRFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A02OUTC | Output | FTU1 | 0/1 | 1 | ***[PRFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| | SEG36 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |
| PR1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT7TXDA | Output | FTU1 | 0/1 | 1 | ***[PRFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT7RXD | Input | FTU1 | 0/1 | 0 | ***[PRFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A02INA0 | Input | FTU1 | 0/1 | 0 | ***[PRFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A02INC0 | Input | FTU1 | 0/1 | 0 | ***[PRFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG35 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |
| PR2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT7TXDB | Output | FTU1 | 0/1 | 1 | ***[PRFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A02INA1 | Input | FTU1 | 0/1 | 0 | ***[PRFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A02INC1 | Input | FTU1 | 0/1 | 0 | ***[PRFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| | SEG34 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |
| PR3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | SEG33 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |
| PR4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | SEG32 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |
| PR5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | SEG31 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |
| PR6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | SEG30 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |
| PR7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | SEG29 | Output | FTU1 | 0/1 | 1 | ***[PRFR6]*** | 0 | 0 | 0 | 0 |

## 4.2.17. PORT T

**Table 4.21 Port T Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PTDATA]* | *[PTCR]* | *[PTFRn]* | *[PTOD]* | *[PTPUP]* | *[PTPDN]* | *[PTIE]* |
| PT0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT23 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | I2C3SDA | I/O | FTU1 | 0/1 | 1 | ***[PTFR1]*** | 1 | 0/1 | 0/1 | 1 |
| | TSPI2CS1 | Output | FTU1 | 0/1 | 1 | ***[PTFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | EI2C3SDA | I/O | FTU12 | 0/1 | 1 | ***[PTFR4]*** | 1 | 0/1 | 0/1 | 1 |
| PT1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT24 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | I2C3SCL | I/O | FTU1 | 0/1 | 1 | ***[PTFR1]*** | 1 | 0/1 | 0/1 | 1 |
| | TSPI2CS0 | Output | FTU1 | 0/1 | 1 | ***[PTFR2]*** | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI2CSIN | Input | FTU1 | 0/1 | 0 | ***[PTFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | EI2C3SCL | I/O | FTU12 | 0/1 | 1 | ***[PTFR4]*** | 1 | 0/1 | 0/1 | 1 |
| PT2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT25 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI2SCK | Input | FTU1 | 0/1 | 0 | ***[PTFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | | Output | | 0/1 | 1 | | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06OUTB | Output | FTU1 | 0/1 | 1 | ***[PTFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| PT3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT26 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | TSPI2TXD | Output | FTU2 | 0/1 | 1 | ***[PTFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06INB0 | Input | FTU1 | 0/1 | 0 | ***[PTFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| PT4 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | TSPI2RXD | Input | FTU1 | 0/1 | 0 | ***[PTFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INB1 | Input | FTU1 | 0/1 | 0 | ***[PTFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| PT5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06OUTA | Output | FTU1 | 0/1 | 1 | ***[PTFR3]*** | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06OUTC | Output | FTU1 | 0/1 | 1 | ***[PTFR4]*** | 0/1 | 0/1 | 0/1 | 0 |
| PT6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | T32A06INA0 | Input | FTU1 | 0/1 | 0 | ***[PTFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INC0 | Input | FTU1 | 0/1 | 0 | ***[PTFR4]*** | 0/1 | 0/1 | 0/1 | 1 |
| PT7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT29 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INA1 | Input | FTU1 | 0/1 | 0 | ***[PTFR3]*** | 0/1 | 0/1 | 0/1 | 1 |
| | T32A06INC1 | Input | FTU1 | 0/1 | 0 | ***[PTFR4]*** | 0/1 | 0/1 | 0/1 | 1 |

## 4.2.18. PORT U

**Table 4.22 Port U Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PUDATA]* | *[PUCR]* | *[PUFRn]* | *[PUOD]* | *[PUPUP]* | *[PUPDN]* | *[PUIE]* |
| PU0 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | INT30 | Input | FTU4 | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| PU1 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| | INT31 | Input | FTU4 | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| PU2 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| PU3 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| PU4 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| PU5 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |

## 4.2.19. PORT V

**Table 4.23 Port V Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PVDATA]* | *[PVCR]* | *[PVFRn]* | *[PVOD]* | *[PVPUP]* | *[PVPDN]* | *[PVIE]* |
| PV0 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | SEG03 | Output | FTU1 | 0/1 | 1 | ***[PVFR6]*** | 0 | 0 | 0 | 0 |
| PV1 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | SEG02 | Output | FTU1 | 0/1 | 1 | ***[PVFR6]*** | 0 | 0 | 0 | 0 |
| PV2 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT17 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | SEG01 | Output | FTU1 | 0/1 | 1 | ***[PVFR6]*** | 0 | 0 | 0 | 0 |
| PV3 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | INT18 | Input | FTU4 | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | SEG00 | Output | FTU1 | 0/1 | 1 | ***[PVFR6]*** | 0 | 0 | 0 | 0 |
| PV4 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |
| PV5 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT4TXDB | Output | FTU1 | 0/1 | 1 | ***[PVFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| PV6 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT4TXDA | Output | FTU1 | 0/1 | 1 | ***[PVFR1]*** | 0/1 | 0/1 | 0/1 | 0 |
| | UT4RXD | Input | FTU1 | 0/1 | 0 | ***[PVFR2]*** | 0/1 | 0/1 | 0/1 | 1 |
| PV7 | After reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | 0 | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | 0 | 0/1 | 0/1 | 0/1 | 0 |
| | UT4RXD | Input | FTU1 | 0/1 | 0 | ***[PVFR1]*** | 0/1 | 0/1 | 0/1 | 1 |
| | UT4TXDA | Output | FTU1 | 0/1 | 1 | ***[PVFR2]*** | 0/1 | 0/1 | 0/1 | 0 |

## 4.2.20. PORT W

**Table 4.24 Port W Registers Setting**

| PORT | Reset status / Function | Input/output | PORT type | Control register | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | *[PWDATA]* | *[PWCR]* | *[PWFRn]* | *[PWOD]* | *[PWPUP]* | *[PWPDN]* | *[PWIE]* |
| PW0 | After reset | | | 0 | 0 | N/A | 0 | 0 | 0 | 0 |
| | Input Port | Input | | 0/1 | 0 | N/A | 0/1 | 0/1 | 0/1 | 1 |
| | Output Port | Output | | 0/1 | 1 | N/A | 0/1 | 0/1 | 0/1 | 0 |

# 5. Block Diagrams of Ports

The port has nine types of circuits, FTU1 to FTU6 and FTU10 to FTU13. Each circuit diagram is shown in the following page and after. The dot line block shows an equivalent circuit which is described in "Datasheet".

The "I/O Reset" shown in the circuit diagram is described the power on reset (POR) or the reset pin (RESET_N). Although, "I/O Reset" of debug pins (TMS/SWDIO, TDI, TDO/SWV, TCK/SWCLK, TRST_N) is the power on reset (POR) only.

## 5.1. Type FTU1

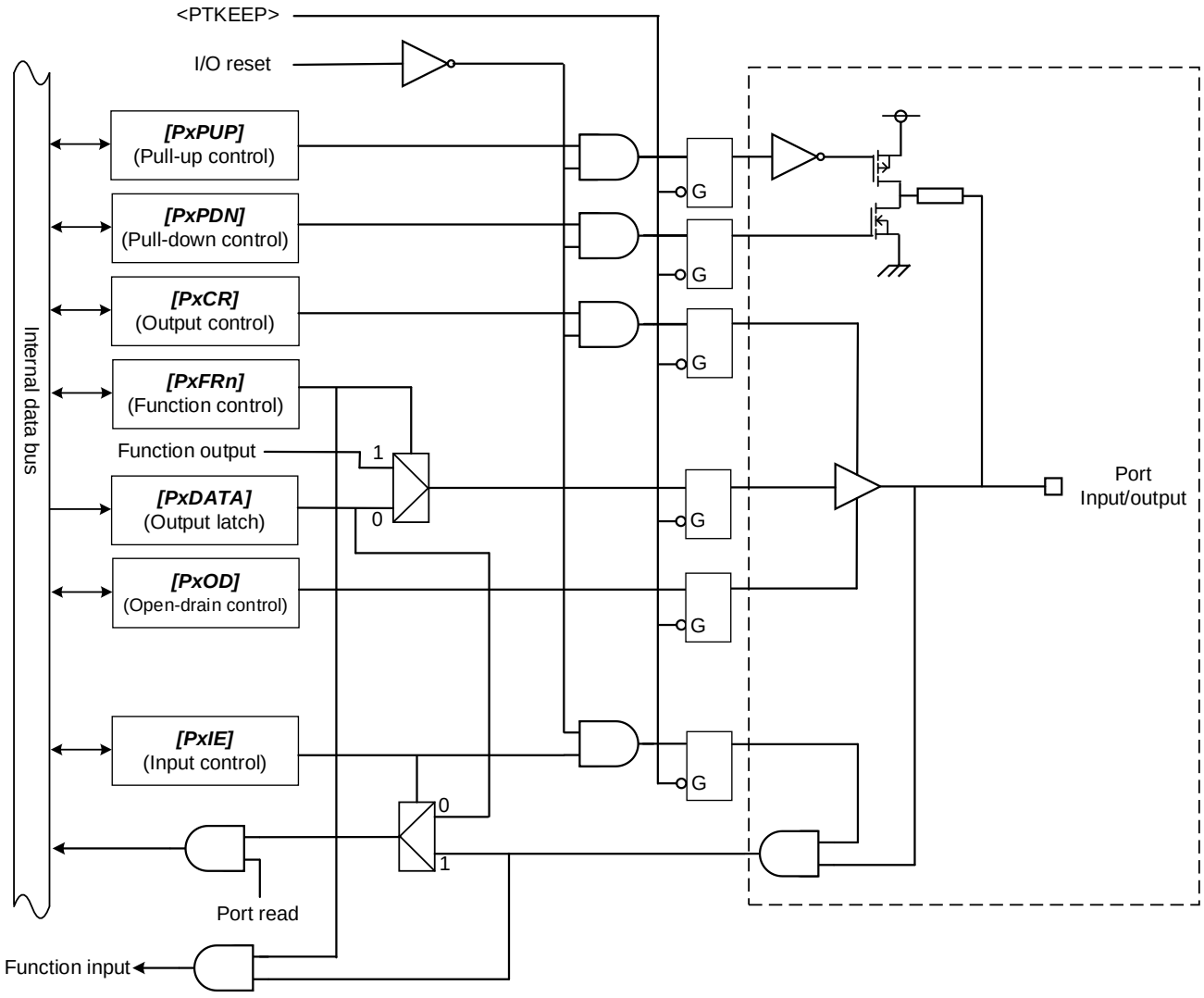



**Figure 5.1 Port Type FTU1**

Note: ***[PxIE]*** is not available on PB0 pin.

## 5.2. Type FTU2

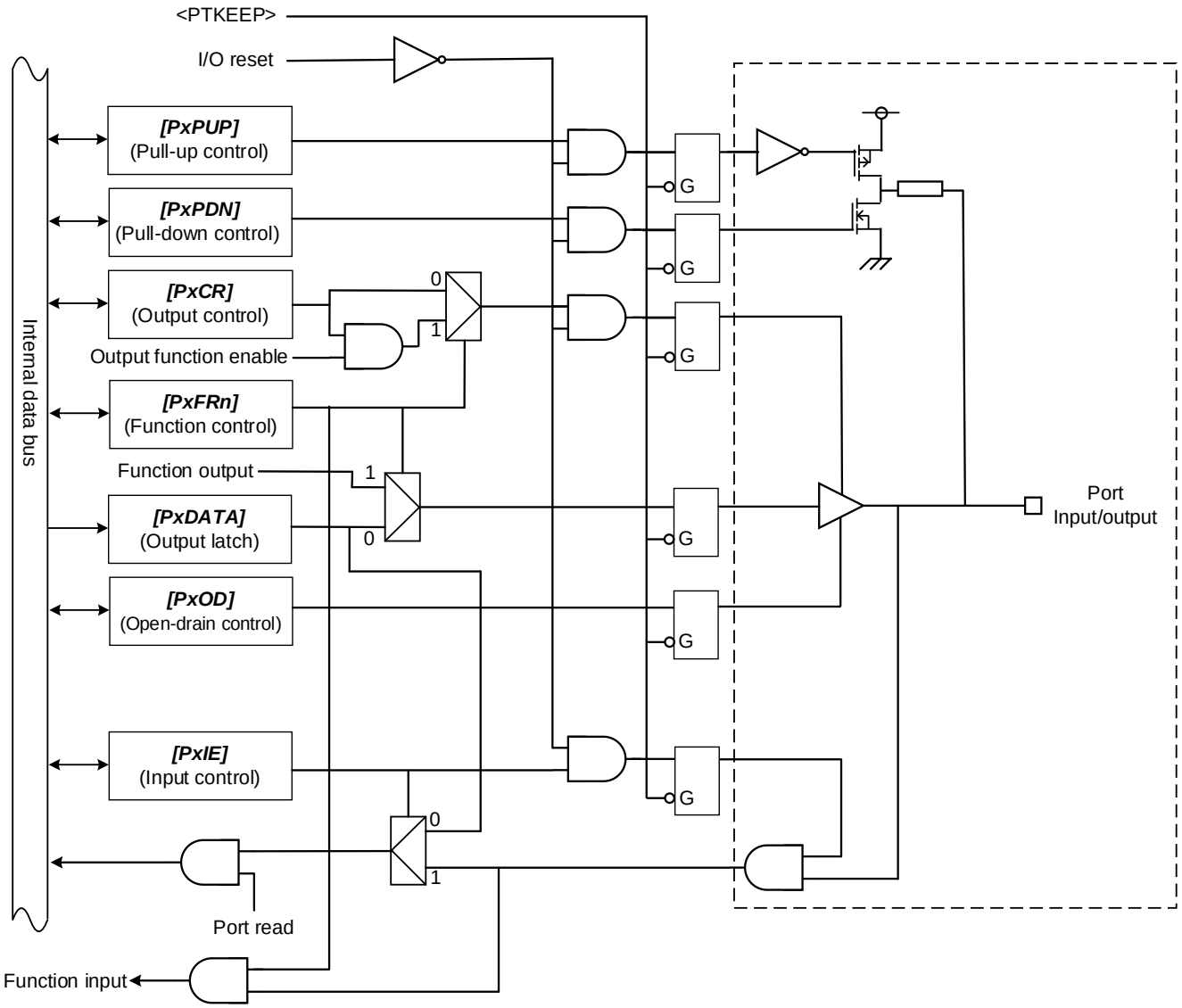



**Figure 5.2 Port Type FTU2**

## 5.3. Type FTU3

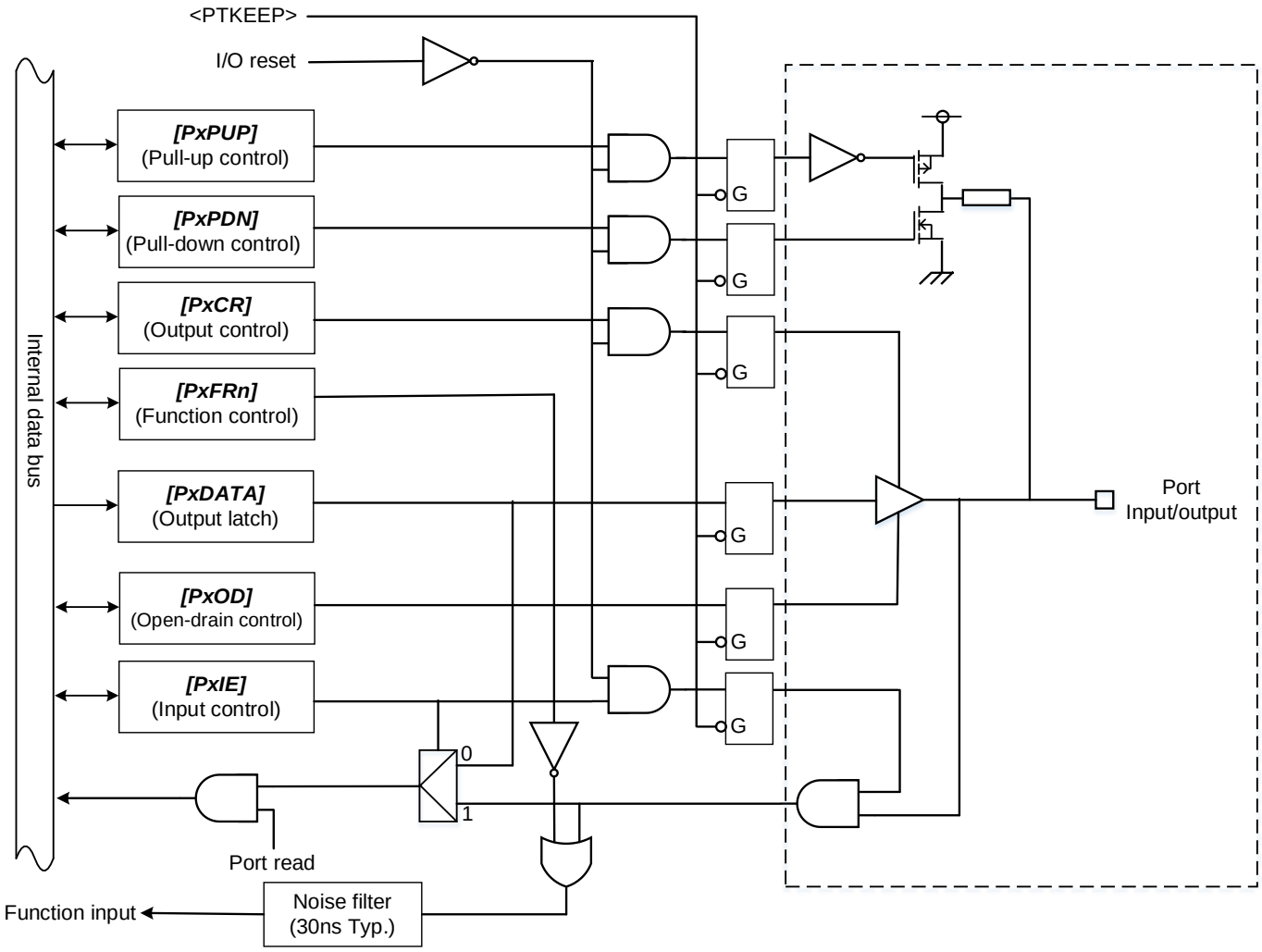



**Figure 5.3 Port Type FTU3**

## 5.4. Type FTU4

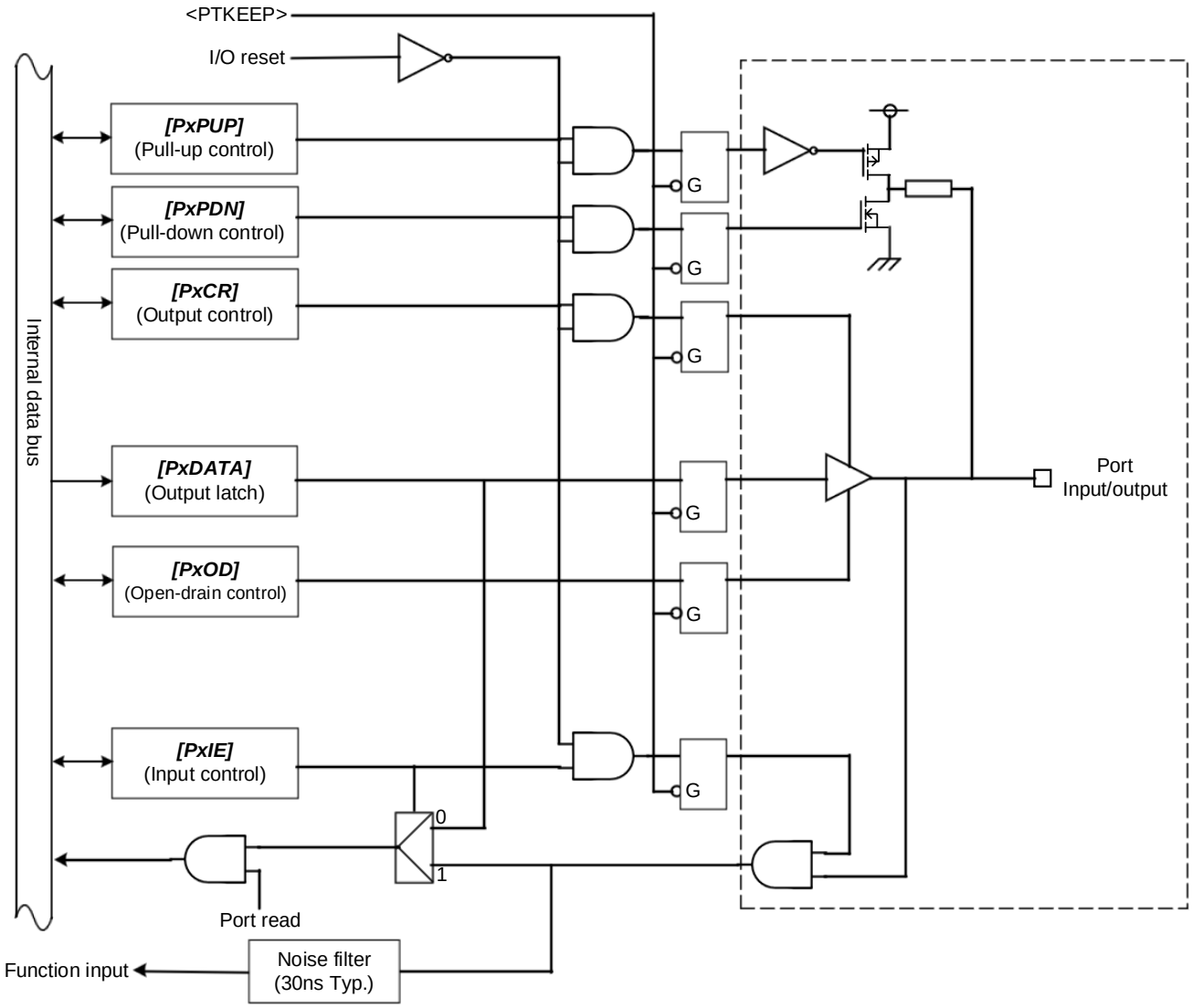



**Figure 5.4 Port Type FTU4**

## 5.5. Type FTU5

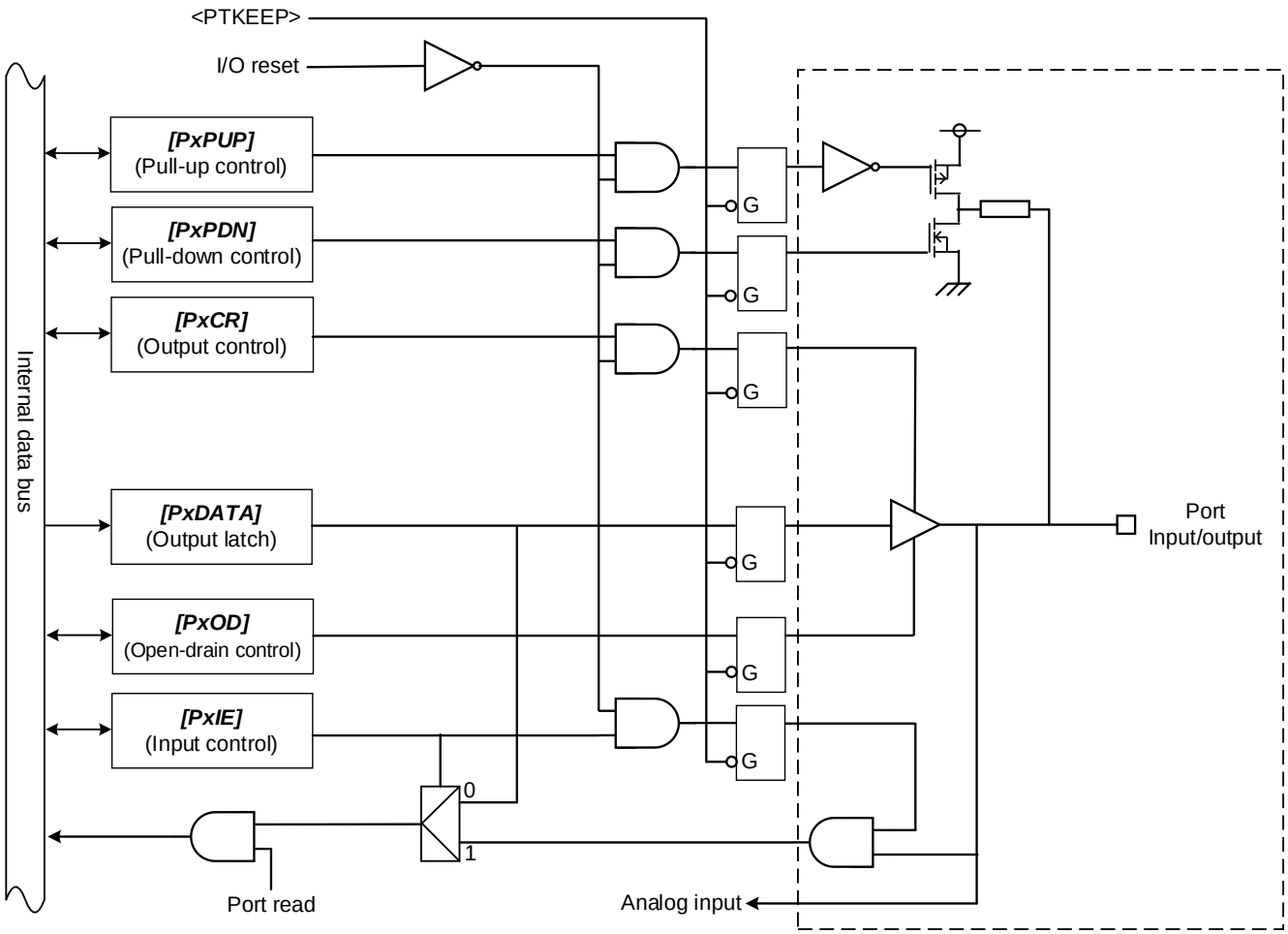



**Figure 5.5 Port Type FTU5**

## 5.6. Type FTU6

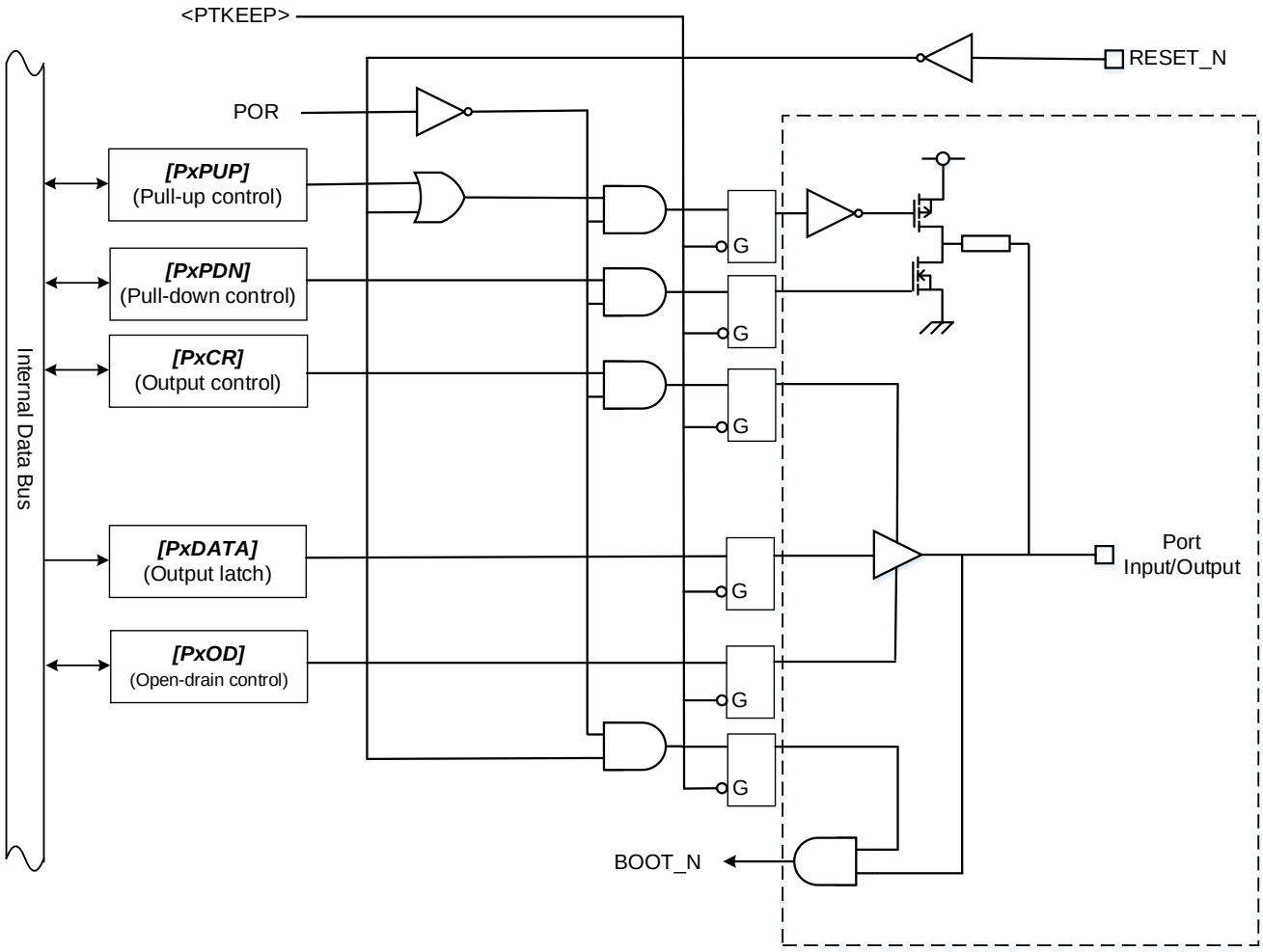



**Figure 5.6 Port Type FTU6**

## 5.7. Type FTU10

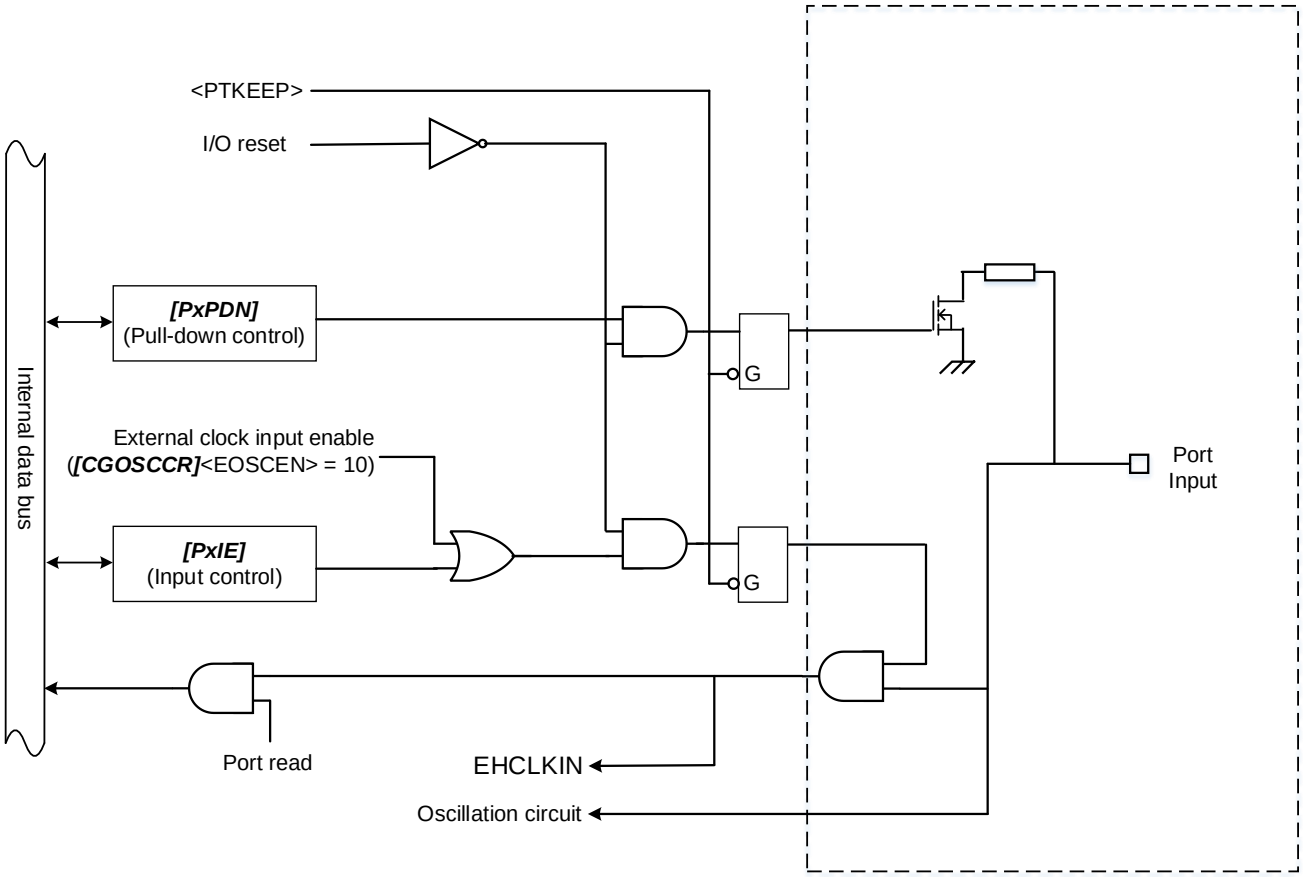



**Figure 5.7 Port Type FTU10**

## 5.8. Type FTU11

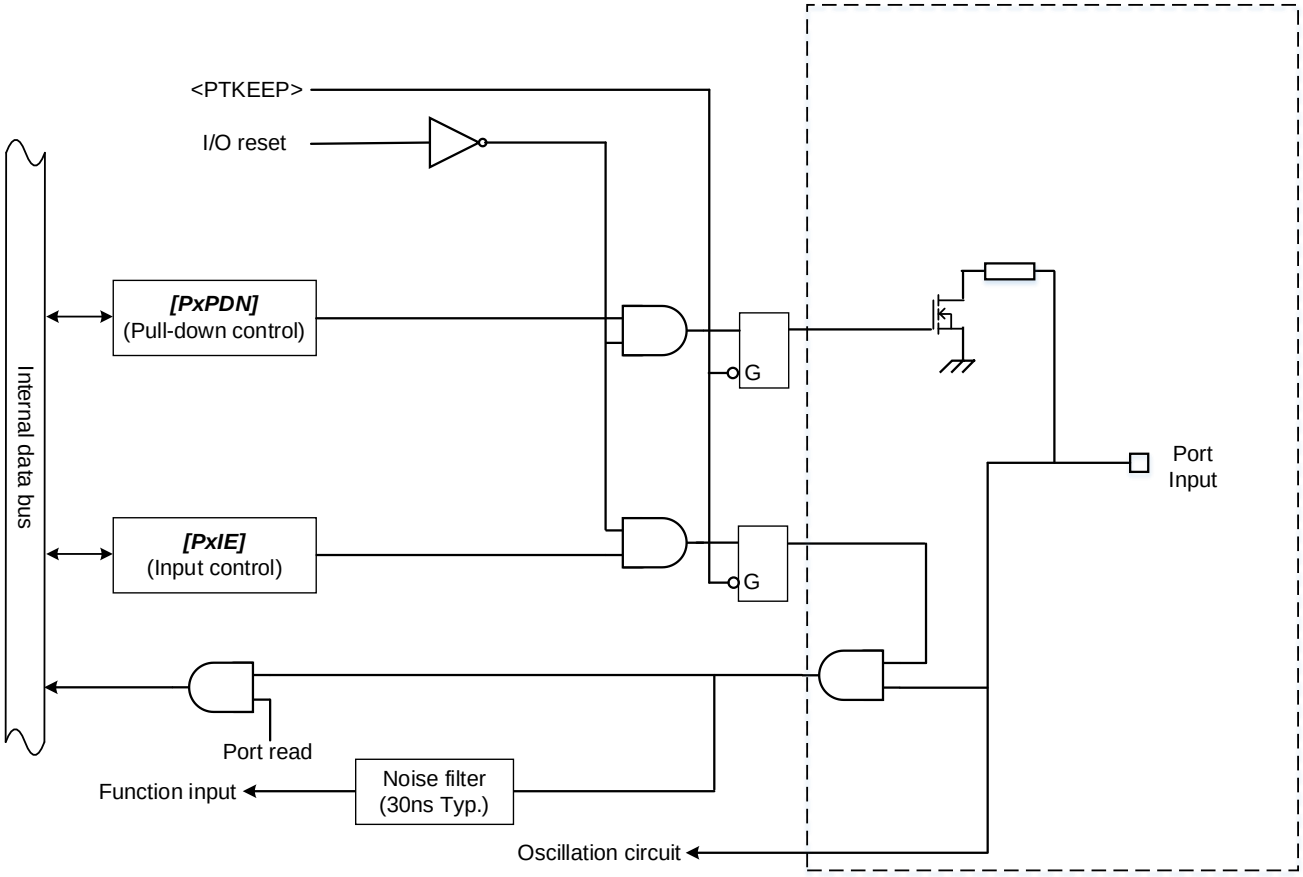



**Figure 5.8 Port Type FTU11**

## 5.9. Type FTU12

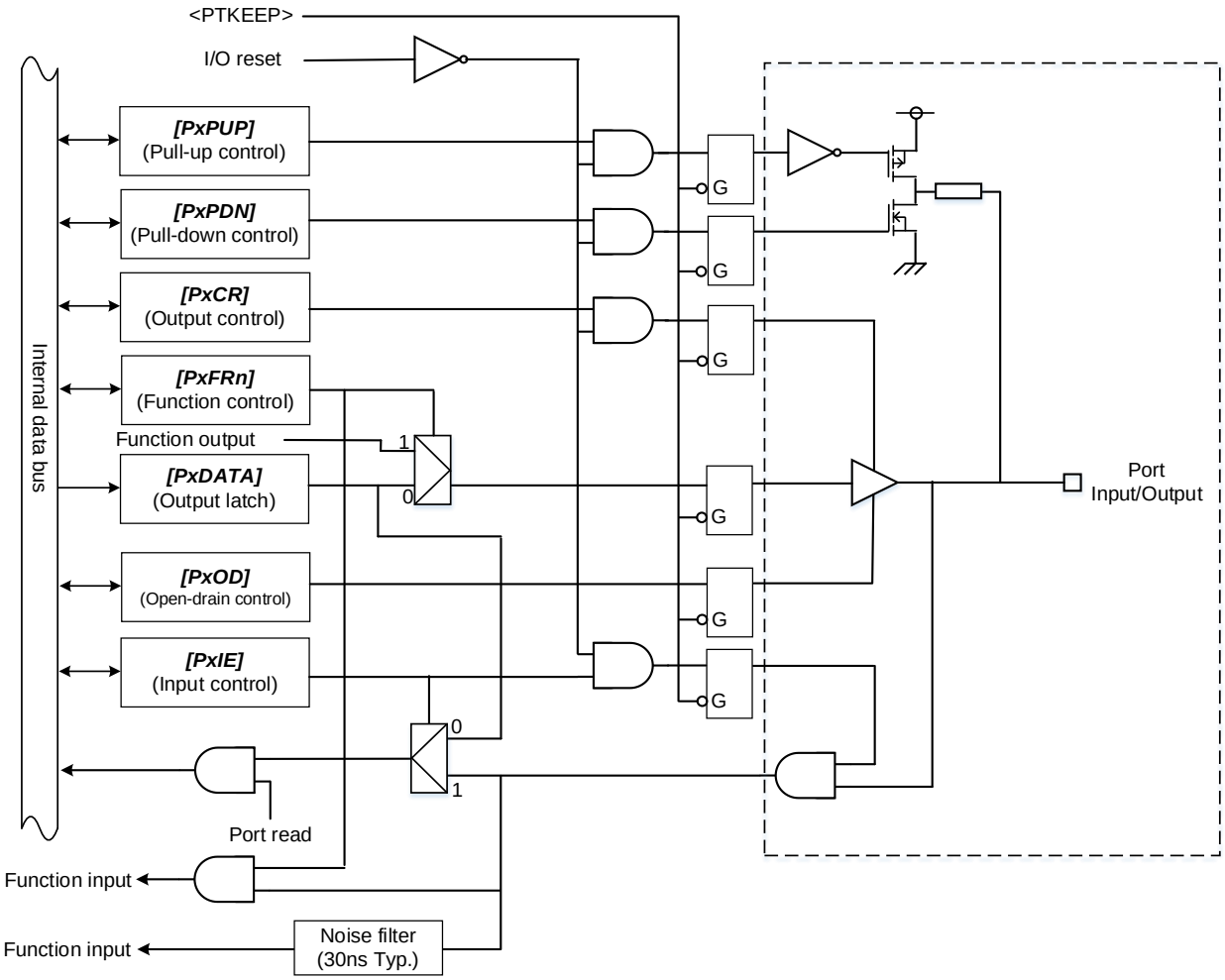



**Figure 5.9 Port Type FTU12**

## 5.10. Type FTU13

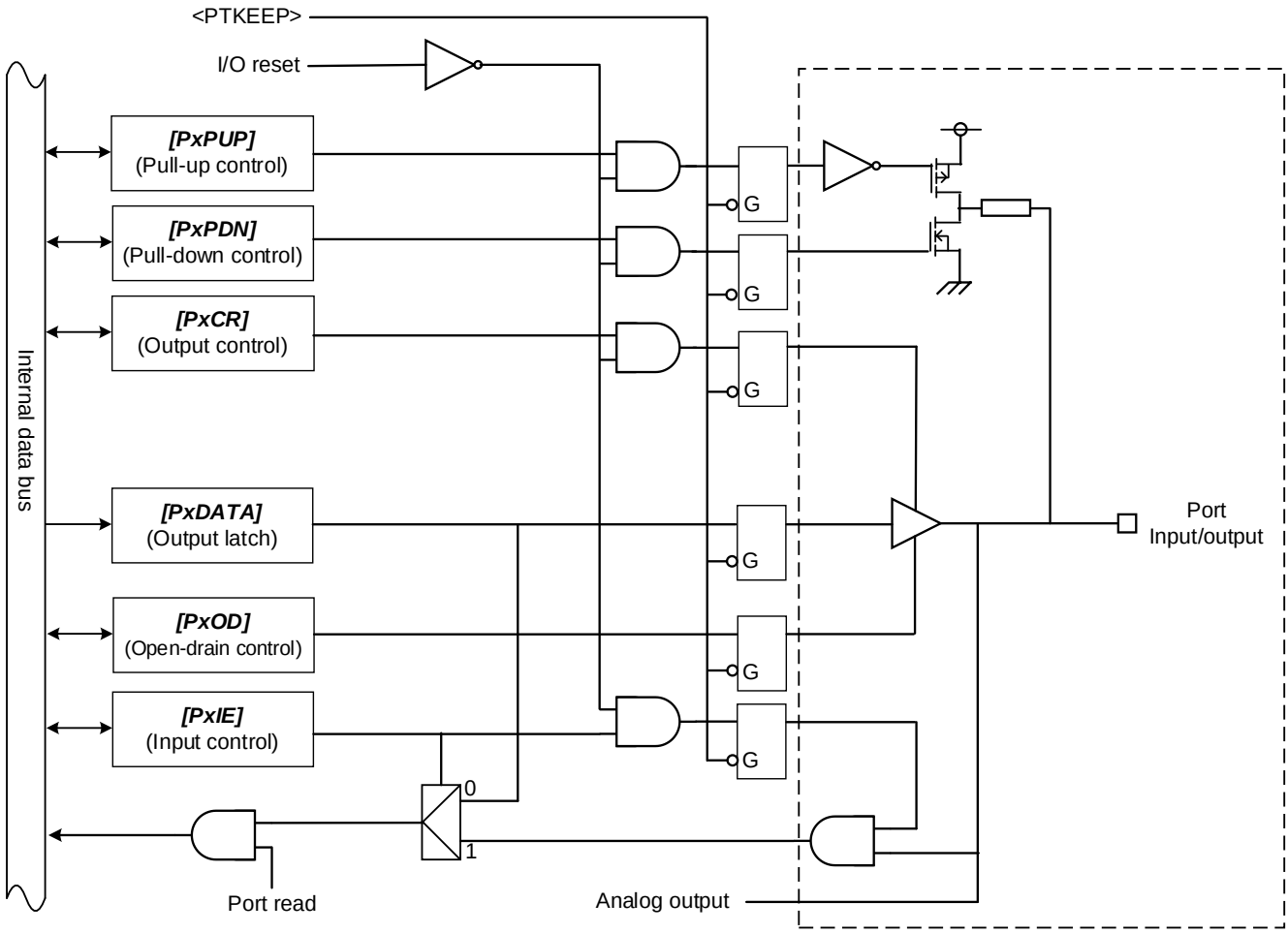



**Figure 5.10 Port Type FTU13**

# 6. Precaution

## 6.1. Pin Status during Reset Period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins(PL0 to PL4) are debug pin status.
- PB0(BOOT_N) works as a BOOT function. It is enabled to be input and pulled-up during pin reset period. At the rising edge of the reset signal, if PB0 is "High", the device enters single chip mode and boots from the on chip flash memory. If PB0 is "Low", the device enters single BOOT mode and boots from the internal BOOT ROM program.

## 6.2. Unused Pins

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

## 6.3. Important Points of Using Debug Interface Pins Used as General-purpose Ports

After releasing reset, If the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer to reference manual "Flash memory".

# 7. Revision History

**Table 7.1 Revision History**

| Revision | Date | Description |
|---|---|---|
| 1.0 | 2021-02-19 | First release |
| 1.1 | 2022-03-31 | - Table 3.1 to 3.13<br>Correct package name of M3HP in title row. |
| 1.2 | 2025-02-21 | - Appearance update<br>- 4.2.3. PORT B<br>Changed table 4.7 and note<br>- 4.2.9. PORT H<br>Changed table 4.13<br>- 5. Block Diagrams of Ports<br>Changed description<br>- 5.7. Type FTU10<br>Added 5.7 chapter<br>- 5.8. Type FTU11<br>Changed figure 5.8<br>Deleted note1 and note2 |

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