32-Bit RISC Microcontroller

TXZ+ Family
TMPM3H Group(1)

Reference Manual
Exception
(EXCEPT-M3H(1))

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
A-PMD	Advanced Programmable Motor Control Circuit
DMAC	Direct Memory Access Controller
EI2C	I^2C Interface Version A
IA	Interrupt control register A
IB	Interrupt control register B
IMCxx	Interrupt Mode Control xx
IMNFLGNMI	Interrupt Monitor Flag NMI
IMNFLGx	Interrupt Monitor Flag x
INT	Interrupt
INTIF	Interrupt Interface Logic
ISR	Interrupt Service Routine
I2C	Inter-Integrated Circuit
I2CS	I^2C wakeup circuit from Stand-by mode
LCD	Liquid Crystal Display
LVD	Voltage Detection Circuit
NICxx	Non-maskable Interrupt Control xx
NVIC	Nested Vectored Interrupt Controller
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
PORF	Power On Reset for FLASH and debug
RAMP	RAM parity
RLMRSTFLGx	RLM Reset Flag x
RMC	Remote Control Signal preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

Exceptions have close relation to the CPU core. Refer to "Arm documentation set for the Arm® Cortex®-M3 processor" if needed.

1. Outlines

Exceptions require CPU to suspend the currently executing process, and to start another process.

There are two types of exceptions: those that are generated when some error condition occurs or when an instruction to generate an exception is executed; and those that are generated by hardware, such as an interrupt request signal from an external pin or peripheral function.

All exceptions are handled by the Nested Vectored Interrupt Controller (NVIC) in the CPU according to the respective priority levels. When an exception occurs, the CPU stores the current state to the stack and branches to the corresponding interrupt service routine (ISR). Upon completion of the ISR, the information stored to the stack is automatically restored.

1.1. Exception Types

The following types of exceptions exist in the Cortex-M3.

For detailed descriptions on each exception, refer to "Arm documentation set for the Arm Cortex-M3 processor".

- Reset
- Non-maskable Interrupt(NMI)
- Hard Fault
- Memory Management
- Bus Fault
- Usage Fault
- SVCall (Supervisor Call)
- Debug Monitor
- PendSV
- SysTick
- External Interrupt

1.2. Exception Handling Flowchart

The following shows how an exception/interrupt is handled. In the following descriptions exception handling by hardware and that by software are explained.

Each step is described later in this reference manual.

Process	Description	See
Detection by INTIF/CPU	The INTIF/CPU detects the exception request.	Section 1.2.1.
⇩		
Handling by CPU	The CPU handles the exception request.	Section 1.2.2.
⇩		
Branch to ISR	The CPU branches to the corresponding interrupt service routine (ISR).	Section 1.2.2.
⇩		
Execution of ISR	Necessary processing is executed	Section 1.2.3.
⇩		
Return from exception	The CPU branches to another ISR or returns to the previous program.	Section 1.2.4.

1.2.1. Exception Request and Detection

(1) Exception Occurrence

Exception factors include instruction execution by the CPU, memory accesses, and interrupt requests from external interrupt pins or peripheral functions.
An exception by the instruction execution occurs when the CPU executes an instruction that causes an exception or when an error condition occurs during instruction execution.
An exception also occurs by an instruction fetch from the Execute Never (XN) region or an access violation to the Fault region.
The request of the exception by the external interrupt pin or the peripheral function occurs by each functional factor. Regarding to interrupt which connected via INTIF, the setup of the Interrupt Control Register is also needed. For details, refer to the chapter, "4.Interrupts".

(2) Exception Detection

If multiple exceptions occur simultaneously, the CPU takes the exception with the highest priority.
The priority of exceptions are below. "Configurable" means that you can assign a priority level to that exception. Memory Management, Bus Fault and Usage Fault exceptions can be enabled or disabled. If a disabled exception occurs, it is handled as Hard Fault.

Table 1.1 Exception Types and Priority

Exception Type	Priority	Description	Offset
Reset	-3(highest)	Reset pin, SIWDT, POR, PORF, OFD, LVD, STOP2 releasing, SYSRESETREQ, LOCKUP signal	0x00
Non-maskable Interrupt	-2	SIWDT, LVD	0x08
Hard Fault	-1	Fault that cannot activate because a higher-priority fault is being handled or it is disabled	0x0C
Memory Management	Configurable	Exception from the Memory Protection Unit (MPU) Instruction fetch from the Execute Never (XN) region	0x10
Bus Fault	Configurable	Access violation to the Hard Fault region of the memory map	0x14
Usage Fault	Configurable	Undefined instruction execution or other faults related to instruction execution	0x18
Reserved	-	-	0x1C to 0x28
SVCall	Configurable	System service call with SVC instruction	0x2C
Debug Monitor	Configurable	Debug monitor when the CPU is not faulting	0x30
Reserved	-	-	0x34
PendSV	Configurable	Pending system service request	0x38
SysTick	Configurable	Notification from system timer	0x3C
External Interrupt	Configurable	External interrupt pin or peripheral function (Note)	0x40

Note: External interrupts have different factors and numbers in each product. For details, see "4.4. List of Interrupt Factors".

(3) Priority Setting

- Priority Level

The external interrupt priority is set to the Interrupt Priority Register and other exceptions are set to <PRI_n> bit in the System Handler Priority Register.

The configuration <PRI_n> can be changed, and the number of bits required for setting the priority varies from 3 bits to 8 bits depending on products. Thus, the range of priority values you can specify is different depending on products.

In the case of 8-bit configuration, the priority can be configured in the range from 0 to 255. The highest priority is "0". If multiple elements with the same priority exist, the smaller the number, the higher the priority becomes.

<PRI_n[7:0]> bit is defined as the upper 4-bit configuration with TMPM3H group(1) products. The priority can be configured in the range from 0 to 15.

- Priority Grouping

The priority group can be split into groups. By setting the <PRIGROUP> of the Application Interrupt and Reset Control Register, <PRI_n> can be divided into the pre-emption priority and the sub priority.

A priority is compared with the pre-emption priority. If the priority is the same as the pre-emption priority, and then it is compared with the sub priority. If the sub priority is the same as the priority, the smaller the exception number, the higher the priority.

The Table 1.2 shows the priority group setting. The pre-emption priority and the sub priority in the table are the number in the case that <PRI_n> is defined as an 8-bit configuration.

Table 1.2 Priority grouping setting

<PRIGROUP[2:0]> setting	<PRI_n[7:0]>		Number of pre-emption priorities	Number of sub priorities
	Pre-emption field	Sub priority field		
000	[7:1]	[0]	128	2
001	[7:2]	[1:0]	64	4
010	[7:3]	[2:0]	32	8
011	[7:4]	[3:0]	16	16
100	[7:5]	[4:0]	8	32
101	[7:6]	[5:0]	4	64
110	[7]	[6:0]	2	128
111	None	[7:0]	1	256

Note: If the configuration of <PRI_n> is less than 8 bits, the lower bit is "0". For the example in the case of 4-bit configuration, the priority is set as <PRI_n[7:4]> and <PRI_n[3:0]> is "0000".

1.2.2. Exception Handling and Branch to Interrupt Service Routine (Pre-emption)

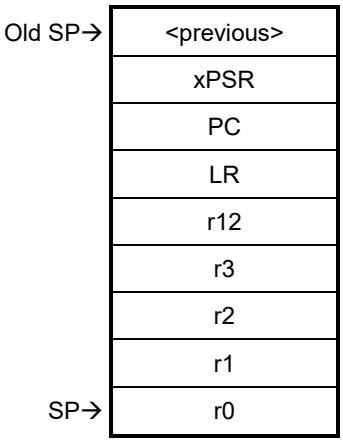
When an exception occurs, the CPU suspends the currently executing process and branches to the interrupt service routine. This is called "pre-emption".

(1) Stacking

When the CPU detects an exception, it pushes the contents of the following eight registers to the stack in the following order:

1. Program Counter (PC)
2. Program Status Register (xPSR)
3. r0 to r3
4. r12
5. Link Register (LR)

The SP is decremented by eight words by the completion of the stack push. The following shows the state of the stack after the register contents have been pushed.



(2) Fetching an ISR

The CPU performs the evacuation of the register. In addition, the CPU performs instruction fetch of the interrupt service routine at the same time.

Prepare a vector table containing the top addresses of ISRs for each exception. After reset, the vector table is located at address 0x00000000 in the Code area. By setting the Vector Table Offset Register, you can place the vector table at any address in the Code or SRAM space.

The vector table should also contain the initial value of the main stack.

(3) Late-arriving

If the CPU detects a higher priority exception before executing the ISR for a previous exception, the CPU handles the higher priority exception first. This is called "late-arriving".

A late-arriving exception causes the CPU to fetch a new vector address for branching to the corresponding ISR, but the CPU does not newly push the register contents to the stack.

(4) Vector Table

The vector table is configured as shown below.
You must always set the first four words (stack top address, reset ISR address, NMI ISR address, and Hard Fault ISR address). Set ISR addresses for other exceptions if necessary.

For other exceptions, you should prepare the ISR addresses if necessary.

Offset	Exception	Contents	Setting
0x00	Reset	Initial value of the main stack	Required
0x04	Reset	ISR address	Required
0x08	Non-maskable Interrupt	ISR address	Required
0x0C	Hard Fault	ISR address	Required
0x10	Memory Management	ISR address	Optional
0x14	Bus Fault	ISR address	Optional
0x18	Usage Fault	ISR address	Optional
0x1C to 0x28	Reserved	-	-
0x2C	SVCall	ISR address	Optional
0x30	Debug Monitor	ISR address	Optional
0x34	Reserved	-	-
0x38	PendSV	ISR address	Optional
0x3C	SysTick	ISR address	Optional
0x40	External Interrupt	ISR address	Optional

1.2.3. Executing an ISR

An ISR performs necessary processing for the corresponding exception. ISRs must be prepared by the user.

An ISR may need to include code for clearing the interrupt request so that the same interrupt will not occur again upon return to normal program execution.

For details about interrupt handling, see "4.Interrupts".

If a higher priority exception occurs during ISR execution for the current exception, the CPU abandons the currently executing ISR and services the newly detected exception.

1.2.4. Exception Exit

(1) Execution after Returning from ISR

When returning from an ISR, the CPU takes one of the following actions:

- Tail-chaining
  If a pending exception exists and there are no stacked exceptions or the pending exception has higher priority than all stacked exceptions, the CPU returns to the ISR of the pending exception.
  In this case, the CPU skips the pop of eight registers and push of eight registers when exiting one ISR and entering another. This is called "tail-chaining".

- Returning to the last stacked ISR
  If there are no pending exceptions or if the highest priority stacked exception is of higher priority than the highest priority pending exception, the CPU returns to the last stacked ISR.

- Returning to the previous program
  If there are no pending or stacked exceptions, the CPU returns to the previous program.

(2) Exception Exit Sequence

When returning from an ISR, the CPU performs the following operations:

- Pop eight registers
  Pop eight registers (PC, xPSR, r0 to r3, r12, and LR) from the stack and adjust the SP.

- Load current active interrupt number
  Loads the current active interrupt number from the stacked xPSR. The CPU uses this to track which interrupt to return to.

- Select SP
  If returning to an exception (Handler Mode), SP is SP_main. If returning to Thread Mode, SP can be SP_main or SP_process.

2. Reset Exception

Reset exceptions are generated from the following nine factors.
Use the ***[RLMRSTFLGn]*** of the Reset Flag Register to identify the factor of a reset.

- Reset exception by external reset pin
  A reset exception occurs when an external reset pin changes from "Low" to "High".

- Reset exception by POR
  A reset exception occurs by POR. For details, refer to Reference Manual "Clock Control and Operation Mode".

- Reset exception by OFD
  The OFD has a reset generating feature. For details, refer to Reference Manual "Oscillation Frequency Detector".

- Reset exception by SIWDT
  The SIWDT has a reset generating feature. For details, refer to Reference Manual "Clock Selective Watchdog Timer".

- Reset exception by LVD
  The LVD has a reset generating feature. For details, refer to Reference Manual "Voltage Detection Circuit".

- Reset exception by PORF
  A reset exception occurs by PORF. For details, refer to Reference Manual "Clock Control and Operation Mode".

- Reset exception by STOP2 mode release
  A reset exception occurs when releasing STOP2 mode. For details, refer to Reference Manual "Clock Control and Operation Mode".

- Reset exception by <SYSRESETREQ>
  A reset can be generated by setting the <SYSRESETREQ> bit in the NVIC's Application Interrupt and Reset Control Register.

- Reset exception by LOCKUP signal
  A reset can be generated by the LOCKUP signal which can be output from the CPU when the un-recoverable exception occurs. For details on the LOCKUP signal, please refer to "Arm documentation set for the Arm Cortex-M3 processor".

3. SysTick

SysTick provides interrupt features using the CPU's system timer.

When you set a value in the SysTick Reload Value Register and enable the SysTick features in the SysTick Control and Status Register, the counter loads with the value set in the Reload Value Register and begins counting down. When the counter reaches "0", a SysTick exception occurs. You may be pending exceptions and use a flag to know when the timer reaches "0".

4. Interrupts

This section explains the route from which a factor and an interrupt request are transmitted, and a required setup.

4.1. Non-maskable Interrupt (NMI)

Non-maskable interrupts are generated from the following two factors.

- Non-maskable interrupt by SIWDT

  The SIWDT has a Non-maskable interrupt generating feature. For details of SIWDT, refer to Reference Manual "Clock Selective Watchdog Timer".

- Non-maskable interrupt by LVD

  The LVD has a Non-maskable interrupt generating feature. For details of LVD, refer to Reference Manual "Voltage Detector Circuit".

4.2. Maskable Interrupt

Please refer to Table 4.3 to Table 4.9 of the "4.4. List of Interrupt Factors" for the factors of the maskable interrupts.

4.3. Interrupt Request

The CPU is notified of interrupt requests by the interrupt signal from each interrupt factor. It sets priority on interrupts and handles an interrupt request with the highest priority.

4.3.1. Interrupt Route

The interrupt is available for the cancellation from a low power consumption mode, and a route varies according to a factor.

Figure 4.1 shows the interrupt transfer route diagram and Table 4.1 shows the explanation of each interrupt transfer route.

- The interrupt that is releasable from IDLE, STOP1, STOP2 mode

  Interrupt which can release from IDLE, STOP1, and the STOP2 mode is controlled by the Interrupt Control Register A in INTIF, and is notified to CPU via INTIF. (Route A, B, C)

- The interrupt that is releasable from IDLE, STOP1 mode

  Interrupt which can release from IDLE and the STOP1 mode is controlled by the Interrupt Control Register B in INTIF, and is notified to CPU via INTIF. (Route D, E, F)

- The interrupt that is releasable from IDLE mode

  Although some factors of interrupt which can release from IDLE mode are controlled by the Interrupt Control Register B via INTIF (Route G), other factors are notified to CPU directly (Route H) not passing through INTIF.

When the interrupt factor that goes by way of an interrupt regardless of low power consumption mode cancellation is used, setting of Interrupt Control Register A or B is necessary.

Please refer to the chapter of "The release source of a Low Power Consumption mode" of a reference manual "Clock Control and Operation Mode" for the details of a low power consumption mode release factor.

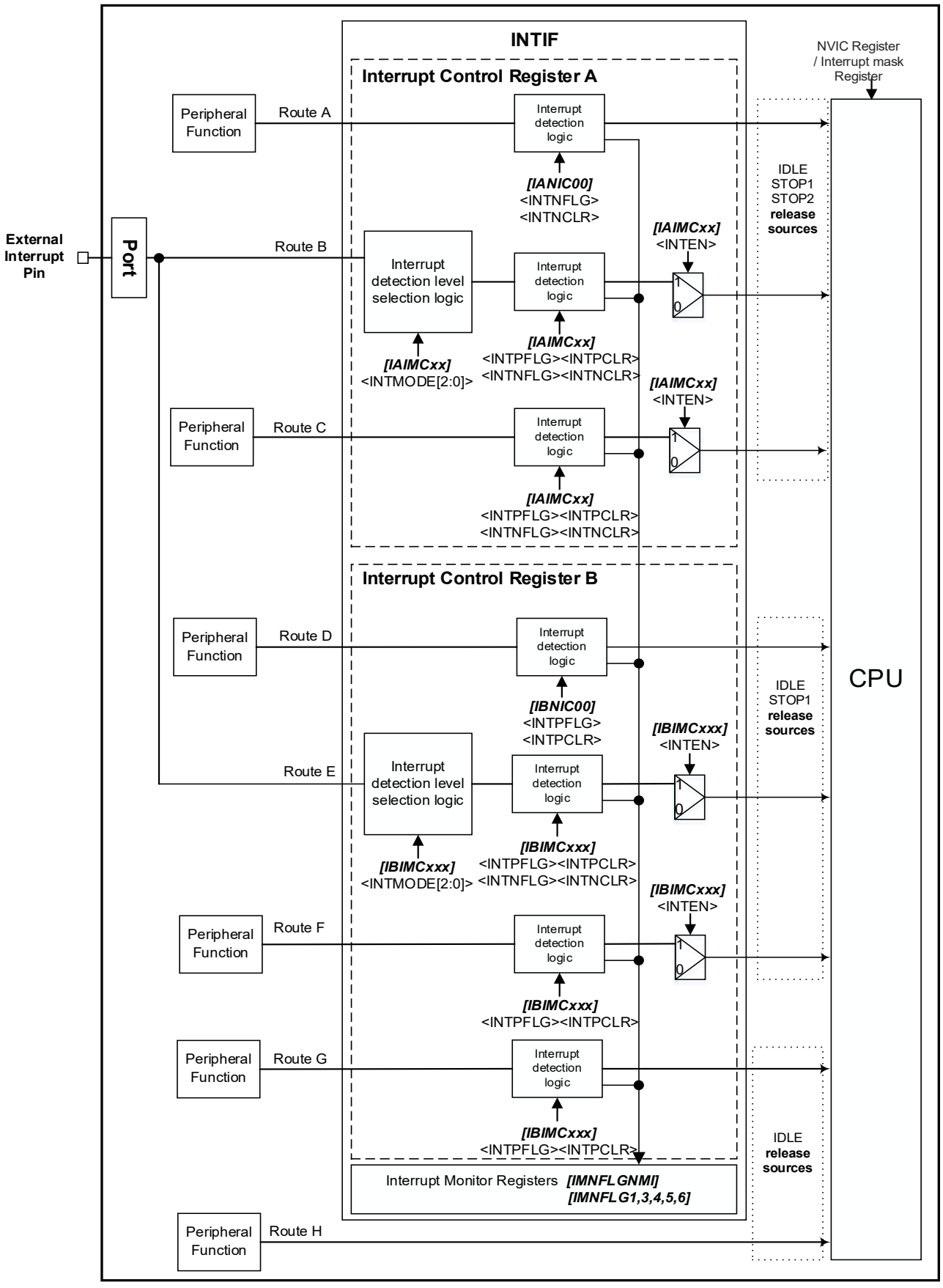


Figure 4.1 Interrupt transfer route Diagram

Table 4.1 Explanation of each interrupt transfer route

Route	Interrupt No.	Interrupt Request	Route Description
A	-	LVD interrupt	This route is NMI interrupt. It is a route input into CPU via INTIF. An interrupt release setup is carried out by the Interrupt Control Register A (***[IANIC00]***).
B	0, 1, 2, 13	External interrupts (00, 01, 02, 13)	This route is the route that an interrupt request of a port is input into CPU. Permission/prohibition of selection of an Interrupt detection level, interrupt release, and an interrupt request are set up by the Interrupt Control Register A (***[IAIMCxx]***) for every factor.
C	50	I2CS I2C Wakeup interrupt	It is a route input into CPU via INTIF. Permission/prohibition of interrupt release and an interrupt request are set up by the Interrupt Control Register A (***[IAIMCxx]***).
	162	RTC interrupt	
D	-	WDT interrupt	This route is non-maskable interrupt. It is a route input into CPU via INTIF. An interrupt release setup is carried out by the Interrupt Control Register B (***[IBNIC00]***).
E	3 to 12 14 to 22	External interrupts (03 to 12, 14 to 33)	This route is the route that an interrupt request of a port is input into CPU. Permission/prohibition of selection of an Interrupt detection level, interrupt release, and an interrupt request are set up by the Interrupt Control Register B (***[IBIMCxxx]***) for every factor.
F	163	Remote control interrupt	This route is a route input into CPU via INTIF. Permission/prohibition of interrupt release and an interrupt request are set up by the Interrupt Control Register B (***[IBIMC094]***).
G	158 to 161	DMAC transfer completion interrupt DMAC transfer error interrupt (Note1)	This route is a route input into CPU via INTIF. An interrupt release setup is carried out by the Interrupt Control Register B (***[IBIMCxxx]***) for every factor.
H	23 to 49, 51 to 157, 164 to 173	Other interrupts (Note2)	It is a route as which an interrupt request is directly input into CPU not passing through INTIF.

Note1: DMAC transfer completion interrupt is an interrupt into which interrupts of two or more channels are combined. Please refer to "4.4.1.About joint interrupt" for details.

Note2: For the details of other interrupts, refer to "4.4. List of Interrupt Factors".

4.3.2. Interrupt Request Generation

An interrupt request is generated from an external interrupt pin or peripheral function which are assigned as interrupt request factors, or by setting the relevant bit of NVIC's Interrupt Set-Pending Register for interrupt request factor.

- Interrupt from external interrupt pin
  Set the port control register so that the external pin can perform as an interrupt function pin. For details on setting, refer to the reference manual "Input/Output Ports".

- Interrupt from peripheral function
  Set the peripheral function to make it possible to output interrupt requests. See the reference manual of each peripheral function for details on setting.

- By setting Interrupt Set-Pending Register (forced pending)
  An interrupt request can be forced to be generated by setting the relevant bit of the Interrupt Set-Pending Register of NVIC.

CPU will recognize the "High" level of the interrupt request as an interrupt.

4.3.3. Monitor of the Interrupt Request

INTIF has the interrupt monitor flags. It can know that the interrupt request has occurred by monitoring the flag. If one request factor is representing several interrupt requests, Interrupt Monitor Register can be used to identify the actual interrupt request factor. For detail, please refer to "4.4. List of Interrupt Factors".

4.3.4. Transmission of Interrupt Request

An interrupt request which is not passing through INTIF will be directly input to the CPU. The interrupts connected to the CPU through INTIF will need proper setting of the Interrupt Control Register in INTIF. A detected interrupt will be sent to the CPU as "High" level signal, when the interrupt is used through INTIF. Please setup an interrupt detection level and interrupt detection enable/disable by INTIF. By the way, please be cautious about external interrupt pin as in the next section.

4.3.5. Precautions When Using External Interrupt Pins

When you use external interrupt, please care about the following points so that an unexpected interrupt does not occur.

If input is disabled (***[PxIE]***<PxmIE>=0), inputs from external interrupt pins are "Low". When the <INTMODE> bit of Interrupt Control Register A (***[IAIMCxx]***) is "Low", then input signals from the external interrupt pins are sent to the CPU as is. Since the CPU recognizes "Low" input as an interrupt, interrupts occur if corresponding interrupts are enabled by the CPU. The interrupt pins should be "High" and the inputs should be enabled. Then the interrupts should be enabled by the CPU.

Note: For port settings, refer to "Input/Output Ports" of the reference manual.

4.4. List of Interrupt Factors

Table 4.2 shows the list of interrupt factors of Non-maskable interrupts. The setting for clearing the NMI factors can be done by Interrupt Control Registers A and B.

Table 4.2 List of Interrupt Factors (Non-maskable Interrupt)

Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
INTLVD	LVD interrupt	***[IANIC00]***	***[IMNFLGNMI]*** <INT000FLG>
INTWDT0	WDT interrupt	***[IBNIC00]***	***[IMNFLGNMI]*** <INT016FLG>

Table 4.3 shows the list of interrupt factors of Interrupt Control Register A. Some interrupt factors set up interrupt detection enable/disable by the Interrupt Control Register A.

Table 4.3 List of Interrupt Factors (Interrupt Control Register A)

Interrupt No,	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
0	INT00	External interrupt 00	***[IAIMC00]***	***[IMNFLG1]*** <INT032FLG>
1	INT01	External interrupt 01	***[IAIMC01]***	***[IMNFLG1]*** <INT033FLG>
2	INT02	External interrupt 02	***[IAIMC02]***	***[IMNFLG1]*** <INT034FLG>
13	INT13	External interrupt 13	***[IAIMC03]***	***[IMNFLG1]*** <INT035FLG>
50	INTI2CWUP	I2CS I2C Wakeup interrupt	***[IAIMC16]***	***[IMNFLG1]*** <INT048FLG>
162	INTRTC	RTC interrupt	***[IAIMC17]***	***[IMNFLG1]*** <INT049FLG>

The factor list of the Interrupt Control Registers B is shown in Table 4.4 to Table 4.10. A part of interrupt sets up interrupt detection enable/disable by the Interrupt Control Register B.

Table 4.4 List of Interrupt Factors (Interrupt Control Register B) (1/7)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
3	INT03	External interrupt 03	***[IBIMC066]***	***[IMNFLG5]*** <INT162FLG>
4	INT04	External interrupt 04	***[IBIMC067]***	***[IMNFLG5]*** <INT163FLG>
5	INT05	External interrupt 05	***[IBIMC068]***	***[IMNFLG5]*** <INT164FLG>
6	INT06	External interrupt 06	***[IBIMC069]***	***[IMNFLG5]*** <INT165FLG>
7	INT07	External interrupt 07	***[IBIMC070]***	***[IMNFLG5]*** <INT166FLG>
8	INT08	External interrupt 08	***[IBIMC071]***	***[IMNFLG5]*** <INT167FLG>
9	INT09	External interrupt 09	***[IBIMC072]***	***[IMNFLG5]*** <INT168FLG>
10	INT10	External interrupt 10	***[IBIMC073]***	***[IMNFLG5]*** <INT169FLG>
11	INT11	External interrupt 11	***[IBIMC074]***	***[IMNFLG5]*** <INT170FLG>
12	INT12	External interrupt 12	***[IBIMC075]***	***[IMNFLG5]*** <INT171FLG>
14	INT14	External interrupt 14	***[IBIMC076]***	***[IMNFLG5]*** <INT172FLG>
15	INT15	External interrupt 15	***[IBIMC077]***	***[IMNFLG5]*** <INT173FLG>
16	INT16	External interrupt 16	***[IBIMC078]***	***[IMNFLG5]*** <INT174FLG>
17	INT17_18_32_33 (Note)	External interrupt 17	***[IBIMC079]***	***[IMNFLG5]*** <INT175FLG>
		External interrupt 18	***[IBIMC080]***	***[IMNFLG5]*** <INT176FLG>
		External interrupt 32	***[IBIMC095]***	***[IMNFLG5]*** <INT191FLG>
		External interrupt 33	***[IBIMC096]***	***[IMNFLG6]*** <INT192FLG>
18	INT19_22 (Note)	External interrupt 19	***[IBIMC081]***	***[IMNFLG5]*** <INT177FLG>
		External interrupt 20	***[IBIMC082]***	***[IMNFLG5]*** <INT178FLG>
		External interrupt 21	***[IBIMC083]***	***[IMNFLG5]*** <INT179FLG>
		External interrupt 22	***[IBIMC084]***	***[IMNFLG5]*** <INT180FLG>
19	INT23_26 (Note)	External interrupt 23	***[IBIMC085]***	***[IMNFLG5]*** <INT181FLG>
		External interrupt 24	***[IBIMC086]***	***[IMNFLG5]*** <INT182FLG>
		External interrupt 25	***[IBIMC087]***	***[IMNFLG5]*** <INT183FLG>
		External interrupt 26	***[IBIMC088]***	***[IMNFLG5]*** <INT184FLG>

Note: Please refer to "4.4.1.About joint interrupt".

Table 4.5 List of Interrupt Factors (Interrupt Control Register B) (2/7)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
20	INT27_28 (Note)	External interrupt 27	***[IBIMC089]***	***[IMNFLG5]*** <INT185FLG>
		External interrupt 28	***[IBIMC090]***	***[IMNFLG5]*** <INT186FLG>
21	INT29	External interrupt 29	***[IBIMC091]***	***[IMNFLG5]*** <INT187FLG>
22	INT30_31 (Note)	External interrupt 30	***[IBIMC092]***	***[IMNFLG5]*** <INT188FLG>
		External interrupt 31	***[IBIMC093]***	***[IMNFLG5]*** <INT189FLG>
23	INTEMG0	A-PMD ch0 EMG interrupt		
24	INTOVV0	A-PMD ch0 OVV interrupt		
25	INTPWM0	A-PMD ch0 PWM interrupt		
26	INTENC00	A-ENC ch0 Encoder input interrupt 0		
27	INTENC01	A-ENC ch0 Encoder input interrupt 1		
28	INTADAPDA	ADC Unit A PMD trigger interrupt A		
29	INTADAPDB	ADC Unit A PMD trigger interrupt B		
30	INTADACP0	ADC Unit A Monitor function 0 interrupt		
31	INTADACP1	ADC Unit A Monitor function 1 interrupt		
32	INTADATRG	ADC Unit A General purpose trigger interrupt		
33	INTADASGL	ADC Unit A Single conversion interrupt		
34	INTADACNT	ADC Unit A Continuous conversion interrupt		
35	INTT0RX	TSPI ch0 Receive interrupt		
36	INTT0TX	TSPI ch0 Transmit interrupt		
37	INTT0ERR	TSPI ch0 Error interrupt		
38	INTT1RX	TSPI ch1 Receive interrupt		
39	INTT1TX	TSPI ch1 Transmit interrupt		
40	INTT1ERR	TSPI ch1 Error interrupt		
41	INTT2RX	TSPI ch2 Receive interrupt		
42	INTT2TX	TSPI ch2 Transmit interrupt		
43	INTT2ERR	TSPI ch2 Error interrupt		
44	INTT3RX	TSPI ch3 Receive interrupt		
45	INTT3TX	TSPI ch3 Transmit interrupt		
46	INTT3ERR	TSPI ch3 Error interrupt		
47	INTT4RX	TSPI ch4 Receive interrupt		
48	INTT4TX	TSPI ch4 Transmit interrupt		
49	INTT4ERR	TSPI ch4 Error interrupt		

Note: Please refer to "4.4.1.About joint interrupt".

Table 4.6 List of Interrupt Factors (Interrupt Control Register B) (3/7)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
50	INTI2CWUP	I2CS I2C Wakeup interrupt	*[IAIMC16]*	*[IMNFLG1]* <INT048FLG>
51	INTI2C0NST (Note)	I2C ch0 interrupt/ EI2C ch0 status interrupt		
52	INTI2C0ATX (Note)	I2C ch0 arbitration lost detection interrupt/ EI2C ch0 transmit buffer empty interrupt		
53	INTI2C0BRX (Note)	I2C ch0 bus free detection interrupt/ EI2C ch0 receive buffer full interrupt		
54	INTI2C0NA	I2C ch0 NACK detection interrupt		
55	INTI2C1NST (Note)	I2C ch1 interrupt/ EI2C ch1 status interrupt		
56	INTI2C1ATX (Note)	I2C ch1 arbitration lost detection interrupt/ EI2C ch1 transmit buffer empty interrupt		
57	INTI2C1BRX (Note)	I2C ch1 bus free detection interrupt/ EI2C ch1 receive buffer full interrupt		
58	INTI2C1NA	I2C ch1 NACK detection interrupt		
59	INTI2C2NST (Note)	I2C ch2 interrupt/ EI2C ch2 status interrupt		
60	INTI2C2ATX (Note)	I2C ch2 arbitration lost detection interrupt/ EI2C ch2 transmit buffer empty interrupt		
61	INTI2C2BRX (Note)	I2C ch2 bus free detection interrupt/ EI2C ch2 receive buffer full interrupt		
62	INTI2C2NA	I2C ch2 NACK detection interrupt		
63	INTI2C3NST (Note)	I2C ch3 interrupt/ EI2C ch3 status interrupt		
64	INTI2C3ATX (Note)	I2C ch3 arbitration lost detection interrupt/ EI2C ch3 transmit buffer empty interrupt		
65	INTI2C3BRX (Note)	I2C ch3 bus free detection interrupt/ EI2C ch3 receive buffer full interrupt		
66	INTI2C3NA	I2C ch3 NACK detection interrupt		
67	INTUART0RX	UART ch0 Reception interrupt		
68	INTUART0TX	UART ch0 Transmission interrupt		
69	INTUART0ERR	UART ch0 Error interrupt		
70	INTUART1RX	UART ch1 Reception interrupt		
71	INTUART1TX	UART ch1 Transmission interrupt		
72	INTUART1ERR	UART ch1 Error interrupt		
73	INTUART2RX	UART ch2 Reception interrupt		
74	INTUART2TX	UART ch2 Transmission interrupt		
75	INTUART2ERR	UART ch2 Error interrupt		
76	INTUART3RX	UART ch3 Reception interrupt		
77	INTUART3TX	UART ch3 Transmission interrupt		
78	INTUART3ERR	UART ch3 Error interrupt		
79	INTUART4RX	UART ch4 Reception interrupt		
80	INTUART4TX	UART ch4 Transmission interrupt		
81	INTUART4ERR	UART ch4 Error interrupt		

Note: Please refer to "4.4.1.About joint interrupt".

Table 4.7 List of Interrupt Factors (Interrupt Control Register B) (4/7)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
82	INTUART5RX	UART ch5 Reception interrupt		
83	INTUART5TX	UART ch5 Transmission interrupt		
84	INTUART5ERR	UART ch5 Error interrupt		
85	INTT32A00A	T32A ch0 timer A match, overflow, and underflow		
86	INTT32A00ACAP0	T32A ch0 timer A capture 0		
87	INTT32A00ACAP1	T32A ch0 timer A capture 1		
88	INTT32A00B	T32A ch0 timer B match, overflow, and underflow		
89	INTT32A00BCAP0	T32A ch0 timer B capture 0		
90	INTT32A00BCAP1	T32A ch0 timer B capture 1		
91	INTT32A00C	T32A ch0 timer C match, overflow, and underflow		
92	INTT32A00CCAP0	T32A ch0 timer C capture 0		
93	INTT32A00CCAP1	T32A ch0 timer C capture 1		
94	INTT32A01A	T32A ch1 timer A match, overflow, and underflow		
95	INTT32A01ACAP0	T32A ch1 timer A capture 0		
96	INTT32A01ACAP1	T32A ch1 timer A capture 1		
97	INTT32A01B	T32A ch1 timer B match, overflow, and underflow		
98	INTT32A01BCAP0	T32A ch1 timer B capture 0		
99	INTT32A01BCAP1	T32A ch1 timer B capture 1		
100	INTT32A01C	T32A ch1 timer C match, overflow, and underflow		
101	INTT32A01CCAP0	T32A ch1 timer C capture 0		
102	INTT32A01CCAP1	T32A ch1 timer C capture 1		
103	INTT32A02A	T32A ch2 timer A match, overflow, and underflow		
104	INTT32A02ACAP0	T32A ch2 timer A capture 0		
105	INTT32A02ACAP1	T32A ch2 timer A capture 1		
106	INTT32A02B	T32A ch2 timer B match, overflow, and underflow		
107	INTT32A02BCAP0	T32A ch2 timer B capture 0		
108	INTT32A02BCAP1	T32A ch2 timer B capture 1		
109	INTT32A02C	T32A ch2 timer C match, overflow, and underflow		
110	INTT32A02CCAP0	T32A ch2 timer C capture 0		
111	INTT32A02CCAP1	T32A ch2 timer C capture 1		

Table 4.8 List of Interrupt Factors (Interrupt Control Register B) (5/7)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
112	INTT32A03A	T32A ch3 timer A match, overflow, and underflow		
113	INTT32A03ACAP0	T32A ch3 timer A capture 0		
114	INTT32A03ACAP1	T32A ch3 timer A capture 1		
115	INTT32A03B	T32A ch3 timer B match, overflow, and underflow		
116	INTT32A03BCAP0	T32A ch3 timer B capture 0		
117	INTT32A03BCAP1	T32A ch3 timer B capture 1		
118	INTT32A03C	T32A ch3 timer C match, overflow, and underflow		
119	INTT32A03CCAP0	T32A ch3 timer C capture 0		
120	INTT32A03CCAP1	T32A ch3 timer C capture 1		
121	INTT32A04A	T32A ch4 timer A match, overflow, and underflow		
122	INTT32A04ACAP0	T32A ch4 timer A capture 0		
123	INTT32A04ACAP1	T32A ch4 timer A capture 1		
124	INTT32A04B	T32A ch4 timer B match, overflow, and underflow		
125	INTT32A04BCAP0	T32A ch4 timer B capture 0		
126	INTT32A04BCAP1	T32A ch4 timer B capture 1		
127	INTT32A04C	T32A ch4 timer C match, overflow, and underflow		
128	INTT32A04CCAP0	T32A ch4 timer C capture 0		
129	INTT32A04CCAP1	T32A ch4 timer C capture 1		
130	INTT32A05A	T32A ch5 timer A match, overflow, and underflow		
131	INTT32A05ACAP0	T32A ch5 timer A capture 0		
132	INTT32A05ACAP1	T32A ch5 timer A capture 1		
133	INTT32A05B	T32A ch5 timer B match, overflow, and underflow		
134	INTT32A05BCAP0	T32A ch5 timer B capture 0		
135	INTT32A05BCAP1	T32A ch5 timer B capture 1		
136	INTT32A05C	T32A ch5 timer C match, overflow, and underflow		
137	INTT32A05CCAP0	T32A ch5 timer C capture 0		
138	INTT32A05CCAP1	T32A ch5 timer C capture 1		
139	INTT32A06A	T32A ch6 timer A match, overflow, and underflow		
140	INTT32A06ACAP0	T32A ch6 timer A capture 0		
141	INTT32A06ACAP1	T32A ch6 timer A capture 1		

Table 4.9 List of Interrupt Factors (Interrupt Control Register B) (6/7)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
142	INTT32A06B	T32A ch6 timer B match, overflow, and underflow		
143	INTT32A06BCAP0	T32A ch6 timer B capture 0		
144	INTT32A06BCAP1	T32A ch6 timer B capture 1		
145	INTT32A06C	T32A ch6 timer C match, overflow, and underflow		
146	INTT32A06CCAP0	T32A ch6 timer C capture 0		
147	INTT32A06CCAP1	T32A ch6 timer C capture 1		
148	INTT32A07A	T32A ch7 timer A match, overflow, and underflow		
149	INTT32A07ACAP0	T32A ch7 timer A capture 0		
150	INTT32A07ACAP1	T32A ch7 timer A capture 1		
151	INTT32A07B	T32A ch7 timer B match, overflow, and underflow		
152	INTT32A07BCAP0	T32A ch7 timer B capture 0		
153	INTT32A07BCAP1	T32A ch7 timer B capture 1		
154	INTT32A07C	T32A ch7 timer C match, overflow, and underflow		
155	INTT32A07CCAP0	T32A ch7 timer C capture 0		
156	INTT32A07CCAP1	T32A ch7 timer C capture 1		
157	INTPARI	RAMP RAM parity interrupt		
158	INTDMAATC (Note)	DMAC Unit A transfer completion interrupt (ch0 to 31)	***[IBIMC000]*** to ***[IBIMC031]***	***[IMNFLG3]*** <INT96FLG> to <INT127FLG>
159	INTDMAAERR	DMAC Unit A transfer error interrupt	***[IBIMC032]***	***[IMNFLG4]*** <INT128FLG>
160	INTDMABTC (Note)	DMAC Unit B transfer completion interrupt (ch0 to 31)	***[IBIMC033]*** to ***[IBIMC064]***	***[IMNFLG4]*** <INT129FLG> to ***[IMNFLG5]*** <INT160FLG>
161	INTDMABERR	DMAC Unit B transfer error interrupt	***[IBIMC065]***	***[IMNFLG5]*** <INT161FLG>
163	INTRMC0	RMC ch0 Remote control interrupt	***[IBIMC094]***	***[IMNFLG5]*** <INT190FLG>
164	INTFLCRDY	Code FLASH Ready interrupt		
165	INTFLDRDY	Data FLASH Ready interrupt		

Note: Please refer to "4.4.1.About joint interrupt".

Table 4.10 List of Interrupt Factors (Interrupt Control Register B) (7/7)

Interrupt No.	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
166	INTLCDBUSF	LCD register write end interrupt		
167	INTLCDSTOP	LCD stop interrupt		
168	INTUART6RX	UART ch6 Reception interrupt		
169	INTUART6TX	UART ch6 Transmission interrupt		
170	INTUART6ERR	UART ch6 Error interrupt		
171	INTUART7RX	UART ch7 Reception interrupt		
172	INTUART7TX	UART ch7 Transmission interrupt		
173	INTUART7ERR	UART ch7 Error interrupt		

4.4.1. About joint interrupt

The details of joint interrupt are as follows:

Table 4.11 Joint interrupt Connection list (1/4)

Interrupt No.	Joint Interrupt factor	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
17	INT17_18_32_33	INT17	External interrupt 17	***[IBIMC079]***	***[IMNFLG5]*** <INT175FLG>
		INT18	External interrupt 18	***[IBIMC080]***	***[IMNFLG5]*** <INT176FLG>
		INT32	External interrupt 32	***[IBIMC095]***	***[IMNFLG5]*** <INT191FLG>
		INT33	External interrupt 33	***[IBIMC096]***	***[IMNFLG6]*** <INT192FLG>
18	INT19_22	INT19	External interrupt 19	***[IBIMC081]***	***[IMNFLG5]*** <INT177FLG>
		INT20	External interrupt 20	***[IBIMC082]***	***[IMNFLG5]*** <INT178FLG>
		INT21	External interrupt 21	***[IBIMC083]***	***[IMNFLG5]*** <INT179FLG>
		INT22	External interrupt 22	***[IBIMC084]***	***[IMNFLG5]*** <INT180FLG>
19	INT23_26	INT23	External interrupt 23	***[IBIMC085]***	***[IMNFLG5]*** <INT181FLG>
		INT24	External interrupt 24	***[IBIMC086]***	***[IMNFLG5]*** <INT182FLG>
		INT25	External interrupt 25	***[IBIMC087]***	***[IMNFLG5]*** <INT183FLG>
		INT26	External interrupt 26	***[IBIMC088]***	***[IMNFLG5]*** <INT184FLG>
20	INT27_28	INT27	External interrupt 27	***[IBIMC089]***	***[IMNFLG5]*** <INT185FLG>
		INT28	External interrupt 28	***[IBIMC090]***	***[IMNFLG5]*** <INT186FLG>
22	INT30_31	INT30	External interrupt 30	***[IBIMC092]***	***[IMNFLG5]*** <INT188FLG>
		INT31	External interrupt 31	***[IBIMC093]***	***[IMNFLG5]*** <INT189FLG>

Table 4.12 Joint interrupt Connection list (2/4)

Interrupt No.	Joint Interrupt Factor	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
51	INTI2C0NST	INTI2C0	I2C ch0 interrupt		
		INTI2C0ST	EI2C ch0 status interrupt		
52	INTI2C0ATX	INTI2C0AL	I2C ch0 arbitration lost detection interrupt		
		INTI2C0TBE	EI2C ch0 transmit buffer empty interrupt		
53	INTI2C0BRX	INTI2C0BF	I2C ch0 bus free detection interrupt		
		INTI2C0RBF	EI2C ch0 receive buffer full interrupt		
55	INTI2C1NST	INTI2C1	I2C ch1 interrupt		
		INTI2C1ST	EI2C ch1 status interrupt		
56	INTI2C1ATX	INTI2C1AL	I2C ch1 arbitration lost detection interrupt		
		INTI2C1TBE	EI2C ch1 transmit buffer empty interrupt		
57	INTI2C1BRX	INTI2C1BF	I2C ch1 bus free detection interrupt		
		INTI2C1RBF	EI2C ch1 receive buffer full interrupt		
59	INTI2C2NST	INTI2C2	I2C ch2 interrupt		
		INTI2C2ST	EI2C ch2 status interrupt		
60	INTI2C2ATX	INTI2C2AL	I2C ch2 arbitration lost detection interrupt		
		INTI2C2TBE	EI2C ch2 transmit buffer empty interrupt		
61	INTI2C2BRX	INTI2C2BF	I2C ch2 bus free detection interrupt		
		INTI2C2RBF	EI2C ch2 receive buffer full interrupt		
63	INTI2C3NST	INTI2C3	I2C ch3 interrupt		
		INTI2C3ST	EI2C ch3 status interrupt		
64	INTI2C3ATX	INTI2C3AL	I2C ch3 arbitration lost detection interrupt		
		INTI2C3TBE	EI2C ch3 transmit buffer empty interrupt		
65	INTI2C3BRX	INTI2C3BF	I2C ch3 bus free detection interrupt		
		INTI2C3RBF	EI2C ch3 receive buffer full interrupt		

Table 4.13 Joint interrupt Connection list (3/4)

Interrupt No.	Interrupt Request		Interrupt Control Register	Interrupt Monitor Register
158	DMAC Unit A transfer completion interrupt (INTDMAATC)	ch0	***[IBIMC000]***	***[IMNFLG3]***<INT96FLG>
		ch1	***[IBIMC001]***	***[IMNFLG3]***<INT97FLG>
		ch2	***[IBIMC002]***	***[IMNFLG3]***<INT98FLG>
		ch3	***[IBIMC003]***	***[IMNFLG3]***<INT99FLG>
		ch4	***[IBIMC004]***	***[IMNFLG3]***<INT100FLG>
		ch5	***[IBIMC005]***	***[IMNFLG3]***<INT101FLG>
		ch6	***[IBIMC006]***	***[IMNFLG3]***<INT102FLG>
		ch7	***[IBIMC007]***	***[IMNFLG3]***<INT103FLG>
		ch8	***[IBIMC008]***	***[IMNFLG3]***<INT104FLG>
		ch9	***[IBIMC009]***	***[IMNFLG3]***<INT105FLG>
		ch10	***[IBIMC010]***	***[IMNFLG3]***<INT106FLG>
		ch11	***[IBIMC011]***	***[IMNFLG3]***<INT107FLG>
		ch12	***[IBIMC012]***	***[IMNFLG3]***<INT108FLG>
		ch13	***[IBIMC013]***	***[IMNFLG3]***<INT109FLG>
		ch14	***[IBIMC014]***	***[IMNFLG3]***<INT110FLG>
		ch15	***[IBIMC015]***	***[IMNFLG3]***<INT111FLG>
		ch16	***[IBIMC016]***	***[IMNFLG3]***<INT112FLG>
		ch17	***[IBIMC017]***	***[IMNFLG3]***<INT113FLG>
		ch18	***[IBIMC018]***	***[IMNFLG3]***<INT114FLG>
		ch19	***[IBIMC019]***	***[IMNFLG3]***<INT115FLG>
		ch20	***[IBIMC020]***	***[IMNFLG3]***<INT116FLG>
		ch21	***[IBIMC021]***	***[IMNFLG3]***<INT117FLG>
		ch22	***[IBIMC022]***	***[IMNFLG3]***<INT118FLG>
		ch23	***[IBIMC023]***	***[IMNFLG3]***<INT119FLG>
		ch24	***[IBIMC024]***	***[IMNFLG3]***<INT120FLG>
		ch25	***[IBIMC025]***	***[IMNFLG3]***<INT121FLG>
		ch26	***[IBIMC026]***	***[IMNFLG3]***<INT122FLG>
		ch27	***[IBIMC027]***	***[IMNFLG3]***<INT123FLG>
		ch28	***[IBIMC028]***	***[IMNFLG3]***<INT124FLG>
		ch29	***[IBIMC029]***	***[IMNFLG3]***<INT125FLG>
		ch30	***[IBIMC030]***	***[IMNFLG3]***<INT126FLG>
		ch31	***[IBIMC031]***	***[IMNFLG3]***<INT127FLG>

Table 4.14 Joint interrupt Connection list (4/4)

Interrupt No.	Interrupt Request		Interrupt Control Register	Interrupt Monitor Register
160	DMAC Unit B transfer completion interrupt (INTDMABTC)	ch0	***[IBIMC033]***	***[IMNFLG4]***<INT129FLG>
		ch1	***[IBIMC034]***	***[IMNFLG4]***<INT130FLG>
		ch2	***[IBIMC035]***	***[IMNFLG4]***<INT131FLG>
		ch3	***[IBIMC036]***	***[IMNFLG4]***<INT132FLG>
		ch4	***[IBIMC037]***	***[IMNFLG4]***<INT133FLG>
		ch5	***[IBIMC038]***	***[IMNFLG4]***<INT134FLG>
		ch6	***[IBIMC039]***	***[IMNFLG4]***<INT135FLG>
		ch7	***[IBIMC040]***	***[IMNFLG4]***<INT136FLG>
		ch8	***[IBIMC041]***	***[IMNFLG4]***<INT137FLG>
		ch9	***[IBIMC042]***	***[IMNFLG4]***<INT138FLG>
		ch10	***[IBIMC043]***	***[IMNFLG4]***<INT139FLG>
		ch11	***[IBIMC044]***	***[IMNFLG4]***<INT140FLG>
		ch12	***[IBIMC045]***	***[IMNFLG4]***<INT141FLG>
		ch13	***[IBIMC046]***	***[IMNFLG4]***<INT142FLG>
		ch14	***[IBIMC047]***	***[IMNFLG4]***<INT143FLG>
		ch15	***[IBIMC048]***	***[IMNFLG4]***<INT144FLG>
		ch16	***[IBIMC049]***	***[IMNFLG4]***<INT145FLG>
		ch17	***[IBIMC050]***	***[IMNFLG4]***<INT146FLG>
		ch18	***[IBIMC051]***	***[IMNFLG4]***<INT147FLG>
		ch19	***[IBIMC052]***	***[IMNFLG4]***<INT148FLG>
		ch20	***[IBIMC053]***	***[IMNFLG4]***<INT149FLG>
		ch21	***[IBIMC054]***	***[IMNFLG4]***<INT150FLG>
		ch22	***[IBIMC055]***	***[IMNFLG4]***<INT151FLG>
		ch23	***[IBIMC056]***	***[IMNFLG4]***<INT152FLG>
		ch24	***[IBIMC057]***	***[IMNFLG4]***<INT153FLG>
		ch25	***[IBIMC058]***	***[IMNFLG4]***<INT154FLG>
		ch26	***[IBIMC059]***	***[IMNFLG4]***<INT155FLG>
		ch27	***[IBIMC060]***	***[IMNFLG4]***<INT156FLG>
		ch28	***[IBIMC061]***	***[IMNFLG4]***<INT157FLG>
		ch29	***[IBIMC062]***	***[IMNFLG4]***<INT158FLG>
		ch30	***[IBIMC063]***	***[IMNFLG4]***<INT159FLG>
		ch31	***[IBIMC064]***	***[IMNFLG5]***<INT160FLG>

4.5. interrupt detection level

When using interrupt via INTIF, interrupt detection level ("Low" level / "High" level / Rising edge / Falling edge) can be selected by interrupt control register A or B. The detected interrupt is output to the CPU with a "High" level signal.

The interrupt signals which are directly transmitted from the various peripheral functions to the CPU, a "High" pulse is output to the CPU as an interrupt request.

The CPU detects the interrupt signal "High" to be an interrupt factor.

4.5.1. Precautions When Releasing the Low Power Consumption Mode

The following setting should be done when releasing STOP1/2 mode.

- The setup of the Interrupt Control Register. (***[IAIMCxx]***, ***[IBIMCxxx]***)
  - Interrupt detection level
  - Interrupt detection enable/disable

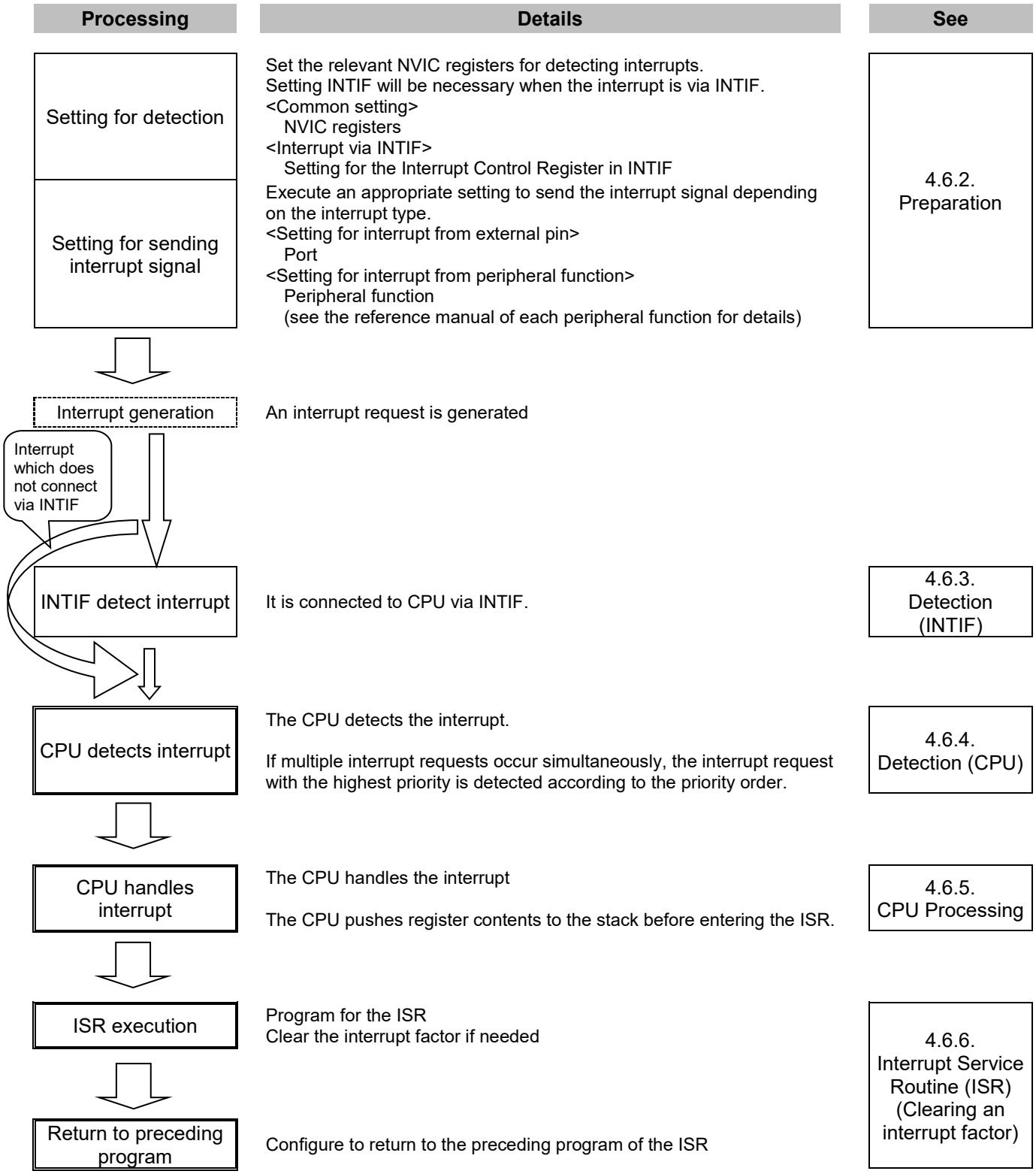
- The setup of the NVIC interrupt enabling set register. (at the time of the STOP1 mode)
  - enable/disable setup

In order to return to NORMAL mode from STOP1 mode, resume suspended instruction by jumping into interrupt after high speed clock oscillation. The operation which returns to NORMAL mode from the STOP2 mode turns on the power supply to the power supply interception domain, and is restarted from the reset sequence.

4.6. Interrupt Handling

4.6.1. Flowchart

The following shows how an interrupt is handled.
The flowchart below explains the interrupt handling process by hardware and software.



4.6.2. Preparation

When preparing for an interrupt, you need to pay attention to the order of configuration to avoid any unexpected interrupt on the way.

Initiating an interrupt or changing its configuration must be implemented in the following order basically. First, disable the interrupt by the CPU. Then, configure each of the interrupt routes. Finally, enable the interrupt by the CPU.

To configure the INTIF, you must follow the order indicated here not to cause any unexpected interrupt. First, configure the precondition. Secondly, clear the data related to the interrupt in the INTIF and then enable the interrupt.

The following sections are listed in the order of interrupt handling and describe how to configure them.

1. Disabling interrupt by CPU
2. CPU registers setting
3. Preconfiguration (1) (Interrupt from external pin)
4. Preconfiguration (2) (Interrupt from peripheral function)
5. Preconfiguration (3) (Interrupt Set-Pending Register)
6. Configuring the INTIF
7. Enabling interrupt by CPU

(1) Disabling Interrupt by CPU

To make the CPU for not accepting any interrupt, write "1" to the corresponding bit of the ***[PRIMASK]*** register. All interrupts and exceptions other than Non-maskable interrupts and hard faults can be masked.

Use "MSR" instruction to set this register.

Interrupt Mask Register		
[PRIMASK]	←	"1"(interrupt disabled)

Note1: ***[PRIMASK]*** register cannot be modified in the user access level.

Note2: If a fault causes when "1" is set to the ***[PRIMASK]*** register, it is treated as a hard fault.

(2) CPU Registers Setting

You can assign a priority level by writing to <PRI_n> field in an Interrupt Priority Register in the NVIC.

Each interrupt factor is provided with eight bits for assigning a priority level from "0" to "255", but the number of bits actually used varies with each product. Priority level "0" is the highest priority level. If multiple factors have the same priority, the smallest-numbered interrupt factor has the highest priority.

You can assign grouping priority by using the <PRIGROUP> in the Application Interrupt and Reset Control Register.

NVIC Register		
<PRI_n>	←	"Priority"
<PRIGROUP>	←	"group priority" (This is configurable if required)

Note: "n" indicates the number of the corresponding exceptions/interrupts.
This product uses four bits for assigning a priority level.

(3) Preconfiguration (1) (Interrupt from external pin)

In order to use external interrupt pin, it is necessary to do proper setting to the port function register of the corresponding pin. Setting ***[PxIE]***<PxmIE> to "1" allows the pin to be used as the function pin and the input port.

Port Register		
[PxIE]<PxmIE>	←	"1"

Note: x: port number, m: bit number of corresponding bit. Be careful not to enable interrupts that are not used when performing interrupt setting. Also be aware of the description of "4.3.5.Precautions When Using External Interrupt Pins".

(4) Preconfiguration (2) (Interrupt from peripheral function)

The setting varies depending on the peripheral function to be used. See the reference manual of each peripheral function for details

(5) Preconfiguration (3) (Interrupt from Set-Pending Register)

To generate an interrupt by using the Interrupt Set-Pending Register, set the corresponding bit of this register to "1".

NVIC Register		
<SETPEND>	←	"1"

Note: <SETPEND>: corresponding bit

(6) Configuring the INTIF

The interrupt by way of INTIF sets the interrupt detection enable in Interrupt Control Registers.

The ***[IANIC00]/[IBNIC00]/[IAIMCxx]/[IBIMCxxx]*** registers are capable of configuring each interrupt factor. Before enabling an interrupt detection, clear the <Detection flag> having active level in order to avoid unexpected interrupt.

Refer to the following for the details of the Interrupt Control Register.

Interrupt Control Register		
[IAIMCxx]<INTMODE> ***[IBIMCxxx]***<INTMODE>	←	Value corresponding to the interrupt to be used (Only for the interrupt having interrupt detection level)
[IANIC00]<INTNCLR> ***[IBNIC00]***<INTPCLR> ***[IAIMCxx]***<INTPCLR><INTNCLR> ***[IBIMCxxx]***<INTPCLR><INTNCLR>	←	<Detection flag> clear to use
[IAIMCxx]<INTEN> ***[IBIMCxxx]***<INTEN>	←	"1" (Interrupt detection enabled)

Note: xx or xxx: number specific to the interrupt request.

(7) Enabling Interrupt by CPU

Enable the interrupt by the CPU as shown below.

Clear the suspended interrupt in the Interrupt Clear-Pending Register. Enable the intended interrupt with the Interrupt Set-Enable Register. Each bit of the register is assigned to a single interrupt factor.

Writing "1" to the corresponding bit of the Interrupt Clear-Pending Register clears the suspended interrupt. Writing "1" to the corresponding bit of the Interrupt Set-Enable Register enables the intended interrupt.

To generate interrupts in the Interrupt Set-Pending Register setting, factors to trigger interrupts are lost if pending interrupts are cleared. Thus, this operation is not necessary.

At the end, ***[PRIMASK]*** register is zero cleared.

NVIC Register		
<CLRPEND>	←	"1"
<SETENA>	←	"1"
Interrupt Mask Register		
[PRIMASK]	←	"0"

Note1: <CLRPEND>,<SETENA>: corresponding bit

Note2: ***[PRIMASK]*** Register cannot be modified by the user access level.

4.6.3. Detection (INTIF)

When the INTIF detects an interrupt request, it sends the interrupt signal in "High" level to the CPU.

INTIF has the functions of the interrupt detection level selection logic, the functions of interrupt detection logic, and the function of the interrupt detection enable/disable. Each function of INTIF is set up by the Interrupt Control Register A or B.

When the rising edge / falling edge / both edges are selected in interrupt detection level selection and INTIF detects an interrupt, it keeps sending the interrupt signal in "High" level to the CPU until the <Detection flag> is cleared in the Interrupt Control Register. If the ISR is exited without clearing the flag, the same interrupt will be detected again when normal operation is resumed. Thus, be sure to clear each <Detection flag> in the ISR. At the same time, the corresponding Interrupt Monitor Register is also cleared.

4.6.4. Detection (CPU)

The CPU detects an interrupt request with the highest priority.

4.6.5. CPU Processing

On detecting an interrupt, the CPU pushes the contents of xPSR, PC, LR, r12, and r3-r0 to the stack then enter the ISR.

4.6.6. Interrupt Service Routine (ISR) (Clearing an interrupt factor)

An ISR requires specific programming according to the application to be used. This section describes what is recommended at the service routine programming and how the factor is cleared.

(1) Process in the Interrupt Service Routine

An ISR normally pushes register contents to the stack and handles an interrupt as required.

The Cortex-M3 processor automatically pushes the contents of xPSR, PC, LR, r12, and r3-r0 to the stack. No extra programming is required for them.

Push the contents of other registers if needed.

Interrupt requests with higher priority and exceptions such as NMI are accepted even when an ISR is being executed. We recommend you to push the contents of general purpose registers that might be rewritten.

(2) Clearing an Interrupt Factor

Some interrupt requests have to be cleared with the Interrupt Control Register.

If an Interrupt detection level is set as level-sensitive, an interrupt request continues to exist until it is cleared at its factor. Therefore, the interrupt factor must be cleared. If a factor is withdrawn in level detection, the interrupt request signal from INTIF will be withdrawn automatically.

A factor is withdrawn by clearing the <Detection flag> of the Interrupt Control Register of INTIF in the case of edge detection. When effective edge occurs again, it is anew recognized as a factor.

Note: After clearing the <Detection flag> of the Interrupt Control Register, please be sure to read the flag which was cleared.

5. Exception/ Interrupt-Related Registers

5.1. Register List

Control Registers and their addresses are as follows:

Interrupt Control Registers A

Peripheral function	Function name	Channel/Unit	Base address
Interrupt control register A	IA	-	0x4003E000

Register name		Address (+Base)
Non-maskable Interrupt A Control Register 00	***[IANIC00]***	0x0000
Interrupt A Mode Control Register 00	***[IAIMC00]***	0x0020
Interrupt A Mode Control Register 01	***[IAIMC01]***	0x0021
Interrupt A Mode Control Register 02	***[IAIMC02]***	0x0022
Interrupt A Mode Control Register 03	***[IAIMC03]***	0x0023
Interrupt A Mode Control Register 16	***[IAIMC16]***	0x0030
Interrupt A Mode Control Register 17	***[IAIMC17]***	0x0031

Note: Byte access is needed for ***[IANIC00]*** and ***[IAIMCxx]***.

Interrupt Control Registers B

Peripheral function	Function name	Channel/Unit	Base address
Interrupt control register B	IB	-	0x400F4E00

Register name		Address (+Base)
Non-maskable Interrupt B Control Register 00	***[IBNIC00]***	0x0010
Interrupt B Mode Control Register 000	***[IBIMC000]***	0x0060
Interrupt B Mode Control Register 001	***[IBIMC001]***	0x0061
Interrupt B Mode Control Register 002	***[IBIMC002]***	0x0062
Interrupt B Mode Control Register 003	***[IBIMC003]***	0x0063
Interrupt B Mode Control Register 004	***[IBIMC004]***	0x0064
Interrupt B Mode Control Register 005	***[IBIMC005]***	0x0065
Interrupt B Mode Control Register 006	***[IBIMC006]***	0x0066
Interrupt B Mode Control Register 007	***[IBIMC007]***	0x0067
Interrupt B Mode Control Register 008	***[IBIMC008]***	0x0068
Interrupt B Mode Control Register 009	***[IBIMC009]***	0x0069
Interrupt B Mode Control Register 010	***[IBIMC010]***	0x006A
Interrupt B Mode Control Register 011	***[IBIMC011]***	0x006B
Interrupt B Mode Control Register 012	***[IBIMC012]***	0x006C
Interrupt B Mode Control Register 013	***[IBIMC013]***	0x006D
Interrupt B Mode Control Register 014	***[IBIMC014]***	0x006E
Interrupt B Mode Control Register 015	***[IBIMC015]***	0x006F
Interrupt B Mode Control Register 016	***[IBIMC016]***	0x0070
Interrupt B Mode Control Register 017	***[IBIMC017]***	0x0071
Interrupt B Mode Control Register 018	***[IBIMC018]***	0x0072
Interrupt B Mode Control Register 019	***[IBIMC019]***	0x0073
Interrupt B Mode Control Register 020	***[IBIMC020]***	0x0074
Interrupt B Mode Control Register 021	***[IBIMC021]***	0x0075
Interrupt B Mode Control Register 022	***[IBIMC022]***	0x0076
Interrupt B Mode Control Register 023	***[IBIMC023]***	0x0077
Interrupt B Mode Control Register 024	***[IBIMC024]***	0x0078
Interrupt B Mode Control Register 025	***[IBIMC025]***	0x0079
Interrupt B Mode Control Register 026	***[IBIMC026]***	0x007A
Interrupt B Mode Control Register 027	***[IBIMC027]***	0x007B
Interrupt B Mode Control Register 028	***[IBIMC028]***	0x007C
Interrupt B Mode Control Register 029	***[IBIMC029]***	0x007D
Interrupt B Mode Control Register 030	***[IBIMC030]***	0x007E
Interrupt B Mode Control Register 031	***[IBIMC031]***	0x007F
Interrupt B Mode Control Register 032	***[IBIMC032]***	0x0080
Interrupt B Mode Control Register 033	***[IBIMC033]***	0x0081
Interrupt B Mode Control Register 034	***[IBIMC034]***	0x0082
Interrupt B Mode Control Register 035	***[IBIMC035]***	0x0083

Register name		Address (+Base)
Interrupt B Mode Control Register 036	***[IBIMC036]***	0x0084
Interrupt B Mode Control Register 037	***[IBIMC037]***	0x0085
Interrupt B Mode Control Register 038	***[IBIMC038]***	0x0086
Interrupt B Mode Control Register 039	***[IBIMC039]***	0x0087
Interrupt B Mode Control Register 040	***[IBIMC040]***	0x0088
Interrupt B Mode Control Register 041	***[IBIMC041]***	0x0089
Interrupt B Mode Control Register 042	***[IBIMC042]***	0x008A
Interrupt B Mode Control Register 043	***[IBIMC043]***	0x008B
Interrupt B Mode Control Register 044	***[IBIMC044]***	0x008C
Interrupt B Mode Control Register 045	***[IBIMC045]***	0x008D
Interrupt B Mode Control Register 046	***[IBIMC046]***	0x008E
Interrupt B Mode Control Register 047	***[IBIMC047]***	0x008F
Interrupt B Mode Control Register 048	***[IBIMC048]***	0x0090
Interrupt B Mode Control Register 049	***[IBIMC049]***	0x0091
Interrupt B Mode Control Register 050	***[IBIMC050]***	0x0092
Interrupt B Mode Control Register 051	***[IBIMC051]***	0x0093
Interrupt B Mode Control Register 052	***[IBIMC052]***	0x0094
Interrupt B Mode Control Register 053	***[IBIMC053]***	0x0095
Interrupt B Mode Control Register 054	***[IBIMC054]***	0x0096
Interrupt B Mode Control Register 055	***[IBIMC055]***	0x0097
Interrupt B Mode Control Register 056	***[IBIMC056]***	0x0098
Interrupt B Mode Control Register 057	***[IBIMC057]***	0x0099
Interrupt B Mode Control Register 058	***[IBIMC058]***	0x009A
Interrupt B Mode Control Register 059	***[IBIMC059]***	0x009B
Interrupt B Mode Control Register 060	***[IBIMC060]***	0x009C
Interrupt B Mode Control Register 061	***[IBIMC061]***	0x009D
Interrupt B Mode Control Register 062	***[IBIMC062]***	0x009E
Interrupt B Mode Control Register 063	***[IBIMC063]***	0x009F
Interrupt B Mode Control Register 064	***[IBIMC064]***	0x00A0
Interrupt B Mode Control Register 065	***[IBIMC065]***	0x00A1
Interrupt B Mode Control Register 066	***[IBIMC066]***	0x00A2
Interrupt B Mode Control Register 067	***[IBIMC067]***	0x00A3
Interrupt B Mode Control Register 068	***[IBIMC068]***	0x00A4
Interrupt B Mode Control Register 069	***[IBIMC069]***	0x00A5
Interrupt B Mode Control Register 070	***[IBIMC070]***	0x00A6
Interrupt B Mode Control Register 071	***[IBIMC071]***	0x00A7
Interrupt B Mode Control Register 072	***[IBIMC072]***	0x00A8
Interrupt B Mode Control Register 073	***[IBIMC073]***	0x00A9
Interrupt B Mode Control Register 074	***[IBIMC074]***	0x00AA
Interrupt B Mode Control Register 075	***[IBIMC075]***	0x00AB
Interrupt B Mode Control Register 076	***[IBIMC076]***	0x00AC
Interrupt B Mode Control Register 077	***[IBIMC077]***	0x00AD

Register name		Address (+Base)
Interrupt B Mode Control Register 078	***[IBIMC078]***	0x00AE
Interrupt B Mode Control Register 079	***[IBIMC079]***	0x00AF
Interrupt B Mode Control Register 080	***[IBIMC080]***	0x00B0
Interrupt B Mode Control Register 081	***[IBIMC081]***	0x00B1
Interrupt B Mode Control Register 082	***[IBIMC082]***	0x00B2
Interrupt B Mode Control Register 083	***[IBIMC083]***	0x00B3
Interrupt B Mode Control Register 084	***[IBIMC084]***	0x00B4
Interrupt B Mode Control Register 085	***[IBIMC085]***	0x00B5
Interrupt B Mode Control Register 086	***[IBIMC086]***	0x00B6
Interrupt B Mode Control Register 087	***[IBIMC087]***	0x00B7
Interrupt B Mode Control Register 088	***[IBIMC088]***	0x00B8
Interrupt B Mode Control Register 089	***[IBIMC089]***	0x00B9
Interrupt B Mode Control Register 090	***[IBIMC090]***	0x00BA
Interrupt B Mode Control Register 091	***[IBIMC091]***	0x00BB
Interrupt B Mode Control Register 092	***[IBIMC092]***	0x00BC
Interrupt B Mode Control Register 093	***[IBIMC093]***	0x00BD
Interrupt B Mode Control Register 094	***[IBIMC094]***	0x00BE
Interrupt B Mode Control Register 095	***[IBIMC095]***	0x00BF
Interrupt B Mode Control Register 096	***[IBIMC096]***	0x00C0

Note: Byte access is needed for ***[IBNIC00]*** and ***[IBIMCxxx]*** Registers.

Reset Flag Registers

Peripheral function	Function name	Channel/Unit	Base address
Low speed oscillation/power control/reset	RLM	-	0x4003E400

Register name		Address (+Base)
Reset Flag Register 0	***[RLMRSTFLG0]***	0x0002
Reset Flag Register 1	***[RLMRSTFLG1]***	0x0003

Note: Byte access is needed for Reset Flag Registers.

Interrupt Monitor Registers

Peripheral function	Function name	Channel/Unit	Base address
Interrupt Monitor	IMN	-	0x400F4F00

Register name		Address (+Base)
Non-maskable Interrupt Monitor Flag Register	***[IMNFLGNMI]***	0x0000
Interrupt Monitor Flag Register 1	***[IMNFLG1]***	0x0004
Interrupt Monitor Flag Register 3	***[IMNFLG3]***	0x000C
Interrupt Monitor Flag Register 4	***[IMNFLG4]***	0x0010
Interrupt Monitor Flag Register 5	***[IMNFLG5]***	0x0014
Interrupt Monitor Flag Register 6	***[IMNFLG6]***	0x0018

NVIC Registers

Peripheral function	Channel/Unit	Base address
NVIC Register	-	0xE000E000

Register name	Address (+Base)
SysTick Control and Status Register	0x0010
SysTick Reload Value Register	0x0014
SysTick Current Value Register	0x0018
SysTick Calibration Value Register	0x001C
Interrupt Set-Enable Register0	0x0100
Interrupt Set-Enable Register1	0x0104
Interrupt Set-Enable Register2	0x0108
Interrupt Set-Enable Register3	0x010C
Interrupt Set-Enable Register4	0x0110
Interrupt Set-Enable Register5	0x0114
Interrupt Clear-Enable Register0	0x0180
Interrupt Clear-Enable Register1	0x0184
Interrupt Clear-Enable Register2	0x0188
Interrupt Clear-Enable Register3	0x018C
Interrupt Clear-Enable Register4	0x0190
Interrupt Clear-Enable Register5	0x0194
Interrupt Set-Pending Register0	0x0200
Interrupt Set-Pending Register1	0x0204
Interrupt Set-Pending Register2	0x0208
Interrupt Set-Pending Register3	0x020C
Interrupt Set-Pending Register4	0x0210
Interrupt Set-Pending Register5	0x0214
Interrupt Clear-Pending Register0	0x0280
Interrupt Clear-Pending Register1	0x0284
Interrupt Clear-Pending Register2	0x0288
Interrupt Clear-Pending Register3	0x028C
Interrupt Clear-Pending Register4	0x0290
Interrupt Clear-Pending Register5	0x0294
Interrupt Priority Register	0x0400 to 0x04AD
Vector Table Offset Register	0x0D08
Application Interrupt and Reset Control Register	0x0D0C
System Handler Priority Register	0x0D18, 0x0D1C, 0x0D20
System Handler Control and State Register	0x0D24

5.2. Interrupt Control Registers A

5.2.1. *[IANIC00]* (Non-maskable Interrupt A Control Register 00)

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
6	-	0	R	Read as "0".
5	INTNFLG	0	R	Detection flag 0: Not detected 1: Detected
4:0	-	00101	R	Read as "00101".

5.2.2. *[IAIMC00 to 03,16 to 17]* (Interrupt A Mode Control Register nn)

(1) *[IAIMC00 to 03]* Registers

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Falling edge detection flag clear control 0: - 1: Clear Read as "0".
6	INTPCLR	0	W	Rising edge detection flag clear control 0: - 1: Clear Read as "0".
5	INTNFLG	0	R	Falling edge detection flag 0: Not detected 1: Detected
4	INTPFLG	0	R	Rising edge detection flag 0: Not detected 1: Detected
3:1	INTMODE[2:0]	000	R/W	Interrupt detection level selection 000: Low level 001: High level 010: Falling edge 011: Rising edge 100: Both edge 101: Reserved 110: Reserved 111: Reserved
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

(2) *[IAIMC16]* Register

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0".
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
5	-	0	R	Read as "0".
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:1	-	011	R	Read as "011".
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

(3) *[IAIMC17]* Register

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
6	-	0	R	Read as "0".
5	INTNFLG	0	R	Detection flag 0: Not detected 1: Detected
4:1	-	0010	R	Read as "0010".
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

5.3. Interrupt Control Registers B

5.3.1. *[IBNIC00]* (Non-maskable Interrupt B Control Register 00)

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0".
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0"".
5	-	0	R	Read as "0".
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:0	-	0111	R	Read as "0111".

5.3.2. *[IBIMC000 to 065, 066 to 093, 094]* (Interrupt B Mode Control Register nnn)

(1) *[IBIMC000 to 065]* Registers

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0".
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
5	-	0	R	Read as "0".
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:0	-	0111	R	Read as"0111".

(2) *[IBIMC066 to 093], [IBIMC095 to 096]* Registers

Bit	Bit Symbol	After Reset	Type	Function
7	INTNCLR	0	W	Falling edge detection flag clear control 0: - 1: Clear Read as "0".
6	INTPCLR	0	W	Rising edge detection flag clear control 0: - 1: Clear Read as "0".
5	INTNFLG	0	R	Falling edge detection flag 0: Not detected 1: Detected
4	INTPFLG	0	R	Rising edge detection flag 0: Not detected 1: Detected
3:1	INTMODE[2:0]	000	R/W	Interrupt detection level selection 000: Low level 001: High level 010: Falling edge 011: Rising edge 100: Both edge 101: Reserved 110: Reserved 111: Reserved
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

(3) *[IBIMC094]* Register

Bit	Bit Symbol	After Reset	Type	Function
7	-	0	R	Read as "0".
6	INTPCLR	0	W	Detection flag clear control 0: - 1: Clear Read as "0".
5	-	0	R	Read as "0".
4	INTPFLG	0	R	Detection flag 0: Not detected 1: Detected
3:1	-	011	R	Read as "011".
0	INTEN	0	R/W	Interrupt control 0: Interrupt detection disabled 1: Interrupt detection enabled

5.4. Reset Flag Registers

5.4.1. *[RLMRSTFLG0]* (Reset Flag Register 0)

Bit	Bit Symbol	After power on reset	Type	Function
7:6	-	0	R	Read as "0".
5	LVDRSTF	Undefined	R	LVD / PORF reset flag 0: - 1: Reset by LVD / PORF
			W	LVD / PORF reset flag 0: Clear 1: Don't care
4	STOP2RSTF	Undefined	R	STOP2 reset flag 0: - 1: Reset generated by releasing STOP2 mode
			W	STOP2 reset flag 0: Clear 1: Don't care
3	PINRSTF	Undefined	R	Reset pin flag 0: - 1: Reset by reset pin
			W	Reset pin flag 0: Clear 1: Don't care
2:1	-	Undefined	R	Read as an undefined value.
			W	Write as "00".
0	PORSTF	1	R	Power On Reset flag 0: - 1: Reset by power-on reset
			W	Power On Reset flag 0: Clear 1: Don't care

Note: Reset flags except <PORSTF> become undefined after Power On Reset release. When release of Power On Reset is detected, please write "0" into all reset flags for initialization.

5.4.2. *[RLMRSTFLG1]* (Reset Flag Register 1)

Bit	Bit Symbol	After power on reset	Type	Function
7:4	-	0	R	Read as "0".
3	OFDRSTF	0	R	OFD reset flag 0: - 1: Reset by OFD
			W	OFD reset flag 0: Clear 1: Don't care
2	WDTRSTF	0	R	SIWDT reset flag 0: - 1: Reset by SIWDT
			W	SIWDT reset flag 0: Clear 1: Don't care
1	LOCKRSTF	0	R	LOCKUP reset flag 0: - 1: Reset by LOCKUP
			W	LOCKUP reset flag 0: Clear 1: Don't care
0	SYSRSTF	0	R	<SYSRESETREQ> reset flag 0: - 1: Reset by <SYSRESETREQ>
			W	<SYSRESETREQ> reset flag 0: Clear 1: Don't care

5.5. Interrupt Monitor Registers

5.5.1. *[IMNFLGNMI]* (Non-maskable Interrupt Monitor Flag Register)

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	INT016FLG	0	R	INTWDT0 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15:1	-	0	R	Read as "0".
0	INT000FLG	0	R	INTLVD Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.2. *[IMNFLG1]* (Interrupt Monitor Flag Register 1)

Bit	Bit Symbol	After Reset	Type	Function
31:18	-	0	R	Read as "0".
17	INT049FLG	0	R	INTRTC Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT048FLG	0	R	INTI2CWUP Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
15:4	-	0	R	Read as "0".
3	INT035FLG	0	R	INT13 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT034FLG	0	R	INT02 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT033FLG	0	R	INT01 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT032FLG	0	R	INT00 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.3. *[IMNFLG3]* (Interrupt Monitor Flag Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31	INT127FLG	0	R	INTDMAATC(ch31) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT126FLG	0	R	INTDMAATC(ch30) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT125FLG	0	R	INTDMAATC(ch29) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT124FLG	0	R	INTDMAATC(ch28) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT123FLG	0	R	INTDMAATC(ch27) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT122FLG	0	R	INTDMAATC(ch26) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT121FLG	0	R	INTDMAATC(ch25) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT120FLG	0	R	INTDMAATC(ch24) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT119FLG	0	R	INTDMAATC(ch23) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT118FLG	0	R	INTDMAATC(ch22) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT117FLG	0	R	INTDMAATC(ch21) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT116FLG	0	R	INTDMAATC(ch20) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT115FLG	0	R	INTDMAATC(ch19) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT114FLG	0	R	INTDMAATC(ch18) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT113FLG	0	R	INTDMAATC(ch17) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT112FLG	0	R	INTDMAATC(ch16) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
15	INT111FLG	0	R	INTDMAATC(ch15) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT110FLG	0	R	INTDMAATC(ch14) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT109FLG	0	R	INTDMAATC(ch13) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
12	INT108FLG	0	R	INTDMAATC(ch12) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT107FLG	0	R	INTDMAATC(ch11) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT106FLG	0	R	INTDMAATC(ch10) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT105FLG	0	R	INTDMAATC(ch9) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT104FLG	0	R	INTDMAATC(ch8) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT103FLG	0	R	INTDMAATC(ch7) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT102FLG	0	R	INTDMAATC(ch6) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT101FLG	0	R	INTDMAATC(ch5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT100FLG	0	R	INTDMAATC(ch4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT099FLG	0	R	INTDMAATC(ch3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT098FLG	0	R	INTDMAATC(ch2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT097FLG	0	R	INTDMAATC(ch1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT096FLG	0	R	INTDMAATC(ch0) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.4. *[IMNFLG4]* (Interrupt Monitor Flag Register 4)

Bit	Bit Symbol	After Reset	Type	Function
31	INT159FLG	0	R	INTDMABTC(ch30) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT158FLG	0	R	INTDMABTC(ch29) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT157FLG	0	R	INTDMABTC(ch28) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT156FLG	0	R	INTDMABTC(ch27) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT155FLG	0	R	INTDMABTC(ch26) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT154FLG	0	R	INTDMABTC(ch25) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT153FLG	0	R	INTDMABTC(ch24) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT152FLG	0	R	INTDMABTC(ch23) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT151FLG	0	R	INTDMABTC(ch22) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT150FLG	0	R	INTDMABTC(ch21) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT149FLG	0	R	INTDMABTC(ch20) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT148FLG	0	R	INTDMABTC(ch19) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT147FLG	0	R	INTDMABTC(ch18) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT146FLG	0	R	INTDMABTC(ch17) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT145FLG	0	R	INTDMABTC(ch16) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT144FLG	0	R	INTDMABTC(ch15) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
15	INT143FLG	0	R	INTDMABTC(ch14) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT142FLG	0	R	INTDMABTC(ch13) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT141FLG	0	R	INTDMABTC(ch12) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
12	INT140FLG	0	R	INTDMABTC(ch11) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT139FLG	0	R	INTDMABTC(ch10) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT138FLG	0	R	INTDMABTC(ch9) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT137FLG	0	R	INTDMABTC(ch8) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT136FLG	0	R	INTDMABTC(ch7) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT135FLG	0	R	INTDMABTC(ch6) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT134FLG	0	R	INTDMABTC(ch5) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT133FLG	0	R	INTDMABTC(ch4) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT132FLG	0	R	INTDMABTC(ch3) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT131FLG	0	R	INTDMABTC(ch2) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT130FLG	0	R	INTDMABTC(ch1) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT129FLG	0	R	INTDMABTC(ch0) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT128FLG	0	R	INTDMAAERR Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.5. *[IMNFLG5]* (Interrupt Monitor Flag Register 5)

Bit	Bit Symbol	After Reset	Type	Function
31	INT191FLG	0	R	INT32 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
30	INT190FLG	0	R	INTRMC0 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
29	INT189FLG	0	R	INT31 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
28	INT188FLG	0	R	INT30 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
27	INT187FLG	0	R	INT29 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
26	INT186FLG	0	R	INT28 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
25	INT185FLG	0	R	INT27 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
24	INT184FLG	0	R	INT26 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
23	INT183FLG	0	R	INT25 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
22	INT182FLG	0	R	INT24 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
21	INT181FLG	0	R	INT23 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
20	INT180FLG	0	R	INT22 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
19	INT179FLG	0	R	INT21 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
18	INT178FLG	0	R	INT20 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
17	INT177FLG	0	R	INT19 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
16	INT176FLG	0	R	INT18 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

Bit	Bit Symbol	After Reset	Type	Function
15	INT175FLG	0	R	INT17 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
14	INT174FLG	0	R	INT16 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
13	INT173FLG	0	R	INT15 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
12	INT172FLG	0	R	INT14 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
11	INT171FLG	0	R	INT12 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
10	INT170FLG	0	R	INT11 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
9	INT169FLG	0	R	INT10 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
8	INT168FLG	0	R	INT09 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
7	INT167FLG	0	R	INT08 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
6	INT166FLG	0	R	INT07 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
5	INT165FLG	0	R	INT06 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
4	INT164FLG	0	R	INT05 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
3	INT163FLG	0	R	INT04 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
2	INT162FLG	0	R	INT03 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
1	INT161FLG	0	R	INTDMABERR Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected
0	INT160FLG	0	R	INTDMABTC(ch31) Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.5.6. *[IMNFLG6]* (Interrupt Monitor Flag Register 6)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	INT192FLG	0	R	INT33 Interrupt detection flag 0: Interrupt not detected 1: Interrupt detected

5.6. NVIC Registers

5.6.1. SysTick Control and Status Register

Bit	Bit Symbol	After Reset	Type	Function
31:17	-	0	R	Read as "0".
16	COUNTFLAG	0	R/W	0: Timer not counted to "0" 1: Timer counted to "0" Returns "1" if timer counted to "0" since last time this was read. Clears on read of any part of the SysTick Control and Status Register.
15:3	-	0	R	Read as "0".
2	CLKSOURCE	0	R/W	0: External reference clock (fosc/64) 1: CPU clock(fsys)
1	TICKINT	0	R/W	0: Do not pend SysTick exception 1: Pend SysTick exception
0	ENABLE	0	R/W	0: Disable 1: Enable If this bit is set to "1", the value of the Reload Value Register is loaded to counter and count starts.

5.6.2. SysTick Reload Value Register

Bit	Bit Symbol	After Reset	Type	Function
31:24	-	0	R	Read as "0".
23:0	RELOAD[23:0]	Undefined	R/W	Reload value Set the value to load into the SysTick Current Value Register when the timer reaches "0".

5.6.3. SysTick Current Value Register

Bit	Bit Symbol	After Reset	Type	Function
31:24	-	0	R	Read as "0".
23:0	CURRENT[23:0]	Undefined	R	Current SysTick timer value
			W	Clear Writing to this register with any value clears it to 0. Clearing this register also clears the <COUNTFLAG> bit of the SysTick Control and Status Register.

5.6.4. SysTick Calibration Value Register

Bit	Bit Symbol	After Reset	Type	Function
31	NOREF	0	R	0: Reference clock provided 1: No reference clock
30	SKEW	1	R	0: Calibration value is 10ms. 1: Calibration value is not 10ms.
29:24	-	0	R	Read as "0".
23:0	TENMS	0x000000	R	Calibration value (Note)

Note: This product does not prepare the calibration value.

5.6.5. Interrupt Control Registers

Following four registers will be used to control each interrupt factor; Interrupt Set-Enable Register, Interrupt Clear-Enable Register, Interrupt Set-Pending Register, and Interrupt Clear-Pending Register.

Each bit corresponds to specified interrupt.

5.6.5.1. Interrupt Set-Enable Register

Each bit corresponds to the specified number of interrupt. It can enable interrupts and check if interrupts are enabled.

Writing "1" to a bit in this register enables the corresponding interrupt.

Writing "0" has no effect.

Reading the bits can see the enable/disable condition of the corresponding interrupts. Writing "1" to a corresponding bit in the Interrupt Clear-Enable Register clears the bit in this register.

(a) Interrupt Set-Enable Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt31)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt30)	0		
29	SETENA (Interrupt29)	0		
28	SETENA (Interrupt28)	0		
27	SETENA (Interrupt27)	0		
26	SETENA (Interrupt26)	0		
25	SETENA (Interrupt25)	0		
24	SETENA (Interrupt24)	0		
23	SETENA (Interrupt23)	0		
22	SETENA (Interrupt22)	0		
21	SETENA (Interrupt21)	0		
20	SETENA (Interrupt20)	0		
19	SETENA (Interrupt19)	0		
18	SETENA (Interrupt18)	0		
17	SETENA (Interrupt17)	0		
16	SETENA (Interrupt16)	0		
15	SETENA (Interrupt15)	0		
14	SETENA (Interrupt14)	0		
13	SETENA (Interrupt13)	0		
12	SETENA (Interrupt12)	0		
11	SETENA (Interrupt11)	0		
10	SETENA (Interrupt10)	0		
9	SETENA (Interrupt9)	0		
8	SETENA (Interrupt8)	0		
7	SETENA (Interrupt7)	0		
6	SETENA (Interrupt6)	0		
5	SETENA (Interrupt5)	0		
4	SETENA (Interrupt4)	0		
3	SETENA (Interrupt3)	0		
2	SETENA (Interrupt2)	0		
1	SETENA (Interrupt1)	0		
0	SETENA (Interrupt0)	0		

(b) Interrupt Set-Enable Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt63)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt62)	0		
29	SETENA (Interrupt61)	0		
28	SETENA (Interrupt60)	0		
27	SETENA (Interrupt59)	0		
26	SETENA (Interrupt58)	0		
25	SETENA (Interrupt57)	0		
24	SETENA (Interrupt56)	0		
23	SETENA (Interrupt55)	0		
22	SETENA (Interrupt54)	0		
21	SETENA (Interrupt53)	0		
20	SETENA (Interrupt52)	0		
19	SETENA (Interrupt51)	0		
18	SETENA (Interrupt50)	0		
17	SETENA (Interrupt49)	0		
16	SETENA (Interrupt48)	0		
15	SETENA (Interrupt47)	0		
14	SETENA (Interrupt46)	0		
13	SETENA (Interrupt45)	0		
12	SETENA (Interrupt44)	0		
11	SETENA (Interrupt43)	0		
10	SETENA (Interrupt42)	0		
9	SETENA (Interrupt41)	0		
8	SETENA (Interrupt40)	0		
7	SETENA (Interrupt39)	0		
6	SETENA (Interrupt38)	0		
5	SETENA (Interrupt37)	0		
4	SETENA (Interrupt36)	0		
3	SETENA (Interrupt35)	0		
2	SETENA (Interrupt34)	0		
1	SETENA (Interrupt33)	0		
0	SETENA (Interrupt32)	0		

(c) Interrupt Set-Enable Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt95)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt94)	0		
29	SETENA (Interrupt93)	0		
28	SETENA (Interrupt92)	0		
27	SETENA (Interrupt91)	0		
26	SETENA (Interrupt90)	0		
25	SETENA (Interrupt89)	0		
24	SETENA (Interrupt88)	0		
23	SETENA (Interrupt87)	0		
22	SETENA (Interrupt86)	0		
21	SETENA (Interrupt85)	0		
20	SETENA (Interrupt84)	0		
19	SETENA (Interrupt83)	0		
18	SETENA (Interrupt82)	0		
17	SETENA (Interrupt81)	0		
16	SETENA (Interrupt80)	0		
15	SETENA (Interrupt79)	0		
14	SETENA (Interrupt78)	0		
13	SETENA (Interrupt77)	0		
12	SETENA (Interrupt76)	0		
11	SETENA (Interrupt75)	0		
10	SETENA (Interrupt74)	0		
9	SETENA (Interrupt73)	0		
8	SETENA (Interrupt72)	0		
7	SETENA (Interrupt71)	0		
6	SETENA (Interrupt70)	0		
5	SETENA (Interrupt69)	0		
4	SETENA (Interrupt68)	0		
3	SETENA (Interrupt67)	0		
2	SETENA (Interrupt66)	0		
1	SETENA (Interrupt65)	0		
0	SETENA (Interrupt64)	0		

(d) Interrupt Set-Enable Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt127)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt126)	0		
29	SETENA (Interrupt125)	0		
28	SETENA (Interrupt124)	0		
27	SETENA (Interrupt123)	0		
26	SETENA (Interrupt122)	0		
25	SETENA (Interrupt121)	0		
24	SETENA (Interrupt120)	0		
23	SETENA (Interrupt119)	0		
22	SETENA (Interrupt118)	0		
21	SETENA (Interrupt117)	0		
20	SETENA (Interrupt116)	0		
19	SETENA (Interrupt115)	0		
18	SETENA (Interrupt114)	0		
17	SETENA (Interrupt113)	0		
16	SETENA (Interrupt112)	0		
15	SETENA (Interrupt111)	0		
14	SETENA (Interrupt110)	0		
13	SETENA (Interrupt109)	0		
12	SETENA (Interrupt108)	0		
11	SETENA (Interrupt107)	0		
10	SETENA (Interrupt106)	0		
9	SETENA (Interrupt105)	0		
8	SETENA (Interrupt104)	0		
7	SETENA (Interrupt103)	0		
6	SETENA (Interrupt102)	0		
5	SETENA (Interrupt101)	0		
4	SETENA (Interrupt100)	0		
3	SETENA (Interrupt99)	0		
2	SETENA (Interrupt98)	0		
1	SETENA (Interrupt97)	0		
0	SETENA (Interrupt96)	0		

(e) Interrupt Set-Enable Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	SETENA (Interrupt159)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	SETENA (Interrupt158)	0		
29	SETENA (Interrupt157)	0		
28	SETENA (Interrupt156)	0		
27	SETENA (Interrupt155)	0		
26	SETENA (Interrupt154)	0		
25	SETENA (Interrupt153)	0		
24	SETENA (Interrupt152)	0		
23	SETENA (Interrupt151)	0		
22	SETENA (Interrupt150)	0		
21	SETENA (Interrupt149)	0		
20	SETENA (Interrupt148)	0		
19	SETENA (Interrupt147)	0		
18	SETENA (Interrupt146)	0		
17	SETENA (Interrupt145)	0		
16	SETENA (Interrupt144)	0		
15	SETENA (Interrupt143)	0		
14	SETENA (Interrupt142)	0		
13	SETENA (Interrupt141)	0		
12	SETENA (Interrupt140)	0		
11	SETENA (Interrupt139)	0		
10	SETENA (Interrupt138)	0		
9	SETENA (Interrupt137)	0		
8	SETENA (Interrupt136)	0		
7	SETENA (Interrupt135)	0		
6	SETENA (Interrupt134)	0		
5	SETENA (Interrupt133)	0		
4	SETENA (Interrupt132)	0		
3	SETENA (Interrupt131)	0		
2	SETENA (Interrupt130)	0		
1	SETENA (Interrupt129)	0		
0	SETENA (Interrupt128)	0		

(f) Interrupt Set-Enable Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:14	-	0	R	Read as "0".
13	SETENA (Interrupt173)	0	R/W	[Write] 1: Enable interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
12	SETENA (Interrupt172)	0		
11	SETENA (Interrupt171)	0		
10	SETENA (Interrupt170)	0		
9	SETENA (Interrupt169)	0		
8	SETENA (Interrupt168)	0		
7	SETENA (Interrupt167)	0		
6	SETENA (Interrupt166)	0		
5	SETENA (Interrupt165)	0		
4	SETENA (Interrupt164)	0		
3	SETENA (Interrupt163)	0		
2	SETENA (Interrupt162)	0		
1	SETENA (Interrupt161)	0		
0	SETENA (Interrupt160)	0		

5.6.5.2. Interrupt Clear-Enable Register

Each bit corresponds to the specified number of interrupt. It can disable interrupts and check if interrupts are disabled.

Writing "1" to a bit in this register disables the corresponding interrupt.

Writing "0" has no effect.

Reading the bits can see the enable/disable condition of the corresponding interrupts.

(a) Interrupt Clear-Enable Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt31)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt30)	0		
29	CLRENA (Interrupt29)	0		
28	CLRENA (Interrupt28)	0		
27	CLRENA (Interrupt27)	0		
26	CLRENA (Interrupt26)	0		
25	CLRENA (Interrupt25)	0		
24	CLRENA (Interrupt24)	0		
23	CLRENA (Interrupt23)	0		
22	CLRENA (Interrupt22)	0		
21	CLRENA (Interrupt21)	0		
20	CLRENA (Interrupt20)	0		
19	CLRENA (Interrupt19)	0		
18	CLRENA (Interrupt18)	0		
17	CLRENA (Interrupt17)	0		
16	CLRENA (Interrupt16)	0		
15	CLRENA (Interrupt15)	0		
14	CLRENA (Interrupt14)	0		
13	CLRENA (Interrupt13)	0		
12	CLRENA (Interrupt12)	0		
11	CLRENA (Interrupt11)	0		
10	CLRENA (Interrupt10)	0		
9	CLRENA (Interrupt9)	0		
8	CLRENA (Interrupt8)	0		
7	CLRENA (Interrupt7)	0		
6	CLRENA (Interrupt6)	0		
5	CLRENA (Interrupt5)	0		
4	CLRENA (Interrupt4)	0		
3	CLRENA (Interrupt3)	0		
2	CLRENA (Interrupt2)	0		
1	CLRENA (Interrupt1)	0		
0	CLRENA (Interrupt0)	0		

(b) Interrupt Clear-Enable Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt63)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt62)	0		
29	CLRENA (Interrupt61)	0		
28	CLRENA (Interrupt60)	0		
27	CLRENA (Interrupt59)	0		
26	CLRENA (Interrupt58)	0		
25	CLRENA (Interrupt57)	0		
24	CLRENA (Interrupt56)	0		
23	CLRENA (Interrupt55)	0		
22	CLRENA (Interrupt54)	0		
21	CLRENA (Interrupt53)	0		
20	CLRENA (Interrupt52)	0		
19	CLRENA (Interrupt51)	0		
18	CLRENA (Interrupt50)	0		
17	CLRENA (Interrupt49)	0		
16	CLRENA (Interrupt48)	0		
15	CLRENA (Interrupt47)	0		
14	CLRENA (Interrupt46)	0		
13	CLRENA (Interrupt45)	0		
12	CLRENA (Interrupt44)	0		
11	CLRENA (Interrupt43)	0		
10	CLRENA (Interrupt42)	0		
9	CLRENA (Interrupt41)	0		
8	CLRENA (Interrupt40)	0		
7	CLRENA (Interrupt39)	0		
6	CLRENA (Interrupt38)	0		
5	CLRENA (Interrupt37)	0		
4	CLRENA (Interrupt36)	0		
3	CLRENA (Interrupt35)	0		
2	CLRENA (Interrupt34)	0		
1	CLRENA (Interrupt33)	0		
0	CLRENA (Interrupt32)	0		

(c) Interrupt Clear-Enable Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt95)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt94)	0		
29	CLRENA (Interrupt93)	0		
28	CLRENA (Interrupt92)	0		
27	CLRENA (Interrupt91)	0		
26	CLRENA (Interrupt90)	0		
25	CLRENA (Interrupt89)	0		
24	CLRENA (Interrupt88)	0		
23	CLRENA (Interrupt87)	0		
22	CLRENA (Interrupt86)	0		
21	CLRENA (Interrupt85)	0		
20	CLRENA (Interrupt84)	0		
19	CLRENA (Interrupt83)	0		
18	CLRENA (Interrupt82)	0		
17	CLRENA (Interrupt81)	0		
16	CLRENA (Interrupt80)	0		
15	CLRENA (Interrupt79)	0		
14	CLRENA (Interrupt78)	0		
13	CLRENA (Interrupt77)	0		
12	CLRENA (Interrupt76)	0		
11	CLRENA (Interrupt75)	0		
10	CLRENA (Interrupt74)	0		
9	CLRENA (Interrupt73)	0		
8	CLRENA (Interrupt72)	0		
7	CLRENA (Interrupt71)	0		
6	CLRENA (Interrupt70)	0		
5	CLRENA (Interrupt69)	0		
4	CLRENA (Interrupt68)	0		
3	CLRENA (Interrupt67)	0		
2	CLRENA (Interrupt66)	0		
1	CLRENA (Interrupt65)	0		
0	CLRENA (Interrupt64)	0		

(d) Interrupt Clear-Enable Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt127)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt126)	0		
29	CLRENA (Interrupt125)	0		
28	CLRENA (Interrupt124)	0		
27	CLRENA (Interrupt123)	0		
26	CLRENA (Interrupt122)	0		
25	CLRENA (Interrupt121)	0		
24	CLRENA (Interrupt120)	0		
23	CLRENA (Interrupt119)	0		
22	CLRENA (Interrupt118)	0		
21	CLRENA (Interrupt117)	0		
20	CLRENA (Interrupt116)	0		
19	CLRENA (Interrupt115)	0		
18	CLRENA (Interrupt114)	0		
17	CLRENA (Interrupt113)	0		
16	CLRENA (Interrupt112)	0		
15	CLRENA (Interrupt111)	0		
14	CLRENA (Interrupt110)	0		
13	CLRENA (Interrupt109)	0		
12	CLRENA (Interrupt108)	0		
11	CLRENA (Interrupt107)	0		
10	CLRENA (Interrupt106)	0		
9	CLRENA (Interrupt105)	0		
8	CLRENA (Interrupt104)	0		
7	CLRENA (Interrupt103)	0		
6	CLRENA (Interrupt102)	0		
5	CLRENA (Interrupt101)	0		
4	CLRENA (Interrupt100)	0		
3	CLRENA (Interrupt99)	0		
2	CLRENA (Interrupt98)	0		
1	CLRENA (Interrupt97)	0		
0	CLRENA (Interrupt96)	0		

(e) Interrupt Clear-Enable Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	CLRENA (Interrupt159)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
30	CLRENA (Interrupt158)	0		
29	CLRENA (Interrupt157)	0		
28	CLRENA (Interrupt156)	0		
27	CLRENA (Interrupt155)	0		
26	CLRENA (Interrupt154)	0		
25	CLRENA (Interrupt153)	0		
24	CLRENA (Interrupt152)	0		
23	CLRENA (Interrupt151)	0		
22	CLRENA (Interrupt150)	0		
21	CLRENA (Interrupt149)	0		
20	CLRENA (Interrupt148)	0		
19	CLRENA (Interrupt147)	0		
18	CLRENA (Interrupt146)	0		
17	CLRENA (Interrupt145)	0		
16	CLRENA (Interrupt144)	0		
15	CLRENA (Interrupt143)	0		
14	CLRENA (Interrupt142)	0		
13	CLRENA (Interrupt141)	0		
12	CLRENA (Interrupt140)	0		
11	CLRENA (Interrupt139)	0		
10	CLRENA (Interrupt138)	0		
9	CLRENA (Interrupt137)	0		
8	CLRENA (Interrupt136)	0		
7	CLRENA (Interrupt135)	0		
6	CLRENA (Interrupt134)	0		
5	CLRENA (Interrupt133)	0		
4	CLRENA (Interrupt132)	0		
3	CLRENA (Interrupt131)	0		
2	CLRENA (Interrupt130)	0		
1	CLRENA (Interrupt129)	0		
0	CLRENA (Interrupt128)	0		

(f) Interrupt Clear-Enable Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:14	-	0	R	Read as "0".
13	CLRENA (Interrupt173)	0	R/W	[Write] 1: Disable Interrupt [Read] 0: Interrupt is disabled 1: Interrupt is enabled
12	CLRENA (Interrupt172)	0		
11	CLRENA (Interrupt171)	0		
10	CLRENA (Interrupt170)	0		
9	CLRENA (Interrupt169)	0		
8	CLRENA (Interrupt168)	0		
7	CLRENA (Interrupt167)	0		
6	CLRENA (Interrupt166)	0		
5	CLRENA (Interrupt165)	0		
4	CLRENA (Interrupt164)	0		
3	CLRENA (Interrupt163)	0		
2	CLRENA (Interrupt162)	0		
1	CLRENA (Interrupt161)	0		
0	CLRENA (Interrupt160)	0		

5.6.5.3. Interrupt Set-Pending Register

Each bit corresponds to the specified number of interrupt. It can force interrupts into the pending state and determines which interrupts are currently pending.

Writing "1" to a bit in this register pends the corresponding interrupt. However, writing "1" has no effect on an interrupt that is already pending or is disabled.

Writing "0" has no effect.

Reading the bit returns the current state of the corresponding interrupt.

Writing "1" to a corresponding bit in the Interrupt Clear-Pending Register clears the bit in this register.

(a) Interrupt Set-Pending Register 0

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt31)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt30)	Undefined		
29	SETPEND (Interrupt29)	Undefined		
28	SETPEND (Interrupt28)	Undefined		
27	SETPEND (Interrupt27)	Undefined		
26	SETPEND (Interrupt26)	Undefined		
25	SETPEND (Interrupt25)	Undefined		
24	SETPEND (Interrupt24)	Undefined		
23	SETPEND (Interrupt23)	Undefined		
22	SETPEND (Interrupt22)	Undefined		
21	SETPEND (Interrupt21)	Undefined		
20	SETPEND (Interrupt20)	Undefined		
19	SETPEND (Interrupt19)	Undefined		
18	SETPEND (Interrupt18)	Undefined		
17	SETPEND (Interrupt17)	Undefined		
16	SETPEND (Interrupt16)	Undefined		
15	SETPEND (Interrupt15)	Undefined		
14	SETPEND (Interrupt14)	Undefined		
13	SETPEND (Interrupt13)	Undefined		
12	SETPEND (Interrupt12)	Undefined		
11	SETPEND (Interrupt11)	Undefined		
10	SETPEND (Interrupt10)	Undefined		
9	SETPEND (Interrupt9)	Undefined		
8	SETPEND (Interrupt8)	Undefined		
7	SETPEND (Interrupt7)	Undefined		
6	SETPEND (Interrupt6)	Undefined		
5	SETPEND (Interrupt5)	Undefined		
4	SETPEND (Interrupt4)	Undefined		
3	SETPEND (Interrupt3)	Undefined		
2	SETPEND (Interrupt2)	Undefined		
1	SETPEND (Interrupt1)	Undefined		
0	SETPEND (Interrupt0)	Undefined		

(b) Interrupt Set-Pending Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt63)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt62)	Undefined		
29	SETPEND (Interrupt61)	Undefined		
28	SETPEND (Interrupt60)	Undefined		
27	SETPEND (Interrupt59)	Undefined		
26	SETPEND (Interrupt58)	Undefined		
25	SETPEND (Interrupt57)	Undefined		
24	SETPEND (Interrupt56)	Undefined		
23	SETPEND (Interrupt55)	Undefined		
22	SETPEND (Interrupt54)	Undefined		
21	SETPEND (Interrupt53)	Undefined		
20	SETPEND (Interrupt52)	Undefined		
19	SETPEND (Interrupt51)	Undefined		
18	SETPEND (Interrupt50)	Undefined		
17	SETPEND (Interrupt49)	Undefined		
16	SETPEND (Interrupt48)	Undefined		
15	SETPEND (Interrupt47)	Undefined		
14	SETPEND (Interrupt46)	Undefined		
13	SETPEND (Interrupt45)	Undefined		
12	SETPEND (Interrupt44)	Undefined		
11	SETPEND (Interrupt43)	Undefined		
10	SETPEND (Interrupt42)	Undefined		
9	SETPEND (Interrupt41)	Undefined		
8	SETPEND (Interrupt40)	Undefined		
7	SETPEND (Interrupt39)	Undefined		
6	SETPEND (Interrupt38)	Undefined		
5	SETPEND (Interrupt37)	Undefined		
4	SETPEND (Interrupt36)	Undefined		
3	SETPEND (Interrupt35)	Undefined		
2	SETPEND (Interrupt34)	Undefined		
1	SETPEND (Interrupt33)	Undefined		
0	SETPEND (Interrupt32)	Undefined		

(c) Interrupt Set-Pending Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt95)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt94)	Undefined		
29	SETPEND (Interrupt93)	Undefined		
28	SETPEND (Interrupt92)	Undefined		
27	SETPEND (Interrupt91)	Undefined		
26	SETPEND (Interrupt90)	Undefined		
25	SETPEND (Interrupt89)	Undefined		
24	SETPEND (Interrupt88)	Undefined		
23	SETPEND (Interrupt87)	Undefined		
22	SETPEND (Interrupt86)	Undefined		
21	SETPEND (Interrupt85)	Undefined		
20	SETPEND (Interrupt84)	Undefined		
19	SETPEND (Interrupt83)	Undefined		
18	SETPEND (Interrupt82)	Undefined		
17	SETPEND (Interrupt81)	Undefined		
16	SETPEND (Interrupt80)	Undefined		
15	SETPEND (Interrupt79)	Undefined		
14	SETPEND (Interrupt78)	Undefined		
13	SETPEND (Interrupt77)	Undefined		
12	SETPEND (Interrupt76)	Undefined		
11	SETPEND (Interrupt75)	Undefined		
10	SETPEND (Interrupt74)	Undefined		
9	SETPEND (Interrupt73)	Undefined		
8	SETPEND (Interrupt72)	Undefined		
7	SETPEND (Interrupt71)	Undefined		
6	SETPEND (Interrupt70)	Undefined		
5	SETPEND (Interrupt69)	Undefined		
4	SETPEND (Interrupt68)	Undefined		
3	SETPEND (Interrupt67)	Undefined		
2	SETPEND (Interrupt66)	Undefined		
1	SETPEND (Interrupt65)	Undefined		
0	SETPEND (Interrupt64)	Undefined		

(d) Interrupt Set-Pending Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt127)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt126)	Undefined		
29	SETPEND (Interrupt125)	Undefined		
28	SETPEND (Interrupt124)	Undefined		
27	SETPEND (Interrupt123)	Undefined		
26	SETPEND (Interrupt122)	Undefined		
25	SETPEND (Interrupt121)	Undefined		
24	SETPEND (Interrupt120)	Undefined		
23	SETPEND (Interrupt119)	Undefined		
22	SETPEND (Interrupt118)	Undefined		
21	SETPEND (Interrupt117)	Undefined		
20	SETPEND (Interrupt116)	Undefined		
19	SETPEND (Interrupt115)	Undefined		
18	SETPEND (Interrupt114)	Undefined		
17	SETPEND (Interrupt113)	Undefined		
16	SETPEND (Interrupt112)	Undefined		
15	SETPEND (Interrupt111)	Undefined		
14	SETPEND (Interrupt110)	Undefined		
13	SETPEND (Interrupt109)	Undefined		
12	SETPEND (Interrupt108)	Undefined		
11	SETPEND (Interrupt107)	Undefined		
10	SETPEND (Interrupt106)	Undefined		
9	SETPEND (Interrupt105)	Undefined		
8	SETPEND (Interrupt104)	Undefined		
7	SETPEND (Interrupt103)	Undefined		
6	SETPEND (Interrupt102)	Undefined		
5	SETPEND (Interrupt101)	Undefined		
4	SETPEND (Interrupt100)	Undefined		
3	SETPEND (Interrupt99)	Undefined		
2	SETPEND (Interrupt98)	Undefined		
1	SETPEND (Interrupt97)	Undefined		
0	SETPEND (Interrupt96)	Undefined		

(e) Interrupt Set-Pending Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	SETPEND (Interrupt159)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
30	SETPEND (Interrupt158)	Undefined		
29	SETPEND (Interrupt157)	Undefined		
28	SETPEND (Interrupt156)	Undefined		
27	SETPEND (Interrupt155)	Undefined		
26	SETPEND (Interrupt154)	Undefined		
25	SETPEND (Interrupt153)	Undefined		
24	SETPEND (Interrupt152)	Undefined		
23	SETPEND (Interrupt151)	Undefined		
22	SETPEND (Interrupt150)	Undefined		
21	SETPEND (Interrupt149)	Undefined		
20	SETPEND (Interrupt148)	Undefined		
19	SETPEND (Interrupt147)	Undefined		
18	SETPEND (Interrupt146)	Undefined		
17	SETPEND (Interrupt145)	Undefined		
16	SETPEND (Interrupt144)	Undefined		
15	SETPEND (Interrupt143)	Undefined		
14	SETPEND (Interrupt142)	Undefined		
13	SETPEND (Interrupt141)	Undefined		
12	SETPEND (Interrupt140)	Undefined		
11	SETPEND (Interrupt139)	Undefined		
10	SETPEND (Interrupt138)	Undefined		
9	SETPEND (Interrupt137)	Undefined		
8	SETPEND (Interrupt136)	Undefined		
7	SETPEND (Interrupt135)	Undefined		
6	SETPEND (Interrupt134)	Undefined		
5	SETPEND (Interrupt133)	Undefined		
4	SETPEND (Interrupt132)	Undefined		
3	SETPEND (Interrupt131)	Undefined		
2	SETPEND (Interrupt130)	Undefined		
1	SETPEND (Interrupt129)	Undefined		
0	SETPEND (Interrupt128)	Undefined		

(f) Interrupt Set-Pending Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:14	-	0	R	Read as "0".
13	SETPEND (Interrupt173)	Undefined	R/W	[Write] 1: Pend interrupt [Read] 0: Not pending 1: Pending
12	SETPEND (Interrupt172)	Undefined		
11	SETPEND (Interrupt171)	Undefined		
10	SETPEND (Interrupt170)	Undefined		
9	SETPEND (Interrupt169)	Undefined		
8	SETPEND (Interrupt168)	Undefined		
7	SETPEND (Interrupt167)	Undefined		
6	SETPEND (Interrupt166)	Undefined		
5	SETPEND (Interrupt165)	Undefined		
4	SETPEND (Interrupt164)	Undefined		
3	SETPEND (Interrupt163)	Undefined		
2	SETPEND (Interrupt162)	Undefined		
1	SETPEND (Interrupt161)	Undefined		
0	SETPEND (Interrupt160)	Undefined		

5.6.5.4. Interrupt Clear-Pending Register

Each bit corresponds to the specified number of interrupt. It can clear pending interrupts and determines which interrupts are currently pending.

Writing "1" to a bit in this register clears the corresponding pending interrupt. However, writing "1" has no effect on an interrupt that is already being serviced. Writing "0" has no effect.

Reading the bit returns the current state of the corresponding interrupt.

(a) Interrupt Clear-Pending Register 0

Bit	Bit Symbol	After Reset	Type	function
31	CLRPEND (Interrupt31)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt30)	Undefined		
29	CLRPEND (Interrupt29)	Undefined		
28	CLRPEND (Interrupt28)	Undefined		
27	CLRPEND (Interrupt27)	Undefined		
26	CLRPEND (Interrupt26)	Undefined		
25	CLRPEND (Interrupt25)	Undefined		
24	CLRPEND (Interrupt24)	Undefined		
23	CLRPEND (Interrupt23)	Undefined		
22	CLRPEND (Interrupt22)	Undefined		
21	CLRPEND (Interrupt21)	Undefined		
20	CLRPEND (Interrupt20)	Undefined		
19	CLRPEND (Interrupt19)	Undefined		
18	CLRPEND (Interrupt18)	Undefined		
17	CLRPEND (Interrupt17)	Undefined		
16	CLRPEND (Interrupt16)	Undefined		
15	CLRPEND (Interrupt15)	Undefined		
14	CLRPEND (Interrupt14)	Undefined		
13	CLRPEND (Interrupt13)	Undefined		
12	CLRPEND (Interrupt12)	Undefined		
11	CLRPEND (Interrupt11)	Undefined		
10	CLRPEND (Interrupt10)	Undefined		
9	CLRPEND (Interrupt9)	Undefined		
8	CLRPEND (Interrupt8)	Undefined		
7	CLRPEND (Interrupt7)	Undefined		
6	CLRPEND (Interrupt6)	Undefined		
5	CLRPEND (Interrupt5)	Undefined		
4	CLRPEND (Interrupt4)	Undefined		
3	CLRPEND (Interrupt3)	Undefined		
2	CLRPEND (Interrupt2)	Undefined		
1	CLRPEND (Interrupt1)	Undefined		
0	CLRPEND (Interrupt0)	Undefined		

(b) Interrupt Clear-Pending Register 1

Bit	Bit Symbol	After Reset	Type	Function
31	CLRPEND (Interrupt63)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt62)	Undefined		
29	CLRPEND (Interrupt61)	Undefined		
28	CLRPEND (Interrupt60)	Undefined		
27	CLRPEND (Interrupt59)	Undefined		
26	CLRPEND (Interrupt58)	Undefined		
25	CLRPEND (Interrupt57)	Undefined		
24	CLRPEND (Interrupt56)	Undefined		
23	CLRPEND (Interrupt55)	Undefined		
22	CLRPEND (Interrupt54)	Undefined		
21	CLRPEND (Interrupt53)	Undefined		
20	CLRPEND (Interrupt52)	Undefined		
19	CLRPEND (Interrupt51)	Undefined		
18	CLRPEND (Interrupt50)	Undefined		
17	CLRPEND (Interrupt49)	Undefined		
16	CLRPEND (Interrupt48)	Undefined		
15	CLRPEND (Interrupt47)	Undefined		
14	CLRPEND (Interrupt46)	Undefined		
13	CLRPEND (Interrupt45)	Undefined		
12	CLRPEND (Interrupt44)	Undefined		
11	CLRPEND (Interrupt43)	Undefined		
10	CLRPEND (Interrupt42)	Undefined		
9	CLRPEND (Interrupt41)	Undefined		
8	CLRPEND (Interrupt40)	Undefined		
7	CLRPEND (Interrupt39)	Undefined		
6	CLRPEND (Interrupt38)	Undefined		
5	CLRPEND (Interrupt37)	Undefined		
4	CLRPEND (Interrupt36)	Undefined		
3	CLRPEND (Interrupt35)	Undefined		
2	CLRPEND (Interrupt34)	Undefined		
1	CLRPEND (Interrupt33)	Undefined		
0	CLRPEND (Interrupt32)	Undefined		

(c) Interrupt Clear-Pending Register 2

Bit	Bit Symbol	After Reset	Type	Function
31	CLRPEND (Interrupt95)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt94)	Undefined		
29	CLRPEND (Interrupt93)	Undefined		
28	CLRPEND (Interrupt92)	Undefined		
27	CLRPEND (Interrupt91)	Undefined		
26	CLRPEND (Interrupt90)	Undefined		
25	CLRPEND (Interrupt89)	Undefined		
24	CLRPEND (Interrupt88)	Undefined		
23	CLRPEND (Interrupt87)	Undefined		
22	CLRPEND (Interrupt86)	Undefined		
21	CLRPEND (Interrupt85)	Undefined		
20	CLRPEND (Interrupt84)	Undefined		
19	CLRPEND (Interrupt83)	Undefined		
18	CLRPEND (Interrupt82)	Undefined		
17	CLRPEND (Interrupt81)	Undefined		
16	CLRPEND (Interrupt80)	Undefined		
15	CLRPEND (Interrupt79)	Undefined		
14	CLRPEND (Interrupt78)	Undefined		
13	CLRPEND (Interrupt77)	Undefined		
12	CLRPEND (Interrupt76)	Undefined		
11	CLRPEND (Interrupt75)	Undefined		
10	CLRPEND (Interrupt74)	Undefined		
9	CLRPEND (Interrupt73)	Undefined		
8	CLRPEND (Interrupt72)	Undefined		
7	CLRPEND (Interrupt71)	Undefined		
6	CLRPEND (Interrupt70)	Undefined		
5	CLRPEND (Interrupt69)	Undefined		
4	CLRPEND (Interrupt68)	Undefined		
3	CLRPEND (Interrupt67)	Undefined		
2	CLRPEND (Interrupt66)	Undefined		
1	CLRPEND (Interrupt65)	Undefined		
0	CLRPEND (Interrupt64)	Undefined		

(d) Interrupt Clear-Pending Register 3

Bit	Bit Symbol	After Reset	Type	Function
31	CLRPEND (Interrupt127)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt126)	Undefined		
29	CLRPEND (Interrupt125)	Undefined		
28	CLRPEND (Interrupt124)	Undefined		
27	CLRPEND (Interrupt123)	Undefined		
26	CLRPEND (Interrupt122)	Undefined		
25	CLRPEND (Interrupt121)	Undefined		
24	CLRPEND (Interrupt120)	Undefined		
23	CLRPEND (Interrupt119)	Undefined		
22	CLRPEND (Interrupt118)	Undefined		
21	CLRPEND (Interrupt117)	Undefined		
20	CLRPEND (Interrupt116)	Undefined		
19	CLRPEND (Interrupt115)	Undefined		
18	CLRPEND (Interrupt114)	Undefined		
17	CLRPEND (Interrupt113)	Undefined		
16	CLRPEND (Interrupt112)	Undefined		
15	CLRPEND (Interrupt111)	Undefined		
14	CLRPEND (Interrupt110)	Undefined		
13	CLRPEND (Interrupt109)	Undefined		
12	CLRPEND (Interrupt108)	Undefined		
11	CLRPEND (Interrupt107)	Undefined		
10	CLRPEND (Interrupt106)	Undefined		
9	CLRPEND (Interrupt105)	Undefined		
8	CLRPEND (Interrupt104)	Undefined		
7	CLRPEND (Interrupt103)	Undefined		
6	CLRPEND (Interrupt102)	Undefined		
5	CLRPEND (Interrupt101)	Undefined		
4	CLRPEND (Interrupt100)	Undefined		
3	CLRPEND (Interrupt99)	Undefined		
2	CLRPEND (Interrupt98)	Undefined		
1	CLRPEND (Interrupt97)	Undefined		
0	CLRPEND (Interrupt96)	Undefined		

(e) Interrupt Clear-Pending Register 4

Bit	Bit Symbol	After Reset	Type	Function
31	CLRPEND (Interrupt159)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
30	CLRPEND (Interrupt158)	Undefined		
29	CLRPEND (Interrupt157)	Undefined		
28	CLRPEND (Interrupt156)	Undefined		
27	CLRPEND (Interrupt155)	Undefined		
26	CLRPEND (Interrupt154)	Undefined		
25	CLRPEND (Interrupt153)	Undefined		
24	CLRPEND (Interrupt152)	Undefined		
23	CLRPEND (Interrupt151)	Undefined		
22	CLRPEND (Interrupt150)	Undefined		
21	CLRPEND (Interrupt149)	Undefined		
20	CLRPEND (Interrupt148)	Undefined		
19	CLRPEND (Interrupt147)	Undefined		
18	CLRPEND (Interrupt146)	Undefined		
17	CLRPEND (Interrupt145)	Undefined		
16	CLRPEND (Interrupt144)	Undefined		
15	CLRPEND (Interrupt143)	Undefined		
14	CLRPEND (Interrupt142)	Undefined		
13	CLRPEND (Interrupt141)	Undefined		
12	CLRPEND (Interrupt140)	Undefined		
11	CLRPEND (Interrupt139)	Undefined		
10	CLRPEND (Interrupt138)	Undefined		
9	CLRPEND (Interrupt137)	Undefined		
8	CLRPEND (Interrupt136)	Undefined		
7	CLRPEND (Interrupt135)	Undefined		
6	CLRPEND (Interrupt134)	Undefined		
5	CLRPEND (Interrupt133)	Undefined		
4	CLRPEND (Interrupt132)	Undefined		
3	CLRPEND (Interrupt131)	Undefined		
2	CLRPEND (Interrupt130)	Undefined		
1	CLRPEND (Interrupt129)	Undefined		
0	CLRPEND (Interrupt128)	Undefined		

(f) Interrupt Clear-Pending Register 5

Bit	Bit Symbol	After Reset	Type	Function
31:14	-	0	R	Read as "0".
13	CLRPEND (Interrupt173)	Undefined	R/W	[Write] 1: Clear pending interrupt [Read] 0: Not pending 1: Pending
12	CLRPEND (Interrupt172)	Undefined		
11	CLRPEND (Interrupt171)	Undefined		
10	CLRPEND (Interrupt170)	Undefined		
9	CLRPEND (Interrupt169)	Undefined		
8	CLRPEND (Interrupt168)	Undefined		
7	CLRPEND (Interrupt167)	Undefined		
6	CLRPEND (Interrupt166)	Undefined		
5	CLRPEND (Interrupt165)	Undefined		
4	CLRPEND (Interrupt164)	Undefined		
3	CLRPEND (Interrupt163)	Undefined		
2	CLRPEND (Interrupt162)	Undefined		
1	CLRPEND (Interrupt161)	Undefined		
0	CLRPEND (Interrupt160)	Undefined		

5.6.6. Interrupt Priority Register

Each interrupt is provided with eight bits of an Interrupt Priority Register.
The following shows the addresses of the Interrupt Priority Registers corresponding to interrupt numbers.

Address	31 24	23 16	15 8	7 0
0xE000E400	PRI_3	PRI_2	PRI_1	PRI_0
0xE000E404	PRI_7	PRI_6	PRI_5	PRI_4
0xE000E408	PRI_11	PRI_10	PRI_9	PRI_8
0xE000E40C	PRI_15	PRI_14	PRI_13	PRI_12
0xE000E410	PRI_19	PRI_18	PRI_17	PRI_16
0xE000E414	PRI_23	PRI_22	PRI_21	PRI_20
0xE000E418	PRI_27	PRI_26	PRI_25	PRI_24
0xE000E41C	PRI_31	PRI_30	PRI_29	PRI_28
0xE000E420	PRI_35	PRI_34	PRI_33	PRI_32
0xE000E424	PRI_39	PRI_38	PRI_37	PRI_36
0xE000E428	PRI_43	PRI_42	PRI_41	PRI_40
0xE000E42C	PRI_47	PRI_46	PRI_45	PRI_44
0xE000E430	PRI_51	PRI_50	PRI_49	PRI_48
0xE000E434	PRI_55	PRI_54	PRI_53	PRI_52
0xE000E438	PRI_59	PRI_58	PRI_57	PRI_56
0xE000E43C	PRI_63	PRI_62	PRI_61	PRI_60
0xE000E440	PRI_67	PRI_66	PRI_65	PRI_64
0xE000E444	PRI_71	PRI_70	PRI_69	PRI_68
0xE000E448	PRI_75	PRI_74	PRI_73	PRI_72
0xE000E44C	PRI_79	PRI_78	PRI_77	PRI_76
0xE000E450	PRI_83	PRI_82	PRI_81	PRI_80
0xE000E454	PRI_87	PRI_86	PRI_85	PRI_84
0xE000E458	PRI_91	PRI_90	PRI_89	PRI_88
0xE000E45C	PRI_95	PRI_94	PRI_93	PRI_92
0xE000E460	PRI_99	PRI_98	PRI_97	PRI_96
0xE000E464	PRI_103	PRI_102	PRI_101	PRI_100
0xE000E468	PRI_107	PRI_106	PRI_105	PRI_104
0xE000E46C	PRI_111	PRI_110	PRI_109	PRI_108
0xE000E470	PRI_115	PRI_114	PRI_113	PRI_112
0xE000E474	PRI_119	PRI_118	PRI_117	PRI_116
0xE000E478	PRI_123	PRI_122	PRI_121	PRI_120
0xE000E47C	PRI_127	PRI_126	PRI_125	PRI_124
0xE000E480	PRI_131	PRI_130	PRI_129	PRI_128
0xE000E484	PRI_135	PRI_134	PRI_133	PRI_132
0xE000E488	PRI_139	PRI_138	PRI_137	PRI_136
0xE000E48C	PRI_143	PRI_142	PRI_141	PRI_140
0xE000E490	PRI_147	PRI_146	PRI_145	PRI_144
0xE000E494	PRI_151	PRI_150	PRI_149	PRI_148
0xE000E498	PRI_155	PRI_154	PRI_153	PRI_152
0xE000E49C	PRI_159	PRI_158	PRI_157	PRI_156
0xE000E4A0	PRI_163	PRI_162	PRI_161	PRI_160
0xE000E4A4	PRI_167	PRI_166	PRI_165	PRI_164
0xE000E4A8	PRI_171	PRI_170	PRI_169	PRI_168
0xE000E4AC	-	-	PRI_173	PRI_172

The number of bits to be used for assigning a priority varies with each product. This product uses four bits for assigning a priority.

The following shows the fields of the Interrupt Priority Registers for interrupt numbers 0 to 3. The Interrupt Priority Registers for all other interrupt numbers have the identical fields. Unused bits return "0" when read, and writing to unused bits has no effect.

Bit	Bit Symbol	After Reset	Type	Function
31:28	PRI_3[3:0]	0000	R/W	Priority of interrupt number 3
27:24	-	0	R	Read as "0".
23:20	PRI_2[3:0]	0000	R/W	Priority of interrupt number 2
19:16	-	0	R	Read as "0".
15:12	PRI_1[3:0]	0000	R/W	Priority of interrupt number 1
11:8	-	0	R	Read as "0".
7:4	PRI_0[3:0]	0000	R/W	Priority of interrupt number 0
3:0	-	0	R	Read as "0".

5.6.7. Vector Table Offset Register

Bit	Bit Symbol	After Reset	Type	Function
31:7	TBLOFF[24:0]	0x0000000	R/W	Offset value Set the offset value from the address of 0x00000000. The offset must be aligned based on the number of exceptions in the table. This means that the minimum alignment is 32 words that you can use for up to 16 interrupts. For more interrupts, you must adjust the alignment by rounding up to the next power of two.
6:0	-	0	R	Read as "0".

5.6.8. Application Interrupt and Reset Control Register

Bit	Bit Symbol	After Reset	Type	Function
31:16	VECTKEY/ VECTKEYSTAT[15:0]	Undefined	W	Register key Writing to this register requires "0x05FA" in the <VECTKEY> field.
			R	Register key Read as "0xFA05".
15	ENDIANESS	0	R/W	Endianness bit: (Note1) 1: Big endian 0: Little endian
14:11	-	0	R	Read as “0”.
10:8	PRIGROUP[2:0]	000	R/W	Interrupt priority grouping 000: seven bits of pre-emption priority, one bit of sub priority 001: six bits of pre-emption priority, two bits of sub priority 010: five bits of pre-emption priority, three bits of sub priority 011: four bits of pre-emption priority, four bits of sub priority 100: three bits of pre-emption priority, five bits of sub priority 101: two bits of pre-emption priority, six bits of sub priority 110: one bit of pre-emption priority, seven bits of sub priority 111: no pre-emption priority, eight bits of sub priority This field configures to split the interrupt priority register <PRI_n> into pre-emption priority and sub priority.
7:3	-	0	R	Read as "0".
2	SYSRESETREQ	0	R/W	System Reset Request 1: CPU outputs a SYSRESETREQ signal. (Note2)
1	VECTCLRACTIVE	0	R/W	Clear active vector bit 1: clear all state information for active NMI, fault, and interrupts. 0: do not clear. This bit self-clears. It is the responsibility of the application to reinitialize the stack.
0	VECTRESET	0	R/W	System Reset bit 1: reset system. 0: do not reset system. Resets the system, with the exception of debug components (FPB, DWT and ITM) by setting this bit to "1" and this bit is also zero cleared

Note 1: Little-endian is the default memory format for this product.

Note 2: When SYSRESETREQ is output, warm reset is performed on this product. <SYSRESETREQ> is cleared by warm reset.

5.6.9. System Handler Priority Register

Each exception is provided with eight bits of a System Handler Priority Register.
The following shows the addresses of the System Handler Priority Registers corresponding to each exception.

Address	31 24	23 16	15 8	7 0
0xE000ED18	PRI_7	PRI_6 (Usage Fault)	PRI_5 (Bus Fault)	PRI_4 (Memory Management)
0xE000ED1C	PRI_11 (SVCall)	PRI_10	PRI_9	PRI_8
0xE000ED20	PRI_15 (SysTick)	PRI_14 (PendSV)	PRI_13	PRI_12 (Debug Monitor)

The number of bits to be used for assigning a priority varies with each product. This product uses four bits for assigning a priority.

The following shows the fields of the System Handler Priority Registers for Usage Fault, Bus Fault, and Memory Management. Unused bits return "0" when read, and writing to unused bits has no effect.

Bit	Bit Symbol	After Reset	Type	Function
31:28	PRI_7[3:0]	0000	R/W	Reserved
27:24	-	0	R	Read as "0".
23:20	PRI_6[3:0]	0000	R/W	Priority of Usage Fault
19:16	-	0	R	Read as "0".
15:12	PRI_5[3:0]	0000	R/W	Priority of Bus Fault
11:8	-	0	R	Read as "0".
7:4	PRI_4[3:0]	0000	R/W	Priority of Memory Management
3:0	-	0	R	Read as "0".

5.6.10. System Handler Control and State Register

Bit	Bit Symbol	After Reset	Type	Function
31:19	-	0	R	Read as "0".
18	USGFAULTENA	0	R/W	Usage Fault 0: Disabled 1: Enabled
17	BUSFAULTENA	0	R/W	Bus Fault 0: Disabled 1: Enabled
16	MEMFAULTENA	0	R/W	Memory Management 0: Disabled 1: Enabled
15	SVCALLPENDED	0	R/W	SVCall 0: Not pended 1: Pended
14	BUSFAULTPENDED	0	R/W	Bus Fault 0: Not pended 1: Pended
13	MEMFAULTPENDED	0	R/W	Memory Management 0: Not pended 1: Pended
12	USGFAULTPENDED	0	R/W	Usage fault 0: Not pended 1: Pended
11	SYSTICKACT	0	R/W	SysTick 0: Inactive 1: Active
10	PENDSVACT	0	R/W	PendSV 0: Inactive 1: Active
9	-	0	R	Read as "0".
8	MONITORACT	0	R/W	Debug Monitor 0: Inactive 1: Active
7	SVCALLACT	0	R/W	SVCall 0: Inactive 1: Active
6:4	-	0	R	Read as "0".
3	USGFAULTACT	0	R/W	Usage Fault 0: Inactive 1: Active
2	-	0	R	Read as "0".
1	BUSFAULTACT	0	R/W	Bus Fault 0: Inactive 1: Active
0	MEMFAULTACT	0	R/W	Memory Management 0: Inactive 1: Active

Note: You must clear or set the active bits with extreme caution because clearing or setting these bits does not repair stack contents.

6. List of Interrupt Factors for Each Product

6.1. TMPM3HQ,TMPM3HP,TMPM3HN,TMPM3HM,TMPM3HL

Table 6.1 List of interrupt request (1/7)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	✓	NMI	INTLVD	LVD interrupt	***[IANIC00]***	***[IMNFLGNMI]*** <INT000FLG>
						INTWDT0	WDT interrupt	***[IBNIC00]***	***[IMNFLGNMI]*** <INT016FLG>
✓	✓	✓	✓	✓	0	INT00	External interrupt 00	***[IAIMC00]***	***[IMNFLG1]*** <INT032FLG>
✓	✓	✓	✓	✓	1	INT01	External interrupt 01	***[IAIMC01]***	***[IMNFLG1]*** <INT033FLG>
✓	✓	✓	✓	-	2	INT02	External interrupt 02	***[IAIMC02]***	***[IMNFLG1]*** <INT034FLG>
✓	✓	✓	✓	✓	3	INT03	External interrupt 03	***[IBIMC066]***	***[IMNFLG5]*** <INT162FLG>
✓	✓	✓	✓	✓	4	INT04	External interrupt 04	***[IBIMC067]***	***[IMNFLG5]*** <INT163FLG>
✓	✓	✓	✓	✓	5	INT05	External interrupt 05	***[IBIMC068]***	***[IMNFLG5]*** <INT164FLG>
✓	✓	✓	✓	✓	6	INT06	External interrupt 06	***[IBIMC069]***	***[IMNFLG5]*** <INT165FLG>
✓	✓	✓	✓	✓	7	INT07	External interrupt 07	***[IBIMC070]***	***[IMNFLG5]*** <INT166FLG>
✓	✓	✓	✓	✓	8	INT08	External interrupt 08	***[IBIMC071]***	***[IMNFLG5]*** <INT167FLG>
✓	✓	✓	✓	-	9	INT09	External interrupt 09	***[IBIMC072]***	***[IMNFLG5]*** <INT168FLG>
✓	✓	✓	✓	✓	10	INT10	External interrupt 10	***[IBIMC073]***	***[IMNFLG5]*** <INT169FLG>
✓	✓	✓	✓	✓	11	INT11	External interrupt 11	***[IBIMC074]***	***[IMNFLG5]*** <INT170FLG>
✓	✓	✓	✓	✓	12	INT12	External interrupt 12	***[IBIMC075]***	***[IMNFLG5]*** <INT171FLG>
✓	✓	✓	✓	-	13	INT13	External interrupt 13	***[IAIMC03]***	***[IMNFLG1]*** <INT035FLG>
✓	✓	✓	✓	✓	14	INT14	External interrupt 14	***[IBIMC076]***	***[IMNFLG5]*** <INT172FLG>
✓	✓	✓	-	-	15	INT15	External interrupt 15	***[IBIMC077]***	***[IMNFLG5]*** <INT173FLG>
✓	✓	✓	-	-	16	INT16	External interrupt 16	***[IBIMC078]***	***[IMNFLG5]*** <INT174FLG>
✓	✓	-	-	-	17	INT17_18_32_33 (Note)	External interrupt 17	***[IBIMC079]***	***[IMNFLG5]*** <INT175FLG>
✓	✓	-	-	-			External interrupt 18	***[IBIMC080]***	***[IMNFLG5]*** <INT176FLG>
✓	✓	✓	-	-			External interrupt 32	***[IBIMC095]***	***[IMNFLG5]*** <INT191FLG>
✓	✓	✓	-	-			External interrupt 33	***[IBIMC096]***	***[IMNFLG6]*** <INT192FLG>

✓: Available, -: N/A

Note: Please refer to "4.4.1.About joint interrupt".

Table 6.2 List of interrupt request (2/7)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	-	-	-	18	INT19_22 (Note)	External interrupt 19	***[IBIMC081]***	***[IMNFLG5]*** <INT177FLG>
✓	✓	-	-	-			External interrupt 20	***[IBIMC082]***	***[IMNFLG5]*** <INT178FLG>
✓	✓	-	-	-			External interrupt 21	***[IBIMC083]***	***[IMNFLG5]*** <INT179FLG>
✓	✓	-	-	-			External interrupt 22	***[IBIMC084]***	***[IMNFLG5]*** <INT180FLG>
✓	✓	-	-	-	19	INT23_26 (Note)	External interrupt 23	***[IBIMC085]***	***[IMNFLG5]*** <INT181FLG>
✓	✓	-	-	-			External interrupt 24	***[IBIMC086]***	***[IMNFLG5]*** <INT182FLG>
✓	✓	-	-	-			External interrupt 25	***[IBIMC087]***	***[IMNFLG5]*** <INT183FLG>
✓	✓	-	-	-			External interrupt 26	***[IBIMC088]***	***[IMNFLG5]*** <INT184FLG>
✓	✓	-	-	-	20	INT27_28 (Note)	External interrupt 27	***[IBIMC089]***	***[IMNFLG5]*** <INT185FLG>
✓	✓	-	-	-			External interrupt 28	***[IBIMC090]***	***[IMNFLG5]*** <INT186FLG>
✓	-	-	-	-	21	INT29	External interrupt 29	***[IBIMC091]***	***[IMNFLG5]*** <INT187FLG>
✓	-	-	-	-	22	INT30_31 (Note)	External interrupt 30	***[IBIMC092]***	***[IMNFLG5]*** <INT188FLG>
✓	-	-	-	-			External interrupt 31	***[IBIMC093]***	***[IMNFLG5]*** <INT189FLG>
✓	✓	✓	✓	✓	23	INTEMG0	A-PMD ch0 EMG interrupt		
✓	✓	✓	✓	✓	24	INTOVV0	A-PMD ch0 OVV interrupt		
✓	✓	✓	✓	✓	25	INTPWM0	A-PMD ch0 PWM interrupt		
✓	✓	✓	✓	✓	26	INTENC00	A-ENC ch0 Encoder input interrupt 0		
✓	✓	✓	✓	✓	27	INTENC01	A-ENC ch0 Encoder input interrupt 1		
✓	✓	✓	✓	✓	28	INTADAPDA	ADC Unit A PMD trigger interrupt A		
✓	✓	✓	✓	✓	29	INTADAPDB	ADC Unit A PMD trigger interrupt B		
✓	✓	✓	✓	✓	30	INTADACP0	ADC Unit A Monitor function 0 interrupt		
✓	✓	✓	✓	✓	31	INTADACP1	ADC Unit A Monitor function 1 interrupt		
✓	✓	✓	✓	✓	32	INTADATRG	ADC Unit A General purpose trigger interrupt		
✓	✓	✓	✓	✓	33	INTADASGL	ADC Unit A Single conversion interrupt		
✓	✓	✓	✓	✓	34	INTADACNT	ADC Unit A Continuous conversion interrupt		
✓	✓	✓	✓	✓	35	INTT0RX	TSPI ch0 Receive interrupt		
✓	✓	✓	✓	✓	36	INTT0TX	TSPI ch0 Transmit interrupt		
✓	✓	✓	✓	✓	37	INTT0ERR	TSPI ch0 Error interrupt		
✓	✓	✓	✓	-	38	INTT1RX	TSPI ch1 Receive interrupt		
✓	✓	✓	✓	-	39	INTT1TX	TSPI ch1 Transmit interrupt		
✓	✓	✓	✓	-	40	INTT1ERR	TSPI ch1 Error interrupt		

✓: Available, -: N/A

Note: Please refer to "4.4.1.About joint interrupt".

Table 6.3 List of interrupt request (3/7)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	-	41	INTT2RX	TSPI ch2 Receive interrupt		
✓	✓	✓	✓	-	42	INTT2TX	TSPI ch2 Transmit interrupt		
✓	✓	✓	✓	-	43	INTT2ERR	TSPI ch2 Error interrupt		
✓	✓	✓	✓	-	44	INTT3RX	TSPI ch3 Receive interrupt		
✓	✓	✓	✓	-	45	INTT3TX	TSPI ch3 Transmit interrupt		
✓	✓	✓	✓	-	46	INTT3ERR	TSPI ch3 Error interrupt		
✓	✓	-	-	-	47	INTT4RX	TSPI ch4 Receive interrupt		
✓	✓	-	-	-	48	INTT4TX	TSPI ch4 Transmit interrupt		
✓	✓	-	-	-	49	INTT4ERR	TSPI ch4 Error interrupt		
✓	✓	✓	✓	✓	50	INTI2CWUP	I2CS I2C Wakeup interrupt	***[IAIMC16]***	***[IMNFLG1]*** <INT048FLG>
✓	✓	✓	✓	✓	51	INTI2C0NST (Note)	I2C ch0 interrupt / EI2C ch0 status interrupt		
✓	✓	✓	✓	✓	52	INTI2C0ATX (Note)	I2C ch0 arbitration lost detection interrupt / EI2C ch0 transmit buffer empty interrupt		
✓	✓	✓	✓	✓	53	INTI2C0BRX (Note)	I2C ch0 bus free detection interrupt / EI2C ch0 receive buffer full interrupt		
✓	✓	✓	✓	✓	54	INTI2C0NA	I2C ch0 NACK detection interrupt		
✓	✓	✓	✓	-	55	INTI2C1NST (Note)	I2C ch1 interrupt / EI2C ch1 status interrupt		
✓	✓	✓	✓	-	56	INTI2C1ATX (Note)	I2C ch1 arbitration lost detection interrupt / EI2C ch1 transmit buffer empty interrupt		
✓	✓	✓	✓	-	57	INTI2C1BRX (Note)	I2C ch1 bus free detection interrupt / EI2C ch1 receive buffer full interrupt		
✓	✓	✓	✓	-	58	INTI2C1NA	I2C ch1 NACK detection interrupt		
✓	✓	✓	✓	✓	59	INTI2C2NST (Note)	I2C ch2 interrupt / EI2C ch2 status interrupt		
✓	✓	✓	✓	✓	60	INTI2C2ATX (Note)	I2C ch2 arbitration lost detection interrupt / EI2C ch2 transmit buffer empty interrupt		
✓	✓	✓	✓	✓	61	INTI2C2BRX (Note)	I2C ch2 bus free detection interrupt / EI2C ch2 receive buffer full interrupt		
✓	✓	✓	✓	✓	62	INTI2C2NA	I2C ch2 NACK detection interrupt		
✓	✓	-	-	-	63	INTI2C3NST (Note)	I2C ch3 interrupt / EI2C ch3 status interrupt		
✓	✓	-	-	-	64	INTI2C3ATX (Note)	I2C ch3 arbitration lost detection interrupt / EI2C ch3 transmit buffer empty interrupt		
✓	✓	-	-	-	65	INTI2C3BRX (Note)	I2C ch3 bus free detection interrupt / EI2C ch3 receive buffer full interrupt		
✓	✓	-	-	-	66	INTI2C3NA	I2C ch3 NACK detection interrupt		
✓	✓	✓	✓	✓	67	INTUART0RX	UART ch0 Reception interrupt		
✓	✓	✓	✓	✓	68	INTUART0TX	UART ch0 Transmission interrupt		
✓	✓	✓	✓	✓	69	INTUART0ERR	UART ch0 Error interrupt		
✓	✓	✓	✓	✓	70	INTUART1RX	UART ch1 Reception interrupt		
✓	✓	✓	✓	✓	71	INTUART1TX	UART ch1 Transmission interrupt		
✓	✓	✓	✓	✓	72	INTUART1ERR	UART ch1 Error interrupt		
✓	✓	✓	✓	✓	73	INTUART2RX	UART ch2 Reception interrupt		
✓	✓	✓	✓	✓	74	INTUART2TX	UART ch2 Transmission interrupt		
✓	✓	✓	✓	✓	75	INTUART2ERR	UART ch2 Error interrupt		

✓: Available, -: N/A

Note: Please refer to "4.4.1.About joint interrupt".

Table 6.4 List of interrupt request (4/7)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	✓	76	INTUART3RX	UART ch3 Reception interrupt		
✓	✓	✓	✓	✓	77	INTUART3TX	UART ch3 Transmission interrupt		
✓	✓	✓	✓	✓	78	INTUART3ERR	UART ch3 Error interrupt		
✓	✓	✓	✓	✓	79	INTUART4RX	UART ch4 Reception interrupt		
✓	✓	✓	✓	✓	80	INTUART4TX	UART ch4 Transmission interrupt		
✓	✓	✓	✓	✓	81	INTUART4ERR	UART ch4 Error interrupt		
✓	✓	✓	✓	✓	82	INTUART5RX	UART ch5 Reception interrupt		
✓	✓	✓	✓	✓	83	INTUART5TX	UART ch5 Transmission interrupt		
✓	✓	✓	✓	✓	84	INTUART5ERR	UART ch5 Error interrupt		
✓	✓	✓	✓	✓	85	INTT32A00A	T32A ch0 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	86	INTT32A00ACAP0	T32A ch0 timer A capture 0		
✓	✓	✓	✓	✓	87	INTT32A00ACAP1	T32A ch0 timer A capture 1		
✓	✓	✓	✓	✓	88	INTT32A00B	T32A ch0 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	89	INTT32A00BCAP0	T32A ch0 timer B capture 0		
✓	✓	✓	✓	✓	90	INTT32A00BCAP1	T32A ch0 timer B capture 1		
✓	✓	✓	✓	✓	91	INTT32A00C	T32A ch0 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	92	INTT32A00CCAP0	T32A ch0 timer C capture 0		
✓	✓	✓	✓	✓	93	INTT32A00CCAP1	T32A ch0 timer C capture 1		
✓	✓	✓	✓	✓	94	INTT32A01A	T32A ch1 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	95	INTT32A01ACAP0	T32A ch1 timer A capture 0		
✓	✓	✓	✓	✓	96	INTT32A01ACAP1	T32A ch1 timer A capture 1		
✓	✓	✓	✓	✓	97	INTT32A01B	T32A ch1 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	98	INTT32A01BCAP0	T32A ch1 timer B capture 0		
✓	✓	✓	✓	✓	99	INTT32A01BCAP1	T32A ch1 timer B capture 1		
✓	✓	✓	✓	✓	100	INTT32A01C	T32A ch1 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	101	INTT32A01CCAP0	T32A ch1 timer C capture 0		
✓	✓	✓	✓	✓	102	INTT32A01CCAP1	T32A ch1 timer C capture 1		
✓	✓	✓	✓	✓	103	INTT32A02A	T32A ch2 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	104	INTT32A02ACAP0	T32A ch2 timer A capture 0		
✓	✓	✓	✓	✓	105	INTT32A02ACAP1	T32A ch2 timer A capture 1		
✓	✓	✓	✓	✓	106	INTT32A02B	T32A ch2 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	107	INTT32A02BCAP0	T32A ch2 timer B capture 0		
✓	✓	✓	✓	✓	108	INTT32A02BCAP1	T32A ch2 timer B capture 1		
✓	✓	✓	✓	✓	109	INTT32A02C	T32A ch2 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	110	INTT32A02CCAP0	T32A ch2 timer C capture 0		
✓	✓	✓	✓	✓	111	INTT32A02CCAP1	T32A ch2 timer C capture 1		

✓: Available, -: N/A

Table 6.5 List of interrupt request (5/7)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	✓	112	INTT32A03A	T32A ch3 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	113	INTT32A03ACAP0	T32A ch3 timer A capture 0		
✓	✓	✓	✓	✓	114	INTT32A03ACAP1	T32A ch3 timer A capture 1		
✓	✓	✓	✓	✓	115	INTT32A03B	T32A ch3 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	116	INTT32A03BCAP0	T32A ch3 timer B capture 0		
✓	✓	✓	✓	✓	117	INTT32A03BCAP1	T32A ch3 timer B capture 1		
✓	✓	✓	✓	✓	118	INTT32A03C	T32A ch3 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	119	INTT32A03CCAP0	T32A ch3 timer C capture 0		
✓	✓	✓	✓	✓	120	INTT32A03CCAP1	T32A ch3 timer C capture 1		
✓	✓	✓	✓	✓	121	INTT32A04A	T32A ch4 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	122	INTT32A04ACAP0	T32A ch4 timer A capture 0		
✓	✓	✓	✓	✓	123	INTT32A04ACAP1	T32A ch4 timer A capture 1		
✓	✓	✓	✓	✓	124	INTT32A04B	T32A ch4 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	125	INTT32A04BCAP0	T32A ch4 timer B capture 0		
✓	✓	✓	✓	✓	126	INTT32A04BCAP1	T32A ch4 timer B capture 1		
✓	✓	✓	✓	✓	127	INTT32A04C	T32A ch4 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	128	INTT32A04CCAP0	T32A ch4 timer C capture 0		
✓	✓	✓	✓	✓	129	INTT32A04CCAP1	T32A ch4 timer C capture 1		
✓	✓	✓	✓	✓	130	INTT32A05A	T32A ch5 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	131	INTT32A05ACAP0	T32A ch5 timer A capture 0		
✓	✓	✓	✓	✓	132	INTT32A05ACAP1	T32A ch5 timer A capture 1		
✓	✓	✓	✓	✓	133	INTT32A05B	T32A ch5 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	134	INTT32A05BCAP0	T32A ch5 timer B capture 0		
✓	✓	✓	✓	✓	135	INTT32A05BCAP1	T32A ch5 timer B capture 1		
✓	✓	✓	✓	✓	136	INTT32A05C	T32A ch5 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	137	INTT32A05CCAP0	T32A ch5 timer C capture 0		
✓	✓	✓	✓	✓	138	INTT32A05CCAP1	T32A ch5 timer C capture 1		

✓: Available, -: N/A

Table 6.6 List of interrupt request (6/7)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	✓	139	INTT32A06A	T32A ch6 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	140	INTT32A06ACAP0	T32A ch6 timer A capture 0		
✓	✓	✓	✓	✓	141	INTT32A06ACAP1	T32A ch6 timer A capture 1		
✓	✓	✓	✓	✓	142	INTT32A06B	T32A ch6 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	143	INTT32A06BCAP0	T32A ch6 timer B capture 0		
✓	✓	✓	✓	✓	144	INTT32A06BCAP1	T32A ch6 timer B capture 1		
✓	✓	✓	✓	✓	145	INTT32A06C	T32A ch6 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	146	INTT32A06CCAP0	T32A ch6 timer C capture 0		
✓	✓	✓	✓	✓	147	INTT32A06CCAP1	T32A ch6 timer C capture 1		
✓	✓	✓	✓	✓	148	INTT32A07A	T32A ch7 timer A match, overflow, and underflow		
✓	✓	✓	✓	✓	149	INTT32A07ACAP0	T32A ch7 timer A capture 0		
✓	✓	✓	✓	✓	150	INTT32A07ACAP1	T32A ch7 timer A capture 1		
✓	✓	✓	✓	✓	151	INTT32A07B	T32A ch7 timer B match, overflow, and underflow		
✓	✓	✓	✓	✓	152	INTT32A07BCAP0	T32A ch7 timer B capture 0		
✓	✓	✓	✓	✓	153	INTT32A07BCAP1	T32A ch7 timer B capture 1		
✓	✓	✓	✓	✓	154	INTT32A07C	T32A ch7 timer C match, overflow, and underflow		
✓	✓	✓	✓	✓	155	INTT32A07CCAP0	T32A ch7 timer C capture 0		
✓	✓	✓	✓	✓	156	INTT32A07CCAP1	T32A ch7 timer C capture 1		
✓	✓	✓	✓	✓	157	INTPARI	RAMP RAM parity interrupt		
✓	✓	✓	✓	✓	158	INTDMAATC (Note)	DMAC Unit A transfer completion interrupt (ch0 to 31)	***[IBIMC000]*** to ***[IBIMC031]***	***[IMNFLG3]*** <INT96FLG> to <INT127FLG>
✓	✓	✓	✓	✓	159	INTDMAAERR	DMAC Unit A transfer error interrupt	***[IBIMC032]***	***[IMNFLG4]*** <INT128FLG>
✓	✓	✓	✓	✓	160	INTDMABTC (Note)	DMAC Unit B transfer completion interrupt (ch0 to 31)	***[IBIMC033]*** to ***[IBIMC064]***	***[IMNFLG4]*** <INT129FLG> to ***[IMNFLG5]*** <INT160FLG>
✓	✓	✓	✓	✓	161	INTDMABERR	DMAC Unit B transfer error interrupt	***[IBIMC065]***	***[IMNFLG5]*** <INT161FLG>
✓	✓	✓	✓	✓	162	INTRTC	RTC interrupt	***[IAIMC17]***	***[IMNFLG1]*** <INT049FLG>
✓	✓	✓	✓	✓	163	INTRMC0	RMC ch0 Remote control interrupt	***[IBIMC094]***	***[IMNFLG5]*** <INT190FLG>
✓	✓	✓	✓	✓	164	INTFLCRDY	Code FLASH Ready interrupt		
✓	✓	✓	✓	✓	165	INTFLDRDY	Data FLASH Ready interrupt		

✓: Available, -: N/A

Note: Please refer to "4.4.1.About joint interrupt".

Table 6.7 List of interrupt request (7/7)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt No	Interrupt Factor	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	-	166	INTLCDBUSF	LCD register write end interrupt		
✓	✓	✓	✓	-	167	INTLCDSTOP	LCD stop interrupt		
✓	✓	✓	✓	✓	168	INTUART6RX	UART ch6 Reception interrupt		
✓	✓	✓	✓	✓	169	INTUART6TX	UART ch6 Transmission interrupt		
✓	✓	✓	✓	✓	170	INTUART6ERR	UART ch6 Error interrupt		
✓	✓	✓	-	-	171	INTUART7RX	UART ch7 Reception interrupt		
✓	✓	✓	-	-	172	INTUART7TX	UART ch7 Transmission interrupt		
✓	✓	✓	-	-	173	INTUART7ERR	UART ch7 Error interrupt		

✓: Available, -: N/A

Table 6.8 Interrupt Number 158 (1/2)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt Factor INTDMAATC (DMAC Unit A)	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	✓	ch0	TSPI ch0 Receive DMA request	***[IBIMC000]***	***[IMNFLG3]***<INT96FLG>
✓	✓	✓	✓	✓	ch1	TSPI ch0 Transmit DMA request	***[IBIMC001]***	***[IMNFLG3]***<INT97FLG>
✓	✓	✓	✓	-	ch2	TSPI ch1 Receive DMA request	***[IBIMC002]***	***[IMNFLG3]***<INT98FLG>
✓	✓	✓	✓	-	ch3	TSPI ch1 Transmit DMA request	***[IBIMC003]***	***[IMNFLG3]***<INT99FLG>
✓	✓	✓	✓	✓	ch4	I2C ch0 Receiving DMA request / EI2C ch0 Receiving DMA request	***[IBIMC004]***	***[IMNFLG3]***<INT100FLG>
✓	✓	✓	✓	✓	ch5	I2C ch0 Transmitting DMA request / EI2C ch0 Transmitting DMA request	***[IBIMC005]***	***[IMNFLG3]***<INT101FLG>
✓	✓	✓	✓	✓	ch6	UART ch0 Reception DMA request	***[IBIMC006]***	***[IMNFLG3]***<INT102FLG>
✓	✓	✓	✓	✓	ch7	UART ch0 Transmission DMA request	***[IBIMC007]***	***[IMNFLG3]***<INT103FLG>
✓	✓	✓	✓	✓	ch8	UART ch1 Reception DMA request	***[IBIMC008]***	***[IMNFLG3]***<INT104FLG>
✓	✓	✓	✓	✓	ch9	UART ch1 Transmission DMA request	***[IBIMC009]***	***[IMNFLG3]***<INT105FLG>
✓	✓	✓	✓	✓	ch10	UART ch2 Reception DMA request	***[IBIMC010]***	***[IMNFLG3]***<INT106FLG>
✓	✓	✓	✓	✓	ch11	UART ch2 Transmission DMA request	***[IBIMC011]***	***[IMNFLG3]***<INT107FLG>
✓	✓	✓	✓	✓	ch12	UART ch3 Reception DMA request	***[IBIMC012]***	***[IMNFLG3]***<INT108FLG>
✓	✓	✓	✓	✓	ch13	UART ch3 Transmission DMA request	***[IBIMC013]***	***[IMNFLG3]***<INT109FLG>
✓	✓	✓	✓	✓	ch14	A-PMD ch0 PWM interrupt	***[IBIMC014]***	***[IMNFLG3]***<INT110FLG>
✓	✓	✓	✓	✓	ch15	T32A ch0 DMA request at match A1 register	***[IBIMC015]***	***[IMNFLG3]***<INT111FLG>
						T32A ch0 DMA request at match C1 register		
						T32A ch1 DMA request at match A1 register		
						T32A ch1 DMA request at match C1 register		
✓	✓	✓	✓	✓	ch16	T32A ch2 DMA request at match A1 register	***[IBIMC016]***	***[IMNFLG3]***<INT112FLG>
						T32A ch2 DMA request at match C1 register		
						T32A ch3 DMA request at match A1 register		
						T32A ch3 DMA request at match C1 register		
✓	✓	✓	✓	✓	ch17	T32A ch0 DMA request at match B1 register	***[IBIMC017]***	***[IMNFLG3]***<INT113FLG>
						T32A ch1 DMA request at match B1 register		
✓	✓	✓	✓	✓	ch18	T32A ch2 DMA request at match B1 register	***[IBIMC018]***	***[IMNFLG3]***<INT114FLG>
						T32A ch3 DMA request at match B1 register		
✓	✓	✓	✓	✓	ch19	T32A ch0 DMA request at capture A0 register	***[IBIMC019]***	***[IMNFLG3]***<INT115FLG>
						T32A ch0 DMA request at capture A1 register		
						T32A ch1 DMA request at capture A0 register		
						T32A ch1 DMA request at capture A1 register		
						T32A ch0 DMA request at capture C0 register		
						T32A ch0 DMA request at capture C1 register		
						T32A ch1 DMA request at capture C0 register		
						T32A ch1 DMA request at capture C1 register		

✓: Available, -: N/A

Table 6.9 Interrupt Number 158 (2/2)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt Factor INTDMAATC (DMAC Unit A)	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	✓	ch20	T32A ch2 DMA request at capture A0 register	*[IBIMC020]*	*[IMNFLG3]*<INT116FLG>
						T32A ch2 DMA request at capture A1 register		
						T32A ch3 DMA request at capture A0 register		
						T32A ch3 DMA request at capture A1 register		
						T32A ch2 DMA request at capture C0 register		
						T32A ch2 DMA request at capture C1 register		
						T32A ch3 DMA request at capture C0 register		
						T32A ch3 DMA request at capture C1 register		
✓	✓	✓	✓	✓	ch21	T32A ch0 DMA request at capture B0 register	*[IBIMC021]*	*[IMNFLG3]*<INT117FLG>
						T32A ch0 DMA request at capture B1 register		
						T32A ch1 DMA request at capture B0 register		
						T32A ch1 DMA request at capture B1 register		
✓	✓	✓	✓	✓	ch22	T32A ch2 DMA request at capture B0 register	*[IBIMC022]*	*[IMNFLG3]*<INT118FLG>
						T32A ch2 DMA request at capture B1 register		
						T32A ch3 DMA request at capture B0 register		
						T32A ch3 DMA request at capture B1 register		
✓	✓	✓	✓	✓	ch23	DMAC A ch0 transmission end interrupt	*[IBIMC023]*	*[IMNFLG3]*<INT119FLG>
						DMAC A ch1 transmission end interrupt		
						DMAC A ch6 transmission end interrupt		
						DMAC A ch7 transmission end interrupt		
✓	✓	✓	✓	✓	ch24	DMAC A ch2 transmission end interrupt	*[IBIMC024]*	*[IMNFLG3]*<INT120FLG>
						DMAC A ch3 transmission end interrupt		
						DMAC A ch8 transmission end interrupt		
						DMAC A ch9 transmission end interrupt		
✓	✓	✓	✓	✓	ch25	DMAC A ch4 transmission end interrupt	*[IBIMC025]*	*[IMNFLG3]*<INT121FLG>
						DMAC A ch5 transmission end interrupt		
						DMAC A ch10 transmission end interrupt		
						DMAC A ch11 transmission end interrupt		
✓	✓	✓	✓	✓	ch26	DMAC A ch12 transmission end interrupt	*[IBIMC026]*	*[IMNFLG3]*<INT122FLG>
						DMAC A ch13 transmission end interrupt		
						DMAC A ch14 transmission end interrupt		
✓	✓	✓	✓	✓	ch27	DMAC A ch15 transmission end interrupt	*[IBIMC027]*	*[IMNFLG3]*<INT123FLG>
						DMAC A ch19 transmission end interrupt		
✓	✓	✓	✓	✓	ch28	DMAC A ch16 transmission end interrupt	*[IBIMC028]*	*[IMNFLG3]*<INT124FLG>
						DMAC A ch20 transmission end interrupt		
✓	✓	✓	✓	✓	ch29	DMAC A ch17 transmission end interrupt	*[IBIMC029]*	*[IMNFLG3]*<INT125FLG>
						DMAC A ch21 transmission end interrupt		
✓	✓	✓	✓	✓	ch30	DMAC A ch18 transmission end interrupt	*[IBIMC030]*	*[IMNFLG3]*<INT126FLG>
						DMAC A ch22 transmission end interrupt		
✓	✓	✓	✓	✓	ch31	TRGIN0 (PB1 pin)	*[IBIMC031]*	*[IMNFLG3]*<INT127FLG>
						TRGIN1 (PA3 pin)		
						TRGIN2 (PN3 pin)		

✓: Available, -: N/A

Table 6.10 Interrupt Number 160 (1/2)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt Factor INTDMABTC (DMAC Unit B)	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	-	ch0	TSPI ch2 Receive DMA request	*[IBIMC033]*	*[IMNFLG4]*<INT129FLG>
✓	✓	-	-	-		I2C ch3 Receiving DMA request / EI2C ch3 Receiving DMA request		
✓	✓	✓	✓	-	ch1	TSPI ch2 Transmit DMA request	*[IBIMC034]*	*[IMNFLG4]*<INT130FLG>
✓	✓	-	-	-		I2C ch3 Transmitting DMA request / EI2C ch3 Transmitting DMA request		
✓	✓	✓	✓	-	ch2	TSPI ch3 Receive DMA request	*[IBIMC035]*	*[IMNFLG4]*<INT131FLG>
✓	✓	✓	✓	-	ch3	TSPI ch3 Transmit DMA request	*[IBIMC036]*	*[IMNFLG4]*<INT132FLG>
✓	✓	-	-	-	ch4	TSPI ch4 Receive DMA request	*[IBIMC037]*	*[IMNFLG4]*<INT133FLG>
✓	✓	-	-	-	ch5	TSPI ch4 Transmit DMA request	*[IBIMC038]*	*[IMNFLG4]*<INT134FLG>
✓	✓	✓	✓	-	ch6	I2C ch1 Receiving DMA request / EI2C ch1 Receiving DMA request	*[IBIMC039]*	*[IMNFLG4]*<INT135FLG>
✓	✓	✓	✓	-	ch7	I2C ch1 Transmitting DMA request / EI2C ch1 Transmitting DMA request	*[IBIMC040]*	*[IMNFLG4]*<INT136FLG>
✓	✓	✓	✓	✓	ch8	I2C ch2 Receiving DMA request / EI2C ch2 Receiving DMA request	*[IBIMC041]*	*[IMNFLG4]*<INT137FLG>
✓	✓	✓	✓	✓	ch9	I2C ch2 Transmitting DMA request / EI2C ch2 Transmitting DMA request	*[IBIMC042]*	*[IMNFLG4]*<INT138FLG>
✓	✓	✓	✓	✓	ch10	UART ch4 Reception DMA request	*[IBIMC043]*	*[IMNFLG4]*<INT139FLG>
✓	✓	✓	✓	✓	ch11	UART ch4 Transmission DMA request	*[IBIMC044]*	*[IMNFLG4]*<INT140FLG>
✓	✓	✓	✓	✓	ch12	UART ch5 Reception DMA request	*[IBIMC045]*	*[IMNFLG4]*<INT141FLG>
✓	✓	✓	✓	✓	ch13	UART ch5 Transmission DMA request	*[IBIMC046]*	*[IMNFLG4]*<INT142FLG>
✓	✓	✓	✓	✓	ch14	ADC Unit A General-purpose trigger DMA request	*[IBIMC047]*	*[IMNFLG4]*<INT143FLG>
						ADC Unit A Single conversion DMA request		
						ADC Unit A Continuous conversion DMA request		
✓	✓	✓	✓	✓	ch15	T32A ch4 DMA request at match A1 register	*[IBIMC048]*	*[IMNFLG4]*<INT144FLG>
						T32A ch4 DMA request at match C1 register		
						T32A ch5 DMA request at match A1 register		
						T32A ch5 DMA request at match C1 register		
✓	✓	✓	✓	✓	ch16	T32A ch6 DMA request at match A1 register	*[IBIMC049]*	*[IMNFLG4]*<INT145FLG>
						T32A ch6 DMA request at match C1 register		
						T32A ch7 DMA request at match A1 register		
						T32A ch7 DMA request at match C1 register		
✓	✓	✓	✓	✓	ch17	T32A ch4 DMA request at match B1 register	*[IBIMC050]*	*[IMNFLG4]*<INT146FLG>
						T32A ch5 DMA request at match B1 register		
						UART ch6 Reception DMA request		
✓	✓	✓	✓	✓	ch18	T32A ch6 DMA request at match B1 register	*[IBIMC051]*	*[IMNFLG4]*<INT147FLG>
						T32A ch7 DMA request at match B1 register		
						UART ch6 Transmission DMA request		
✓	✓	✓	✓	✓	ch19	T32A ch4 DMA request at capture A0 register	*[IBIMC052]*	*[IMNFLG4]*<INT148FLG>
						T32A ch4 DMA request at capture A1 register		
						T32A ch5 DMA request at capture A0 register		
						T32A ch5 DMA request at capture A1 register		
						T32A ch4 DMA request at capture C0 register		
						T32A ch4 DMA request at capture C1 register		
						T32A ch5 DMA request at capture C0 register		
						T32A ch5 DMA request at capture C1 register		

✓: Available, -: N/A

Table 6.11 Interrupt Number 160 (2/2)

M3HQ	M3HP	M3HN	M3HM	M3HL	Interrupt Factor INTDMAATC (DMAC Unit A)	Interrupt Request	Interrupt Control Register	Interrupt Monitor Register
✓	✓	✓	✓	✓	ch20	T32A ch6 DMA request at capture A0 register	*[IBIMC053]*	*[IMNFLG4]*<INT149FLG>
						T32A ch6 DMA request at capture A1 register		
						T32A ch7 DMA request at capture A0 register		
						T32A ch7 DMA request at capture A1 register		
						T32A ch6 DMA request at capture C0 register		
						T32A ch6 DMA request at capture C1 register		
						T32A ch7 DMA request at capture C0 register		
						T32A ch7 DMA request at capture C1 register		
✓	✓	✓	✓	✓	ch21	T32A ch4 DMA request at capture B0 register	*[IBIMC054]*	*[IMNFLG4]*<INT150FLG>
						T32A ch4 DMA request at capture B1 register		
						T32A ch5 DMA request at capture B0 register		
						T32A ch5 DMA request at capture B1 register		
						UART ch7 Reception DMA request (Note)		
✓	✓	✓	✓	✓	ch22	T32A ch6 DMA request at capture B0 register	*[IBIMC055]*	*[IMNFLG4]*<INT151FLG>
						T32A ch6 DMA request at capture B1 register		
						T32A ch7 DMA request at capture B0 register		
						T32A ch7 DMA request at capture B1 register		
						UART ch7 Transmission DMA request (Note)		
✓	✓	✓	✓	✓	ch23	DMAC B ch0 transmission end interrupt	*[IBIMC056]*	*[IMNFLG4]*<INT152FLG>
						DMAC B ch1 transmission end interrupt		
						DMAC B ch6 transmission end interrupt		
						DMAC B ch7 transmission end interrupt		
✓	✓	✓	✓	✓	ch24	DMAC B ch2 transmission end interrupt	*[IBIMC057]*	*[IMNFLG4]*<INT153FLG>
						DMAC B ch3 transmission end interrupt		
						DMAC B ch8 transmission end interrupt		
						DMAC B ch9 transmission end interrupt		
✓	✓	✓	✓	✓	ch25	DMAC B ch4 transmission end interrupt	*[IBIMC058]*	*[IMNFLG4]*<INT154FLG>
						DMAC B ch5 transmission end interrupt		
						DMAC B ch10 transmission end interrupt		
						DMAC B ch11 transmission end interrupt		
✓	✓	✓	✓	✓	ch26	DMAC B ch12 transmission end interrupt	*[IBIMC059]*	*[IMNFLG4]*<INT155FLG>
						DMAC B ch13 transmission end interrupt		
						DMAC B ch14 transmission end interrupt		
✓	✓	✓	✓	✓	ch27	DMAC B ch15 transmission end interrupt	*[IBIMC060]*	*[IMNFLG4]*<INT156FLG>
						DMAC B ch19 transmission end interrupt		
✓	✓	✓	✓	✓	ch28	DMAC B ch16 transmission end interrupt	*[IBIMC061]*	*[IMNFLG4]*<INT157FLG>
						DMAC B ch20 transmission end interrupt		
✓	✓	✓	✓	✓	ch29	DMAC B ch17 transmission end interrupt	*[IBIMC062]*	*[IMNFLG4]*<INT158FLG>
						DMAC B ch21 transmission end interrupt		
✓	✓	✓	✓	✓	ch30	DMAC B ch18 transmission end interrupt	*[IBIMC063]*	*[IMNFLG4]*<INT159FLG>
						DMAC B ch22 transmission end interrupt		
✓	✓	✓	✓	✓	ch31	TRGIN0 (PB1 pin)	*[IBIMC064]*	*[IMNFLG5]*<INT160FLG>
						TRGIN1 (PA3 pin)		
						TRGIN2 (PN3 pin)		

✓: Available, -: N/A

Note: M3HM and M3HL do not have UART 7ch interrupt request.

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2021-03-02	First release

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