# 32-bit RISC Microcontroller

# TXZ+ Family
## Reference Manual

## LCD Display Control Circuit (DLCD-A)

## Revision 1.0

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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## Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

## Terms and Abbreviations

Some of abbreviations used in this document are as follows:

| | |
|---|---|
| COM | Common |
| SEG | Segment |
| LCD | Liquid Crystal Display |
| fc | High speed clock from fosc or $f_{PLL}$ . |
| $f_{IHOSC2}$ | Clock from high speed oscillator |
| $f_{PLL}$ | Clock from multiplier circuit (PLL) |
| IHOSC2 | Internal High Speed Oscillator 2 |
| VLC | LCD power supply |

# 1. Outlines

The LCD display control circuit can directly drive a liquid crystal display (hereinafter LCD) with a maximum of 160 pixels (40 SEG × 4 COM). This circuit supports 4 Common/3 Common of non-bias drive, contrast adjustment can be controlled by frame length control and time division control. This circuit has a built-in switching function for the SEG and DCOM pin order, and can be set according to the pin configuration.

**Table 1.1 LCD driving system (Outline)**

| Driving system | Number of COM | Duty | Output Voltage | | Maximum pixels |
|---|---|---|---|---|---|
| | | | Segment | Common | |
| Non-bias drive | 4 | 1/6 | 2 Level | 2 Level | 160 |
| | 3 | 1/4 | | | 120 |

**Table 1.2 Contrast adjustment (Outline)**

| Contrast adjustment | remark |
|---|---|
| Frame length control | Insert contrast adjustment state, and control in that cycle |
| Time division control | Control by inserting a contrast adjustment cycle in each state |

# 2. Configuration

The figure below shows the LCD display control circuit.

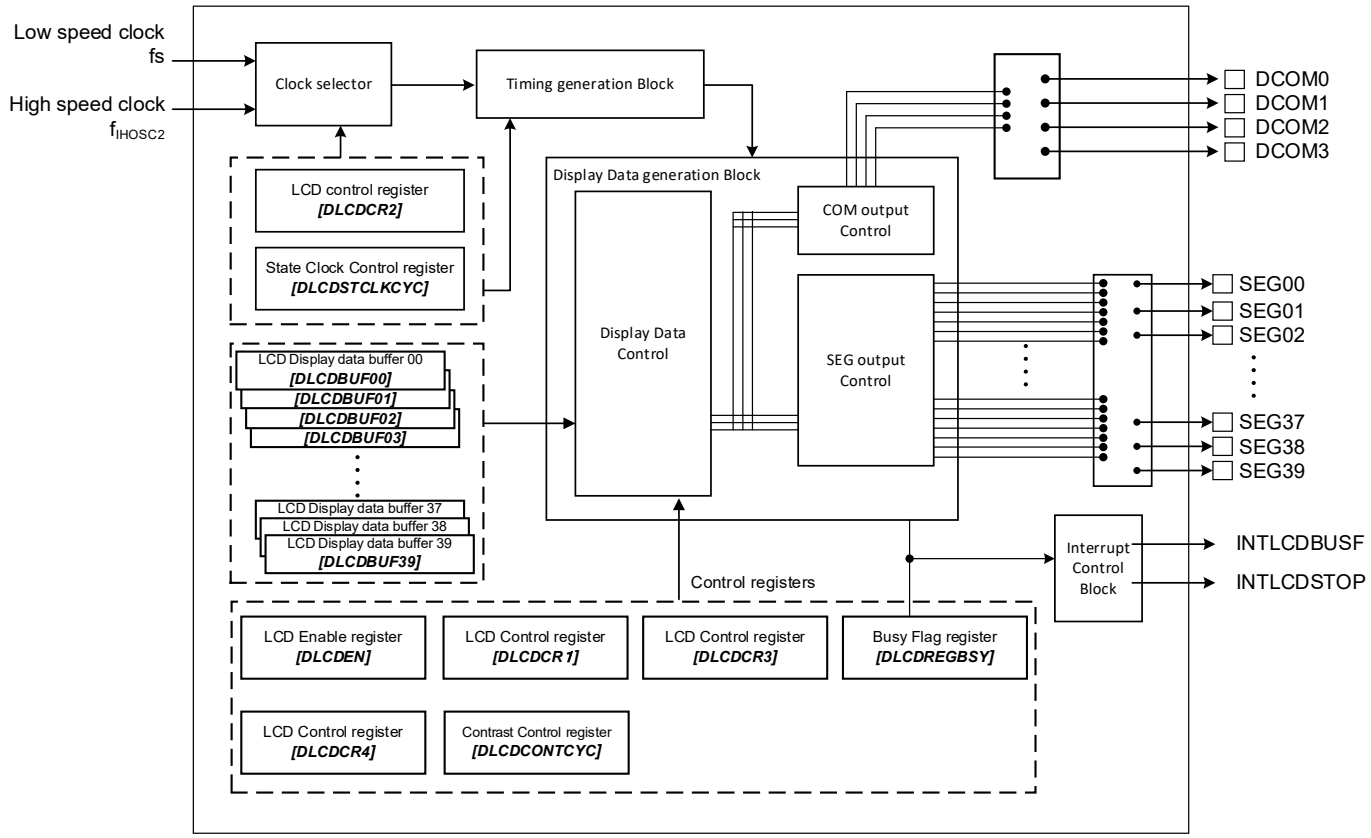


**Figure 2.1 LCD Display Control Circuit**

**Table 2.1 List of Signals**

| No | Symbol | Signal Name | I/O | Related reference manual |
|---|---|---|---|---|
| 1 | DCOMx | 1/1Bias Drive LCD COMx output (x=0 to 3) | Output | Product Information, Input and Output ports |
| 2 | SEGx | LCD SEGx Output (x=00 to 39) | Output | Product Information, Input and Output ports |
| 3 | INTLCDBUSF | Register Writing Completion Interrupt | Output | Exception, Product Information |
| 4 | INTLCDSTOP | LCD Stopped Interrupt | Output | Exception, Product Information |
| 5 | fs | Low Speed Clock (=32.768kHz) | Input | Product Information |
| 6 | $f_{IHOSC2}$ | On Chip High Speed Clock (=10MHz) | Input | Product Information |

# 3. Function & Operation

When using the LCD display control circuit, make sure that the IHOSC2 or fs clock used as the operating clock is oscillating stably.

For detail of Clock setting, refer to reference manual "Clock Control and Operation mode".

## 3.1. LCD Drive system selection

### 3.1.1. Overview

The LCD drive system supports 2 types of non-bias drive system, 4COM and 3COM. Two types of contrast adjustment methods, "frame length control" and "time division control" can be selected.

With this, four kinds of circuit operations are performed.

## 3.2. Operation Clock selection

The LCD display control circuit can select either of the two operating clocks by software setting.

### 3.2.1. Overview

The operating clock (Lck1) can be selected from the internal high-speed oscillation 2 (IHOSC2, 10MHz) divided by 256 and the low-speed oscillation (fs) by setting the LCD control register ***[DLCDCR2]***<CLKSEL>.

**Table 3.1 Operating clock selection**

| ***[DLCDCR2]*<CLKSEL>** | **Operating Clock (Lck1)** | **Frequency[kHz]** |
|---|---|---|
| 0 | $f_{IHOSC2}$ / 256 | 39.0625 |
| 1 | fs | 32.765 |

### 3.2.2. Reference Clock

The reference clock used in the LCD display control circuit is set as shown in the table below by setting the Lck1 and ***[DLCDCR2]***<CONTSEL> registers.

| **Contrast Control** | | **Reference Clock** |
|---|---|---|
| Time division Contrast control | <CONTSEL>=1 | (***[DLCDSTCLKCYC]*** + 1) / Lck1 |
| Frame length Contrast control | <CONTSEL>=0 | (***[DLCDCONTCYC]*** + 1) × 6 / Lck1 |
| | | (***[DLCDCONTCYC]*** + 1) × 4 / Lck1 |

A period of minimum reference clock when Lck1 is 39kHz is calculated as (0+1)/39kHz = 25.6 (μs).

## 3.3. Operation

The following shows each drive method and output waveform of the LCD display control circuit.

### 3.3.1. Non-Bias Drive

The non-bias drive method can control both SEG and COM with only two values (VDD, GND), and does not require the circuit that generates the intermediate potential that was required in the past.

As for 4COM drive, 1 frame configuration is 1/6 duty including dummy frame, and the ratio of ON voltage.

The ratio of ON voltage required for LCD display to OFF voltage required for non-display (ON/OFF ratio) is narrower at 1.41 compared to 1.73 of the conventional drive type.

When the actual ON/OFF voltage is 2.44V / 1.73V and exceeds the LCD display threshold, all Segments will be turned on. To reduce the ON/OFF voltage, it is necessary to control by adding a non-lighting period (blanking period) in one frame.

The non-bias drive diagram for 4COM/3COM is shown below.

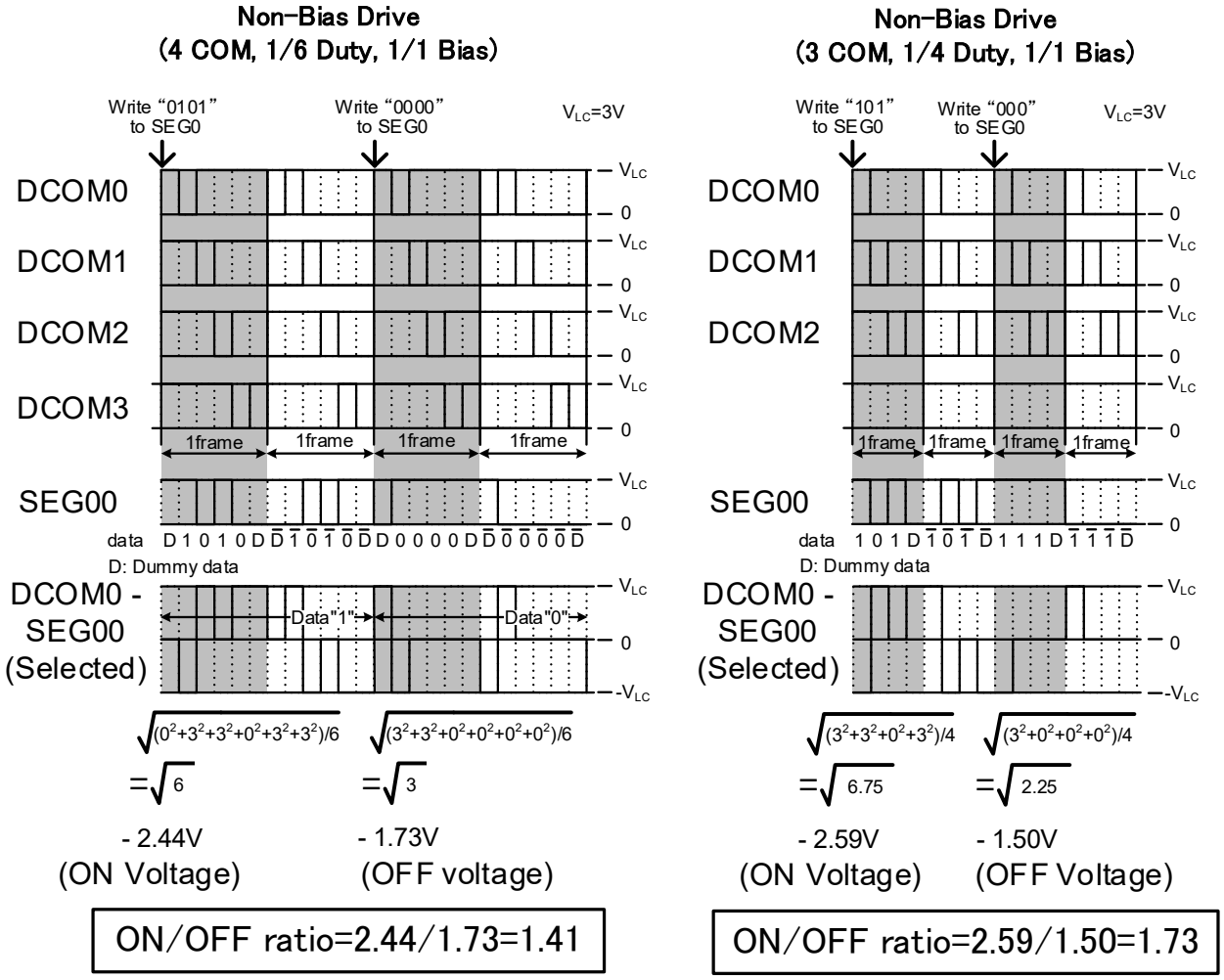


**Figure 3.1 Non-Bias Drive**

### 3.3.1.1. Non-Bias drive (4 Common, 1/6 Duty) Timing

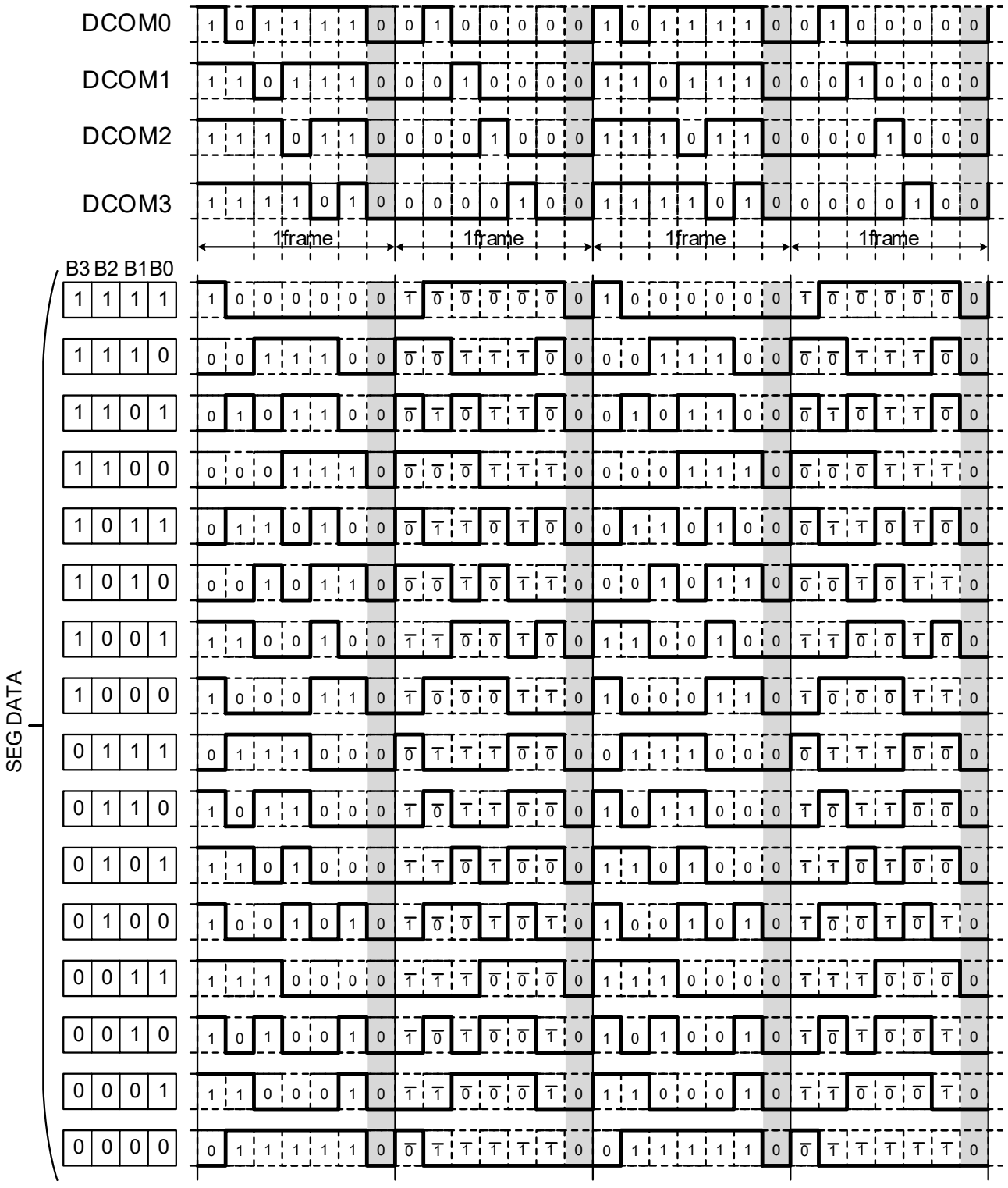


**Figure 3.2 Non-Bias drive (4 Common, 1/6 Duty) Timing**

### 3.3.1.2. Non-Bias drive (3 Common, 1/4 Duty) Timing

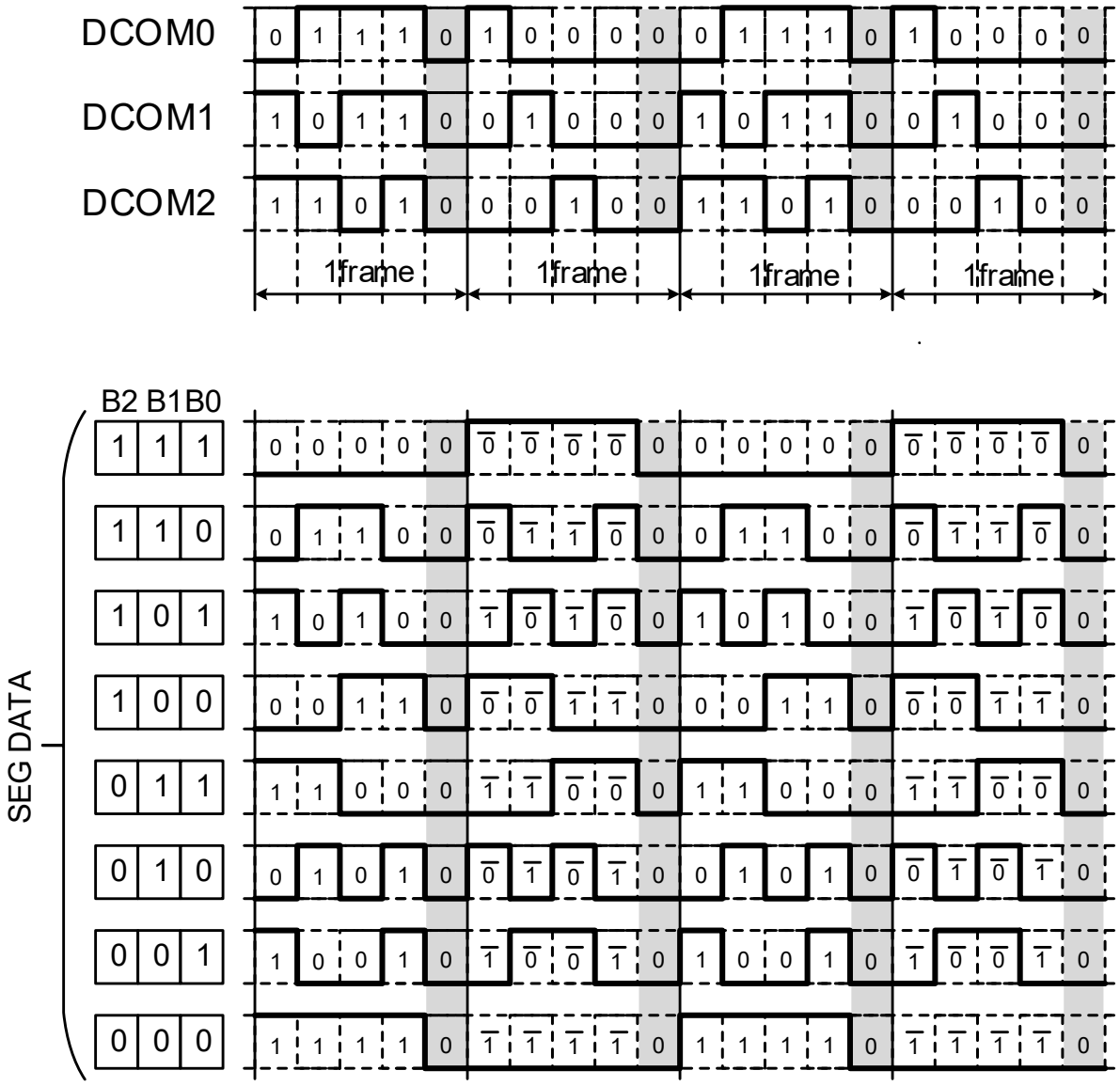


**Figure 3.3 Non-Bias drive (3 Common, 1/4 Duty) Timing**

### 3.3.2. Frame Frequency

The frame frequency is calculated by the formula in the following table according to the lck2 clock frequency and the ***[DLCDSTCLKCYC]***<STCYC[7:0]> and ***[DLCDCONTCYC]***<CONT[7:0]> register values. Normally, set it to about 80Hz.

lck2 is the frequency of fs when ***[DLCDCR2]***<CLKSEL> is fs, or is the frequency of $f_{IHOSC2}$ divided by 256 (=39.0625[kHz]) when IHOSC2 using.

In the case of the frame length control method, the number of cycles of the set values of ***[DLCDSTCLKCYC]***<STCYC[7:0]> and ***[DLCDCONTCYC]***<CONT[7:0]> is the same. Therefore, the frame frequency does not change even if one is added (subtracted) and the other is subtracted (added) by the same number.

In the case of time division control method, the frame frequency is determined by the value of ***[DLCDSTCLKCYC]***, and the value of ***[DLCDCONTCYC]*** does not affect the frame frequency.

**Table 3.2 The formula of Frame Frequency**

| Driving system | Frame Frequency[Hz] | |
|---|---|---|
| | Frame length control | Time division control |
| 4COM 1/6 duty | $\frac{\text{lck2[Hz]}}{((<\text{STCYC[7:0]}> + 1) + (<\text{CONT[7:0]}> + 1)) \times 6}$ | $\frac{\text{lck2[Hz]}}{(<\text{STCYC[7:0]}> + 1) \times 6}$ |
| 3COM 1/4 duty | $\frac{\text{lck2[Hz]}}{((<\text{STCYC[7:0]}> + 1) + (<\text{CONT[7:0]}> + 1)) \times 4}$ | $\frac{\text{lck2[Hz]}}{(<\text{STCYC[7:0]}> + 1) \times 4}$ |

### 3.3.3. Contrast adjustment

Contrast adjustment supports two types of "frame length control method" and "time division control method" as shown below.

#### 3.3.3.1. Frame length control method

Setting ***[DLCDCR2]***<CONTSEL> to "0" enables contrast adjustment by the frame length control method.

This method adjusts the contrast by inserting the "L" output at the end of the frame.

Figure 3.4 shows an example when STCYC=36 and CONT=30.

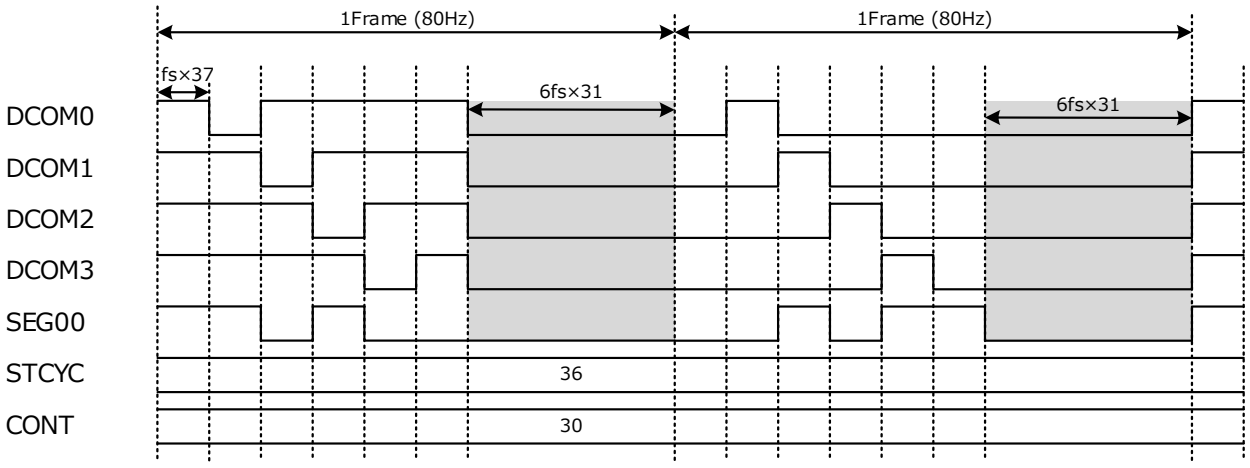


**Figure 3.4 Frame length control method (*[DLCDCR2]*<CLKSEL>=1, *[DLCDCR2]*<DUTY[1:0]>=00)**

### 3.3.3.2. Time division control method

When ***[DLCDCR1]***<CONTSEL> is set to "1", the contrast can be adjusted by the time division control method. This method adjusts the contrast by inserting the "L" output in the display cycle.

Figure 3.5 shows an example when <STCYC>=67 and <CONT>=49.

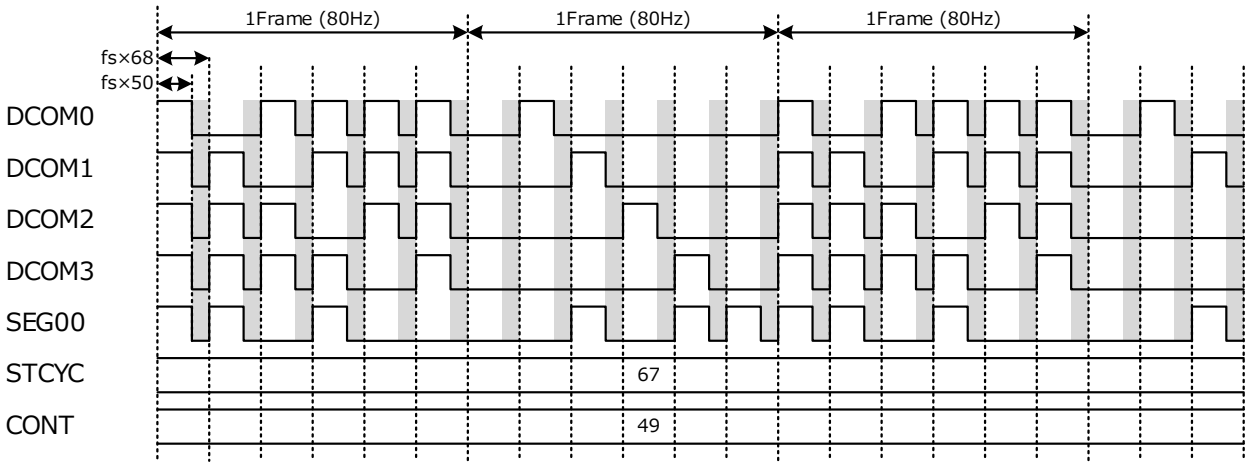


**Figure 3.5 Time division control method (*[DLCDCR2]*<CLKSEL>=1, *[DLCDCR2]*<DUTY[1:0]>=00)**

### 3.3.3.3. Formula and Setting

The Von/Voff calculation formulas and setting examples for the frame length control system and time division control system are shown below.

**Table 3.3 Formula of Von/ Voff voltage (Frame length control)**

| Driving system | | Run Voltage [$V_{RM}$] |
|---|---|---|
| 4 COM 1/6 Duty | Von voltage | $\sqrt{V^2 \times \frac{4}{6} \times \frac{[DLCDSTCLKCYC]+1}{([DLCDSTCLKCYC]+[DLCDCONTCYC]+2)}}$ |
| | Voff voltage | $\sqrt{V^2 \times \frac{2}{6} \times \frac{[DLCDSTCLKCYC]+1}{([DLCDSTCLKCYC]+[DLCDCONTCYC]+2)}}$ |
| 3 COM 1/4 Duty | Von voltage | $\sqrt{V^2 \times \frac{3}{4} \times \frac{[DLCDSTCLKCYC]+1}{([DLCDSTCLKCYC]+[DLCDCONTCYC]+2)}}$ |
| | Voff voltage | $\sqrt{V^2 \times \frac{1}{4} \times \frac{[DLCDSTCLKCYC]+1}{([DLCDSTCLKCYC]+[DLCDCONTCYC]+2)}}$ |

**Table 3.4 Formula of Von/ Voff voltage (Time division control)**

| Driving system | | Run voltage [$V_{RM}$] |
|---|---|---|
| 4 COM 1/6 Duty | Von voltage | $\sqrt{V^2 \times \frac{4}{6} \times \frac{[DLCDCONTCYC]+1}{[DLCDSTCLKCYC]+1}}$ |
| | Voff voltage | $\sqrt{V^2 \times \frac{2}{6} \times \frac{[DLCDCONTCYC]+1}{[DLCDSTCLKCYC]+1}}$ |
| 3 COM 1/4 Duty | Von voltage | $\sqrt{V^2 \times \frac{3}{4} \times \frac{[DLCDCONTCYC]+1}{[DLCDSTCLKCYC]+1}}$ |
| | Voff voltage | $\sqrt{V^2 \times \frac{1}{4} \times \frac{[DLCDCONTCYC]+1}{[DLCDSTCLKCYC]+1}}$ |

Table 3.5 shows the register setting example for adjusting the contrast while keeping the frame frequency at about 80Hz when lck2=fs (32.768kHz).

**Table 3.5 Example of Contrast adjustment (fs)**

| Driving system | | Frame length control | Time division control |
|---|---|---|---|
| Non-Bias drive 4COM 1/6 Duty | | 80.31[Hz] | 80.31[Hz] |
| | ***[DLCDSTCLKCYC]***<STCYC[7:0]> | <STCYC[7:0]>+<CONT[7:0]>=66 | 67 |
| | ***[DLCDCONTCYC]***<CONT[7:0]> | | 0 to 67 |
| Non-Bias drive 3COM 1/4 Duty | | 80.31[Hz] | 80.31[Hz] |
| | ***[DLCDSTCLKCYC]***<STCYC[7:0]> | <STCYC[7:0]>+<CONT[7:0]>=100 | 101 |
| | ***[DLCDCONTCYC]***<CONT[7:0]> | | 0 to 101 |

Table 3.6 shows the register setting example for adjusting the contrast while keeping the frame frequency at about 80Hz when lck2=IHOSC2 (39.0625kHz).

**Table 3.6 Example of Contrast adjustment (IHOSC2)**

| Driving system | | Frame length control | Time division control |
|---|---|---|---|
| Non-Bias drive 4COM 1/6 Duty | | 80.38[Hz] | 80.38[Hz] |
| | ***[DLCDSTCLKCYC]***<STCYC[7:0]> | <STCYC[7:0]>+<CONT[7:0]>=79 | 80 |
| | ***[DLCDCONTCYC]***<CONT[7:0]> | | 0 to 80 |
| Non-Bias drive 3COM 1/4 Duty | | 80.05[Hz] | 80.05[Hz] |
| | ***[DLCDSTCLKCYC]***<STCYC[7:0]> | <STCYC[7:0]>+<CONT[7:0]>=120 | 120 |
| | ***[DLCDCONTCYC]***<CONT[7:0]> | | 0 to 120 |

# 3.4. LCD Display data buffer

## 3.4.1. Outline

The LCD display control circuit has a display buffer that holds display data of up to 160 pixels (40 SEG × 4 COM).

The display buffer consists of 40 × 8-bit registers, and each register is assigned to one display Segment.

The lower 4 bits in the 8-bit register are COM0 to COM3 for main display, and the upper 4 bits are COM0 to COM3 for sub display. Normally, the data on the main display side is selected.

The display Segment is turned on when the data bit for each Segment and Common of the display buffer is "1", and be turned off when the data bit is "0". Blink operation can be realized by selecting the display buffer in ***[DLCDCR2]***.

The main display and sub display are switched according to the buffer selection setting.

## 3.4.2. Display buffer configuration

After power-on reset, the register can select the Display buffer if only one source clock is operating.

**Table 3.7 Display buffer configuration (n= 0 to 39)**

| ***[DLCDCR2]*** | | **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit0** |
|---|---|---|---|---|---|---|---|---|---|
| | | **Sub display<SEGnH[3:0]>** | | | | **Main display<SEGnL[3:0]>** | | | |
| ***[DLCDBUF00]*** | SEG00 | COM3 | COM2 | COM1 | COM0 | COM3 | COM2 | COM1 | COM0 |
| ***[DLCDBUF01]*** | SEG01 | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| ***[DLCDBUF02]*** | SEG02 | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| ***[DLCDBUF03]*** | SEG03 | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| ***[DLCDBUF36]*** | SEG36 | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| ***[DLCDBUF37]*** | SEG37 | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| ***[DLCDBUF38]*** | SEG38 | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| ***[DLCDBUF39]*** | SEG39 | COM3 | COM2 | COM1 | COM0 | COM3 | COM2 | COM1 | COM0 |

## 3.4.3. Notice of using the display data buffer

When using the display buffer, note the following notice.

- The display data buffer is in an undefined state because it is not initialized by cold reset.
  Set the data before using display.
- Set the display data after setting the LCD drive method with ***[DLCDCR2]***<DUTY[1:0]>.
- When the LCD display data buffer is rewritten, the set value is executed and reflected immediately after rewriting within one frame.
- The display data buffer ***[DLCDBUFn]*** may have a discontinuous <SEGxx> pinout depending on the product implementation.
  For detail, refer to the reference manual "Product Information".

### 3.4.4. SEG/COM pin order switching

As for the SEG00 to SEG39 and DCOM0 to DCOM3 pins, the pin output order can be switched by setting ***[DLCDCR4]***<RVDPIN[2:0]> as shown below.

**Table 3.8 SEG/COM pin order switching**

| Output Pin | Output signal | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | RVDPIN=000 | RVDPIN=001 | RVDPIN=010 | RVDPIN=011 | RVDPIN=100 | RVDPIN=101 | RVDPIN=110 | RVDPIN=111 |
| SEG00 | seg00 | seg39 | seg00 | seg39 | dcom0 | ← | dcom3 | ← |
| SEG01 | seg01 | seg38 | seg01 | seg38 | dcom1 | ← | dcom2 | ← |
| SEG02 | seg02 | seg37 | seg02 | seg37 | dcom2 | ← | dcom1 | ← |
| SEG03 | seg03 | seg36 | seg03 | seg36 | dcom3 | ← | dcom0 | ← |
| SEG04 | seg04 | seg35 | seg04 | seg35 | seg00 | seg39 | seg00 | seg39 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| SEG35 | seg35 | seg04 | seg35 | seg04 | seg31 | seg08 | seg31 | seg08 |
| SEG36 | seg36 | seg03 | seg36 | seg03 | seg32 | seg07 | seg32 | seg07 |
| SEG37 | seg37 | seg02 | seg37 | seg02 | seg33 | seg06 | seg33 | seg06 |
| SEG38 | seg38 | seg01 | seg38 | seg01 | seg34 | seg05 | seg34 | seg05 |
| SEG39 | seg39 | seg00 | seg39 | seg00 | seg35 | seg04 | seg35 | seg04 |
| DCOM0 | dcom0 | ← | dcom3 | ← | seg36 | seg03 | seg36 | seg03 |
| DCOM1 | dcom1 | ← | dcom2 | ← | seg37 | seg02 | seg37 | seg02 |
| DCOM2 | dcom2 | ← | dcom1 | ← | seg38 | seg01 | seg38 | seg01 |
| DCOM3 | dcom3 | ← | dcom0 | ← | seg39 | seg00 | seg39 | seg00 |

The output pin differs depending on the product specifications. For detail, refer to the reference manual "Product Information" in each product.

## 3.5. Interrupt

This product has two interrupts to detect the timing of LCD control.

Since the LCD operation clock (about 32 to 39 kHz) is slower than the MCU operation clock (1 to 200 MHz), it is prepared to detect the end of register update and the timing during display blank operation

- INTLCDBUSF
  When the end of writing to the rewritable register is detected during operation, an interrupt pulse is output.

  Register for Interrupt : ***[DLCDCONTCYC]***, ***[DLCDSTCLKCYC]***, ***[DLCDCR3]***
  When the register is continuously rewritten to generate an interrupt, rewrite it within (Lck1 × 3) clocks. If it takes time to rewrite, an unexpected interrupt may occur.

- INTLCDSTOP
  When detecting the display blanking condition which is the display stop condition, an interrupt pulse is output.

# 4. Register

## 4.1. Register List

The register and address are shown below.

| Function name | | Channel/ unit | Base address | | |
|---|---|---|---|---|---|
| | | | Type1 | Type2 | Type3 |
| LCD Display Control Circuit | DLCD | - | 0x4003F200 | - | - |

Note: The channel/unit and base address type are different by products. Please refer to the reference manual "Product Information" for the details.

| Register | | Address (Base+) |
|---|---|---|
| LCD enable register | ***[DLCDEN]*** | 0x0000 |
| LCD control register 1 | ***[DLCDCR1]*** | 0x0001 |
| LCD control register 2 | ***[DLCDCR2]*** | 0x0002 |
| LCD control register 3 | ***[DLCDCR3]*** | 0x0003 |
| LCD control register 4 | ***[DLCDCR4]*** | 0x0004 |
| State clock control register | ***[DLCDSTCLKCYC]*** | 0x0005 |
| Contrast control register | ***[DLCDCONTCYC]*** | 0x0006 |
| Busy Flag register | ***[DLCDREGBSY]*** | 0x0008 |
| LCD Display data buffer register 00 | ***[DLCDBUF00]*** | 0x0010 |
| LCD Display data buffer register 01 | ***[DLCDBUF01]*** | 0x0011 |
| LCD Display data buffer register 02 | ***[DLCDBUF02]*** | 0x0012 |
| LCD Display data buffer register 03 | ***[DLCDBUF03]*** | 0x0013 |
| LCD Display data buffer register 04 | ***[DLCDBUF04]*** | 0x0014 |
| LCD Display data buffer register 05 | ***[DLCDBUF05]*** | 0x0015 |
| LCD Display data buffer register 06 | ***[DLCDBUF06]*** | 0x0016 |
| LCD Display data buffer register 07 | ***[DLCDBUF07]*** | 0x0017 |
| LCD Display data buffer register 08 | ***[DLCDBUF08]*** | 0x0018 |
| LCD Display data buffer register 09 | ***[DLCDBUF09]*** | 0x0019 |
| LCD Display data buffer register 10 | ***[DLCDBUF10]*** | 0x001A |
| LCD Display data buffer register 11 | ***[DLCDBUF11]*** | 0x001B |
| LCD Display data buffer register 12 | ***[DLCDBUF12]*** | 0x001C |
| LCD Display data buffer register 13 | ***[DLCDBUF13]*** | 0x001D |
| LCD Display data buffer register 14 | ***[DLCDBUF14]*** | 0x001E |
| LCD Display data buffer register 15 | ***[DLCDBUF15]*** | 0x001F |
| LCD Display data buffer register 16 | ***[DLCDBUF16]*** | 0x0020 |
| LCD Display data buffer register 17 | ***[DLCDBUF17]*** | 0x0021 |
| LCD Display data buffer register 18 | ***[DLCDBUF18]*** | 0x0022 |
| LCD Display data buffer register 19 | ***[DLCDBUF19]*** | 0x0023 |
| LCD Display data buffer register 20 | ***[DLCDBUF20]*** | 0x0024 |
| LCD Display data buffer register 21 | ***[DLCDBUF21]*** | 0x0025 |
| LCD Display data buffer register 22 | ***[DLCDBUF22]*** | 0x0026 |
| LCD Display data buffer register 23 | ***[DLCDBUF23]*** | 0x0027 |
| LCD Display data buffer register 24 | ***[DLCDBUF24]*** | 0x0028 |
| LCD Display data buffer register 25 | ***[DLCDBUF25]*** | 0x0029 |

| Register | | Address (Base+) |
|---|---|---|
| LCD Display data buffer register 26 | ***[DLCDBUF26]*** | 0x002A |
| LCD Display data buffer register 27 | ***[DLCDBUF27]*** | 0x002B |
| LCD Display data buffer register 28 | ***[DLCDBUF28]*** | 0x002C |
| LCD Display data buffer register 29 | ***[DLCDBUF29]*** | 0x002D |
| LCD Display data buffer register 30 | ***[DLCDBUF30]*** | 0x002E |
| LCD Display data buffer register 31 | ***[DLCDBUF31]*** | 0x002F |
| LCD Display data buffer register 32 | ***[DLCDBUF32]*** | 0x0030 |
| LCD Display data buffer register 33 | ***[DLCDBUF33]*** | 0x0031 |
| LCD Display data buffer register 34 | ***[DLCDBUF34]*** | 0x0032 |
| LCD Display data buffer register 35 | ***[DLCDBUF35]*** | 0x0033 |
| LCD Display data buffer register 36 | ***[DLCDBUF36]*** | 0x0034 |
| LCD Display data buffer register 37 | ***[DLCDBUF37]*** | 0x0035 |
| LCD Display data buffer register 38 | ***[DLCDBUF38]*** | 0x0036 |
| LCD Display data buffer register 39 | ***[DLCDBUF39]*** | 0x0037 |

Note: These registers cannot be accessed in the bit band, only byte access is possible.

## 4.2. Register descriptions

### 4.2.1. *[DLCDEN]* (LCD enable register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:1 | - | 0 | R | Read as "0" |
| 0 | LCDE | 0 | R/W | Operation of LCD display control circuit<br>0: Disable<br>1: Enable |

Note: To disable the operation of the LCD display control, set ***[DLCDCR1]***<EDSP[1:0]> to "00" in advance, and then set the <LCDE> to "0" after confirm that ***[DLCDCR1]***<LCDF> has been "0".

### 4.2.2. *[DLCDCR1]* (LCD Control register 1)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:5 | - | 0 | R | Read as "0" |
| 4 | LCDF | 0 | R | LCD Display control circuit status flag<br>0: Stopped<br>1: Operating |
| 3:2 | - | 0 | R | Read as "0" |
| 1:0 | EDSP[1:0] | 00 | R/W | LCD Display control<br>00/01: Display disable (SEG/COM "L" level output)<br>10: Display enable (SEG/COM Non-lighting operation)<br>11: Display enable (SEG/COM Lighting operation by the display buffer) |

Note: This register can change the setting during display operation.

### 4.2.3. *[DLCDCR2]* (LCD Control register 2)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:4 | - | 0 | R | Read as "0" |
| 3 | CONTSEL | 0 | R/W | Selection of Contrast control<br>0: Frame length control method<br>1: Time division control method |
| 2 | CLKSEL | 0 | R/W | Selection of clock source for LCD display control circuit<br>0: Internal High speed oscillator 2 (IHOSC2)<br>1: fs |
| 1:0 | DUTY[1:0] | 00 | R/W | LCD driving system setting<br>00 : 4COM 1/6 duty<br>01 : 3COM 1/4 duty<br>10 : reserved<br>11 : reserved |

Note: This register can change the setting only while the display is stopped.

### 4.2.4. *[DLCDCR3]* (LCD Control register 3)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7 | BFLG | 0 | R | Selection Flag of Display buffer area<br>0: Select ***[DLCDBUFn]***<SEGnL[3:0]> area<br>1: Select ***[DLCDBUFn]***<SEGnH[3:0]> area |
| 6:4 | - | 0 | R | Read as "0" |
| 3:2 | BTGL[1:0] | 00 | R/W | Selection of Display buffer by Event<br>00: Invalid (Initialize Internal Counter)<br>01: Toggle Buffer area for each External trigger event (Initialize Internal counter)<br>10: Toggle Buffer area every 2Hz<br>11: Toggle Buffer area every 4Hz |
| 1:0 | BSEL[1:0] | 00 | R/W | Selection of Display buffer by instruction<br>00: Buffer area not change (Select Lower area after reset)<br>01: Select ***[DLCDBUFn]***<SEGnL[3:0]> area data<br>10: Select ***[DLCDBUFn]***<SEGnH[3:0]> area data<br>11: Toggle Buffer area |

Note1: ***[DLCDBUFn]***<SEGnL[3:0]> is data for lower 4 bits of Display buffer, ***[DLCDBUFn]***<SEGnH[3:0]> is data for upper 4 bits of Display buffer.
Note2: Writing other than "00" to <BSEL[1:0]> is invalid, when <BTGL[1:0]> is other than "00".
Note3: When <BTGL[1:0]> and <BSEL[1:0]> are rewritten to other than "00" at the same time, the setting of <BTGL[1:0]> takes priority and <BSEL[1 :0]> is invalid.
Note4: The settings of <BTGL[1:0]> and <BSEL[1:0]> are reflected for each frame.
Note5: When using internal oscillation operation, toggle interval does not become 2Hz or 4Hz accuracy.
Note6: There is no External trigger depend on the product. For detail, refer to the reference manual "Product Information".
Note7: While the LCD display is disabled, <BFLG> is not reflected even if setting <BSEL[1:0]>.

### 4.2.5. *[DLCDCR4]* (LCD Control register 4)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:3 | - | 0 | R | Read as "0" |
| 2:0 | RVDPIN[2:0] | 000 | R/W | Control SEG/COM pin order switching<br>Refer to "Table 3.8 SEG/COM pin order switching" |

Note: This register can change the setting only while the display is stopped.

### 4.2.6. *[DLCDSTCLKCYC]* (State Clock Control register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:0 | STCYC[7:0] | 0x00 | R/W | Set State cycle<br>0x00 to 0xFF |

Note: This register can change the setting during display operation.

### 4.2.7. *[DLCDCONTCYC]* (Contrast Control register )

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:0 | CONT[7:0] | 0x00 | R/W | Set Contrast cycle.<br>0x00 to 0xFF |

Note: This register can change the setting during display operation.

### 4.2.8. *[DLCDREGBSY]* (Busy Flag register )

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:4 | - | 0 | R | Read as "0" |
| 3 | CONF | 0 | R | Status of Data transfer by ***[DLCDCONTCYC]*** register<br>0: Transmission completed, Not data transfer<br>1: While data transfer |
| 2 | STCF | 0 | R | Status of Data transfer by ***[DLCDSTCLKCYC]*** register<br>0: Transmission completed, Not data transfer<br>1: While data transfer |
| 1 | CR3F | 0 | R | Status of Data transfer by ***[DLCDCR3]*** register<br>0: Transmission completed, Not data transfer<br>1: While data transfer |
| 0 | CR1F | 0 | R | Status of Data transfer by ***[DLCDCR1]*** register<br>0: Transmission completed, Not data transfer<br>1: While data transfer |

### 4.2.9. *[DLCDBUFn]* (LCD Display buffer register n=00 to 39)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 7:4 | SEGnH[3:0] | undefined | R/W | SEGnH Data<br>[3]: COM3 data of SEGnH<br>[2]: COM2 data of SEGnH<br>[1]: COM1 data of SEGnH<br>[0]: COM0 data of SEGnH |
| 3:0 | SEGnL[3:0] | undefined | R/W | SEGnL Data<br>[3]: COM3 data of SEGnL<br>[2]: COM2 data of SEGnL<br>[1]: COM1 data of SEGnL<br>[0]: COM0 data of SEGnL |

Note: When writing to this register, dummy data is generated and held, so it is necessary to determine the LCD drive method in advance with ***[DLCDCR2]***<DUTY[1:0]>.

# 5. Usage Example

## 5.1. Procedure of LCD Display starting

The procedure to start LCD Display after reset is as follows.

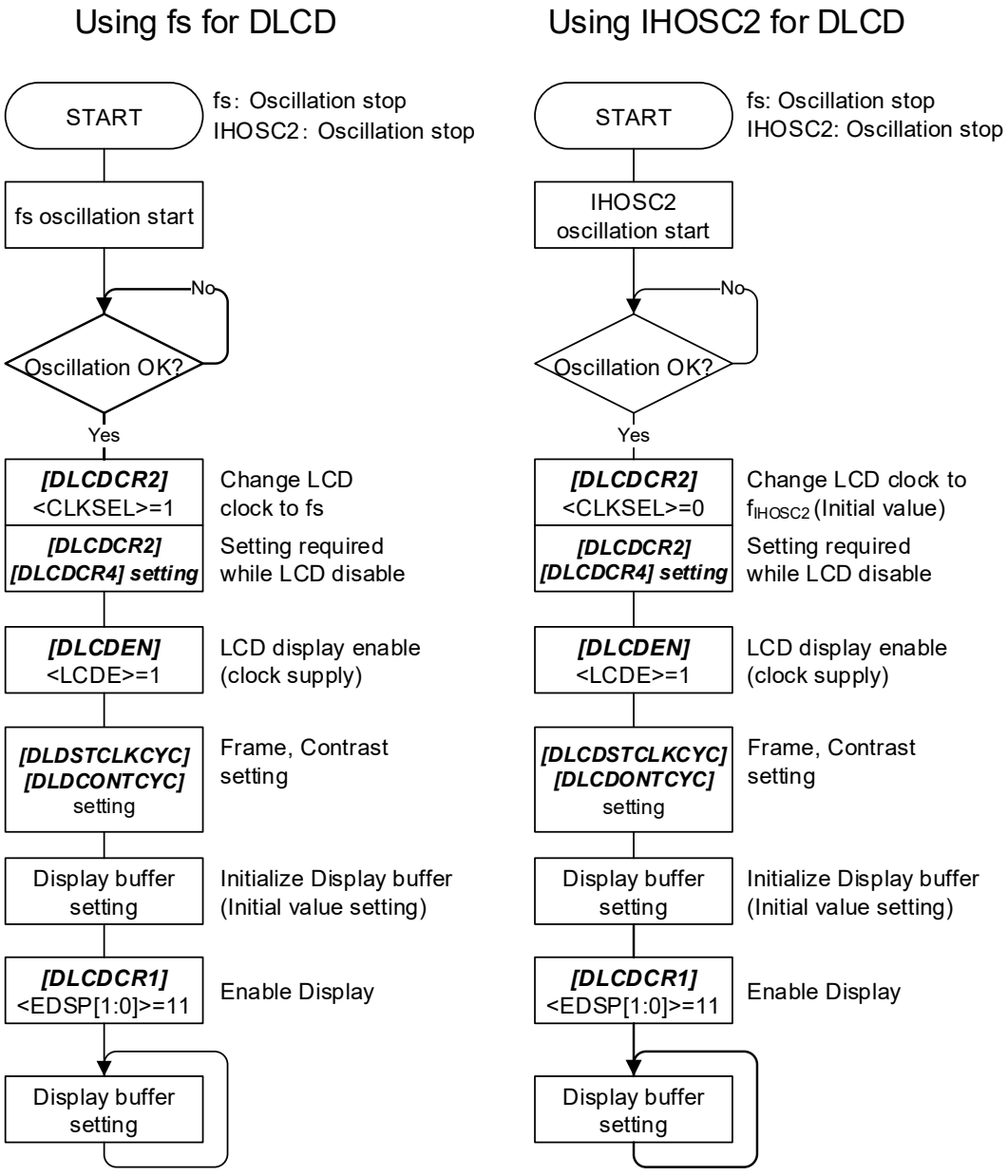


**Figure 5.1 Procedure of LCD Display after reset**

Note1: When using fs as the LCD clock, set ***[DLCDCR2]***<CLKSEL>=1 and then ***[DLCDEN]***<LCDE>=1 after confirming that fs oscillation is stable (after warming up).
Note2: Set the display buffer after setting ***[DLCDCR2]***<DUTY[1:0]>.
Note3: When switching from display disable to display enable, if the double buffer register is being transferred, SEG/COM is held at "L" level until the transfer is completed.

## 5.2. Procedure of LCD Display stopping

To stop the LCD display, follow the procedure below. There are two ways to stop LCD display, one is to continuously output non-display data and the other is to output "L" level from the SEG/COM pin.

In the latter case, the LCD clock can be stopped if necessary.

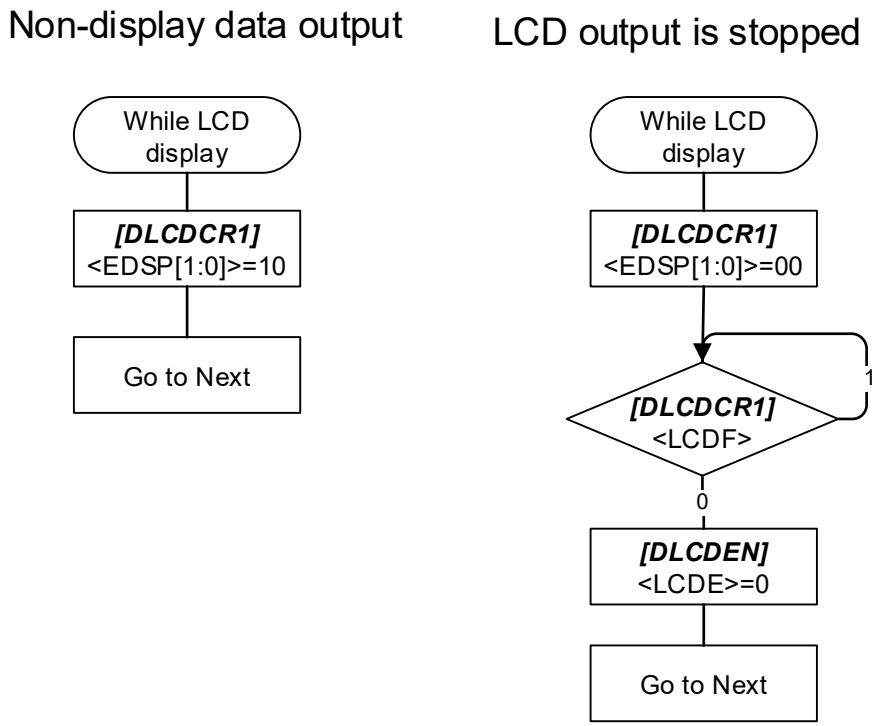


**Figure 5.2 LCD Display stop procedure**

Note: To set ***[DLCDEN]***<LCDE>=0, set ***[DLCDCR1]***<EDSP[1:0]>=00 in advance, and then set ***[DLCDEN]***<LCDE>=0 after ***[DLCDCR1]***<LCDF>=0.

## 5.3. Procedure of register changing while LCD Display on

Use the following procedure to set the registers that can be changed when the LCD display is on.

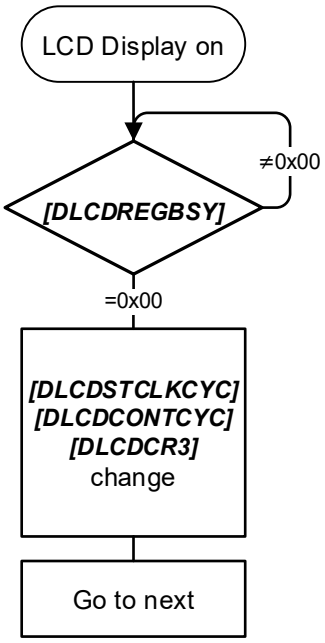


**Figure 5.3 Procedure of register changing while LCD Display on**

Note1: ***[DLCDCR3]***, ***[DLCDSTCLKCYC]***, and ***[DLCDCONTCYC]*** can be rewritten during LCD display on. However, check the transfer status with the ***[DLCDREGBSY]*** register before writing. If rewriting the register during transfer, the data transfer may fail and invalid data may continue to be processed.

Note2: It is prohibited to change ***[DLCDCR3], [DLCDSTCLKCYC],*** and ***[DLCDCONTCYC]*** continuously more than once. For the second and subsequent changes, make sure ***[DLCDREGBSY]*** = 00.

## 5.4. Procedure of LCD clock switching

To switch the LCD display clock, please set registers according to the following procedure

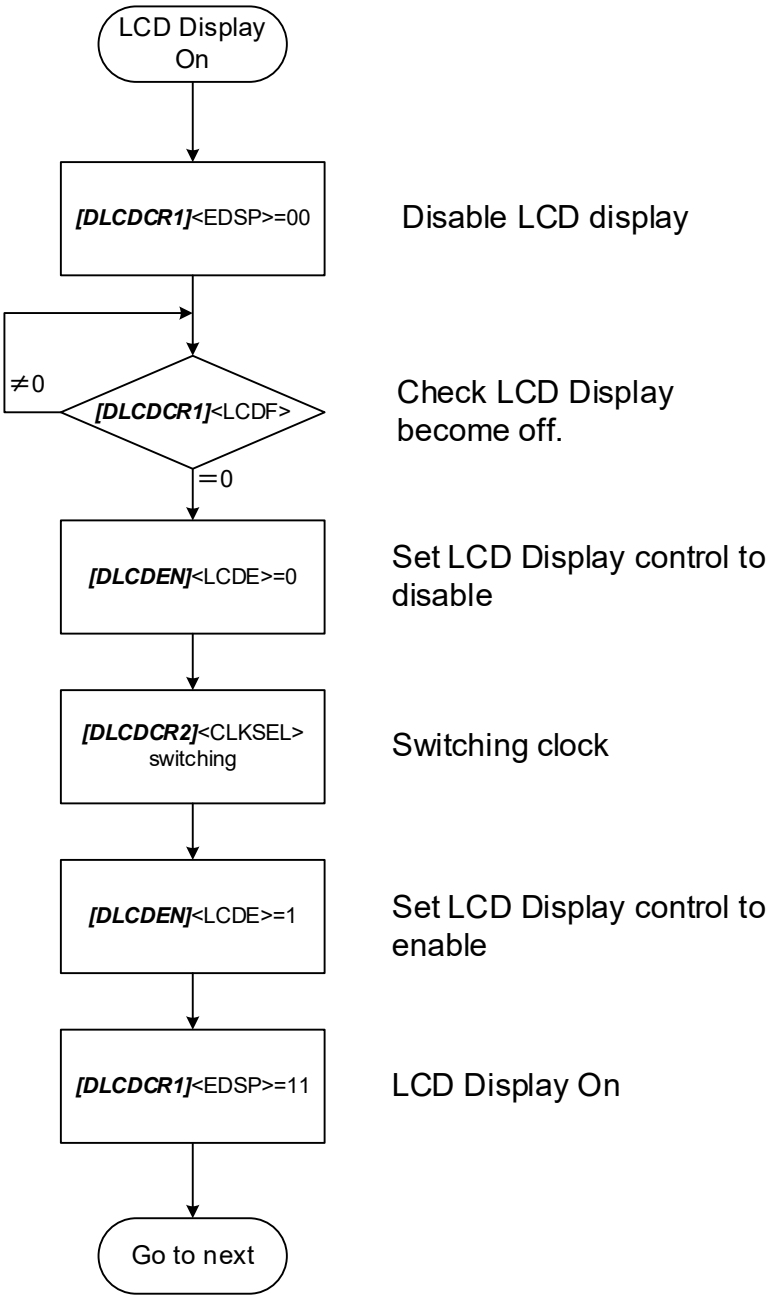


**Figure 5.4 Procedure of LCD clock switching**

## 5.5. Precautions when selecting the source clock

After power-on reset, if only one of the source clocks is operating, the register selection is possible.

When stopping the LCD display operation by setting ***[DLCDEN]***<LCDE >=0 and then restarting the operation by setting ***[DLCDEN]***<LCDE >= 1, use the source clock that was used immediately before. (Do not change the source clock selection while LCD operation is stopped)

When switching the source clock selection with ***[DLCDCR2]***<CLKSEL>, make sure that both oscillations are stable.

# 6. Precautions

- Set the initial value of PORT shared with COM pin to "L" output.
- Do not access the address that is not assigned register.

# 7. Revision History

**Table 7.1 Revision history**

| Revision | Date | Description |
|---|---|---|
| 1.0 | 2020-12-21 | First release |

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