July 2005

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

Restriction on Use of 8-bit Timers (July 2005)

*If your datasheet is dated 10 May 2005 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers 900 Family
(TMP91CW12F) (TMP91PW12F) (TMP91CW12AF) (TMP91FY12AF) (TMP91C815F) (TMP91C016F)
(TMP91CW18AF) (TMP91PW18AF) (TMP91C219F) (TMP91C820AF) (TMP91CY22F)
(TMP91FY22F) (TMP91C824F) (TMP91C025F) (TMP91CK27U) (TMP91CP27U)
(TMP91CP27RUG) (TMP91CU27U) (TMP91CU27RUG) (TMP91FY27U) (TMP91CW28FG)
(TMP91CY28FG) (TMP91FY28FG) (TMP91C829F) (TMP91C630F)
(TMP92C820FG) (TMP92CH21FG) (TMP92CM22FG) (TMP92CA25FG) (TMP92CM27FG)
(TMP92CD54IF) (TMP92FD54AIF)
(TMP94C241CF) (TMP94C251AF)

Dear Customer July 2005

Restriction on Use of 8-bit Timers

With regard to our TLCS-900/L1 Series and TLCS-900/H1 Series of 16-bit microcontrollers, we have found that the following problem may occur when 8-bit timers are used under certain conditions.

[Problem]

If the timer register of an 8-bit timer is updated under the following conditions, the timer flip-flop may output an unexpected value.

[Conditions]

This problem occurs if all the following conditions are met:

- When the 8-bit timer is used in PWM or PPG mode
- When the double buffer is enabled
- When the data in the register buffer is updated immediately before an overflow occurs in the up-counter

[Workaround]

This problem can be avoided by software by using either of the following methods:

(1) Disable the double buffer.

(After reset the double buffer is initially disabled.)

(2) Observe the following timing requirement when writing new data to the register buffer:

a) In the case of using PWM mode

Write new data to the register buffer by six cycles before the next overflow occurs, using the interrupt routine to be activated by an overflow interrupt.

b) In the case of using PPG mode

Write new data to the register buffer by six cycles before the next cycle compare match occurs, using the interrupt routine to be activated by a cycle compare match interrupt (*).

(*) An interrupt that specifies when to transfer data from the register buffer to the timer register

[Note]

When the double buffer is enabled for an 8-bit timer in PWM or PPG mode, caution is required as explained below.

If new data is written to the register buffer immediately before an overflow occurs by a match between the timer register value and the up-counter value, the timer flip-flop may output an unexpected value.

For this reason, make sure that in PWM mode new data is written to the register buffer by six cycles (fsys x 6) before the next overflow occurs by using an overflow interrupt.

In the case of using PPG mode, make sure that new data is written to the register buffer by six cycles before the next cycle compare match occurs by using a cycle compare match interrupt.

Example when using PWM mode