TOSHIBA

October 2004

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

Datasheet Modifications regarding I^2C Bus Mode Control (October 2004)

*If your datasheet is dated 9 February 2004 or earlier, please download the latest datasheet or request it from your local Toshiba office.

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TOSHIBA Microcontrollers
900 Family
(TMP93CS20) (TMP93PW20A)
(TMP93PS44) (TMP93CU44) (TMP93PW44A) (TMP93CW44) (TMP93CS44/45)

October 2004

Datasheet Modifications: I²C Bus Mode Control

The following modifications (shown in red) will be made to the technical datasheets in the next revision.

Section: "I²C Bus Mode Control"

▪ **In the explanation of the Serial Bus Interface Control Register 1**

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

Serial clock selection

000	N = 4	- (Note)	System clock: fc Clock gear : fc/1 fc = 20 MHz (Output on SCL pin)
001	N = 5	- (Note)	
010	N = 6	- (Note)	
011	N = 7	74.6 kHz	
100	N = 8	38.2 kHz	
101	N = 9	19.3 kHz	
110	N = 10	9.71 kHz	
111		Reserved	

Note: This I²C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I²C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I²C specification is not guaranteed in that case.

▪ **In "(3) Serial clock"**

1. Add the following sentence about the communication baud rate.

a. Clock source

SBICR1<SCK2:0> are used to select a maximum transfer frequency output on the SCL pin in the master mode. **Set a communication baud rate that meets the I²C bus specification, such as the shortest pulse width of t_{LOW}, based on the equations shown below.**

$$t_{LOW} = 2^n/f_{FPH}$$
$$t_{HIGH} = 2^n/f_{FPH} + 12/f_{FPH}$$
$$fscl = 1/(t_{Low} + t_{HIGH})$$
$$= \frac{f_{FPH}}{2x2^n + 12}$$