

October 2004

## **Important Notices**

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

### ▶ **Datasheet Modifications regarding I<sup>2</sup>C Bus Mode Control** (October 2004)

\*If your datasheet is dated 31 March 2003 or earlier, please download the latest datasheet or request it from your local Toshiba office.

**TOSHIBA Microcontrollers**  
**900 Family**  
**(TMP91CW11) (TMP91PW11)**

October 2004

## Datasheet Modifications: I<sup>2</sup>C Bus Mode Control

The following modifications (shown in red) will be made to the technical datasheets in the next revision.

- In the explanation of the serial bus interface control register 1 in “3.10.4 I<sup>2</sup>C Bus Mode Control”, “3.11.4 I<sup>2</sup>C Bus Mode Control”, and “3.12.4 I<sup>2</sup>C Bus Mode Control”
  1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
  2. Add the following note.

Internal serial clock selection

|     |          |                                                                                                                                                    |
|-----|----------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 000 | - (Note) | $\left( \begin{array}{l} \text{System clock: } f_c \\ \text{Clock gear: } f_c/1 \\ f_c = 20 \text{ MHz (internal SCL output)} \end{array} \right)$ |
| 001 | - (Note) |                                                                                                                                                    |
| 010 | - (Note) |                                                                                                                                                    |
| 011 | 75.8 kHz |                                                                                                                                                    |
| 100 | 38.5 kHz |                                                                                                                                                    |
| 101 | 19.4 kHz |                                                                                                                                                    |
| 110 | 9.73 kHz |                                                                                                                                                    |
| 111 | Reserved |                                                                                                                                                    |

**Note:** This I<sup>2</sup>C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I<sup>2</sup>C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I<sup>2</sup>C specification is not guaranteed in that case.

- In “3.10.5 Control in I<sup>2</sup>C Bus Mode”, “3.11.5 Control in I<sup>2</sup>C Bus Mode”, and “3.12.5 Control in I<sup>2</sup>C Bus Mode”
  1. Add the following sentence about the communication baud rate.
  2. Modify the equations as shown below.

### (3) Serial clock

#### 1. Clock source

SBI0CR1X<SCK2:0> is used to specify the maximum transfer frequency for output on the SCL pin in Master mode. **Set a communication baud rate that meets the I<sup>2</sup>C bus specification, such as the shortest pulse width of  $t_{LOW}$ , based on the equations shown below.**

$$\begin{aligned}
 t_{LOW} &= 2^{n-1}/f_{SBI} \\
 t_{HIGH} &= 2^{n-1}/f_{SBI} + 8/f_{SBI} \\
 f_{SCL} &= 1/(t_{LOW} + t_{HIGH}) \\
 &= \frac{f_{SBI}}{2^n + 8}
 \end{aligned}$$