

July 2005

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

▶ **Announcement of Restrictions on Use of 8-bit Timer** (July 2005)

*If your datasheet is dated 16 February 2004 or earlier, please download the latest datasheet or request it from your local Toshiba office.

▶ **Datasheet Modifications regarding I²C Bus Mode Control** (October 2004)

▶ **Datasheet Modifications: PWM Cycle of 8-bit Timers** (October 2004)

*If your datasheet is dated 15 February 2004 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers 900 Family

(TMP91CW12F) (TMP91PW12F) (TMP91CW12AF) (TMP91FY12AF) (TMP91C815F) (TMP91C016F)
(TMP91CW18AF) (TMP91PW18AF) (TMP91C219F) (TMP91C820AF) (TMP91CY22F)
(TMP91FY22F) (TMP91C824F) (TMP91C025F) (TMP91CK27U) (TMP91CP27U)
(TMP91CP27RUG) (TMP91CU27U) (TMP91CU27RUG) (TMP91FY27U) (TMP91CW28FG)
(TMP91CY28FG) (TMP91FY28FG) (TMP91C829F) (TMP91C630F)
(TMP92C820FG) (TMP92CH21FG) (TMP92CM22FG) (TMP92CA25FG) (TMP92CM27FG)
(TMP92CD54IF) (TMP92FD54AIF)
(TMP94C241CF) (TMP94C251AF)

Dear Customer

July 2005

Restriction on Use of 8-bit Timers

With regard to our TLCS-900/L1 Series and TLCS-900/H1 Series of 16-bit microcontrollers, we have found that the following problem may occur when 8-bit timers are used under certain conditions.

[Problem]

If the timer register of an 8-bit timer is updated under the following conditions, the timer flip-flop may output an unexpected value.

[Conditions]

This problem occurs if all the following conditions are met:

- When the 8-bit timer is used in PWM or PPG mode
- When the double buffer is enabled
- When the data in the register buffer is updated immediately before an overflow occurs in the up-counter

[Workaround]

This problem can be avoided by software by using either of the following methods:

- (1) Disable the double buffer.

(After reset the double buffer is initially disabled.)

- (2) Observe the following timing requirement when writing new data to the register buffer:

- a) In the case of using PWM mode

Write new data to the register buffer by six cycles before the next overflow occurs, using the interrupt routine to be activated by an overflow interrupt.

- b) In the case of using PPG mode

Write new data to the register buffer by six cycles before the next cycle compare match occurs, using the interrupt routine to be activated by a cycle compare match interrupt (*).

(*) An interrupt that specifies when to transfer data from the register buffer to the timer register

[Note]

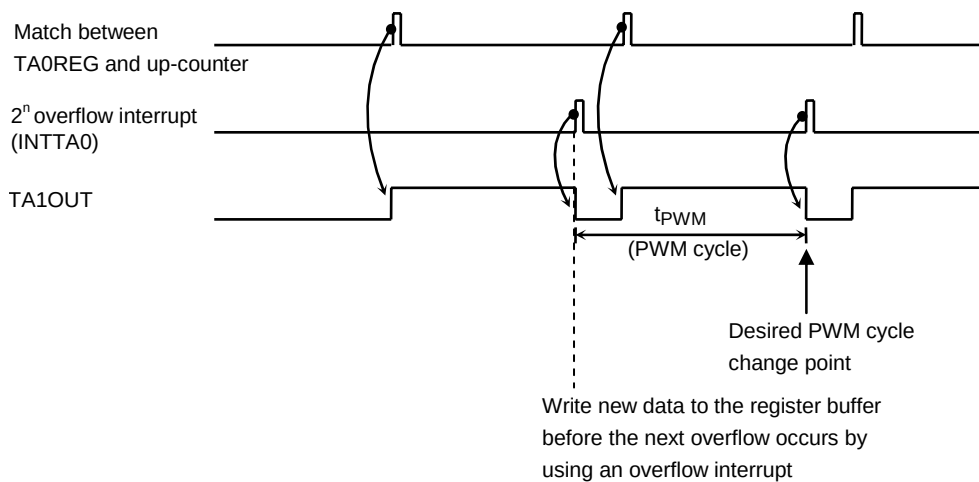
When the double buffer is enabled for an 8-bit timer in PWM or PPG mode, caution is required as explained below.

If new data is written to the register buffer immediately before an overflow occurs by a match between the timer register value and the up-counter value, the timer flip-flop may output an unexpected value.

For this reason, make sure that in PWM mode new data is written to the register buffer by six cycles ($f_{\text{sys}} \times 6$) before the next overflow occurs by using an overflow interrupt.

In the case of using PPG mode, make sure that new data is written to the register buffer by six cycles before the next cycle compare match occurs by using a cycle compare match interrupt.

Example when using PWM mode



TOSHIBA Microcontrollers

900 Family

(TMP91CW12) (TMP91PW12) (TMP91CW12A) (TMP91FY12A)

(TMP91CY22) (TMP91FY22)

(TMP91CY23I)

(TMP91CP27) (TMP91FY27)

(TMP91C815) (TMP91C820A) (TMP91C824)

October 2004

Datasheet Modifications: I²C Bus Mode Control

The following modifications (shown in red) will be made to the technical datasheets in the next revision.

Section: "I²C Bus Mode Control Register"

■ In the explanation of the Serial Bus Interface Control Register 1

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

Internal serial clock selection <SCK2:0> @ write

000	n=5	- (Note)	$\left(\begin{array}{l} \text{System clock: } f_c \\ \text{Clock gear: } f_c/1 \\ f_c = 16 \text{ MHz} \\ \text{(Output to internal SCL)} \\ \text{Frequency} = \frac{f_c}{2^n + 8} \text{ [Hz]} \end{array} \right)$
001	n=6	- (Note)	
010	n=7	- (Note)	
011	n=8	60.6 kHz	
100	n=9	30.8 kHz	
101	n=10	15.5 kHz	
110	n=11	7.78 kHz	
111		Reserved	

Note: This I²C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I²C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I²C specification is not guaranteed in that case.

Section: "Control in I²C Bus Mode"

■ In "(3) Serial clock"

1. Add the following sentence about the communication baud rate.
2. Modify the equations as shown below.

a. Clock source

The SBI0CR1<SCK2:0> is used to select a maximum transfer frequency outputted on the SCL pin in master mode. **Set a communication baud rate that meets the I²C bus specification, such as the shortest pulse width of t_{LOW}, based on the equations shown below.**

$$t_{\text{LOW}} = 2^{n-1} / f_{\text{SBI}}$$

$$t_{\text{HIGH}} = 2^{n-1} / f_{\text{SBI}} + 8 / f_{\text{SBI}}$$

$$f_{\text{SCL}} = 1 / (t_{\text{LOW}} + t_{\text{HIGH}})$$

$$= \frac{f_{\text{SBI}}}{2^n + 8}$$

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(TMP91C016) (TMP91CW18A) (TMP91PW18A) (TMP91C219)
(TMP91C820A) (TMP91CY22) (TMP91FY22) (TMP91CY23I) (TMP91C824) (TMP91C025)
(TMP91CP27) (TMP91FY27) (TMP91CW28) (TMP91CY28) (TMP91FY28)
(TMP91C829) (TMP91C630) (TMP91CP82T) (TMP91PP82T)
(TMP92C820) (TMP92CH21) (TMP92CM22)
(TMP92CW53I) (TMP92CW53AI) (TMP94FD53) (TMP92FD54AI) (TMP92CD54I)

Dear Customer

October 2004

Datasheet Modifications: PWM Cycle of 8-bit Timers

With regard to the TLCS-900/L1 and TLCS-900/H1 microcontrollers listed above, please be advised of the modifications to be made to the technical datasheets about the PWM cycle of 8-bit timers in PWM mode.

[Modifications to be made]

In the datasheet the PWM cycle of 8-bit timers when used in PWM mode is described as " 2^n-1 ". This should be corrected to " 2^n " as shown below.

TMRA01Mode Register									
TA01MOD (xxxxH)	7	6	5	4	3	2	1	0	
	bit Symbol	TA01M1	TA01M0	PWM01	PWM00	TA1CLK1	TA1CLK0	TA0CLK1	TA0CLK0
	Read/Write	R/W							
	After reset	0	0	0	0	0	0	0	0
Function	Operation mode		PWM cycle		Source clock for TMRA1		Source clock for TMRA0		
	00: 8-bit timer mode		00: Reserved		00: TA0TRG		00: TA0IN pin		
	01: 16-bit timer mode		01: 2 ⁶ -1		01: φT1		01: φT1		
	10: 8-bit PPG		10: 2 ⁷ -1		10: φT16		10: φT4		
	11: 8-bit PWM		11: 2 ⁸ -1		11: φT256		11: φT16		

PWM cycle

00: Reserved

01: 2⁶

10: 2⁷

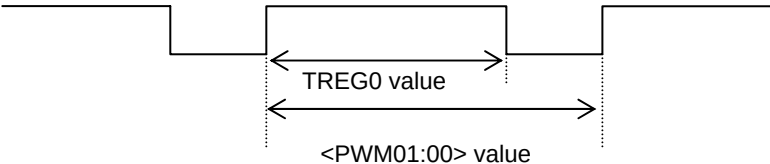
11: 2⁸

Correct

(The mode register for 8-bit timer TMRA01 is shown here as an example.)

[Operation]

Waveform in PWM mode (in the case of 8-bit timer TMRA01)



Datasheet Actual cycle

PWM cycle: 2^n-1 $\Rightarrow$ 2^n