October 2004

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

- **Datasheet Modifications regarding I^2C Bus Mode Control** (October 2004)

  *If your datasheet is dated 15 December 2000 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA

TOSHIBA Microcontrollers
870 Family
(TMP87C444) (TMP87C844) (TMP87P844)
(TMP87CH36) (TMP87CK36) (TMP87CM36)(TMP87PM36)
(TMP87CH38) (TMP87CK38) (TMP87CM38) (TMP87CP38) (TMP87CS38) (TMP87PS38)
(TMP87CM39) (TMP87CP39) (TMP87CS39) (TMP87PS39)
(TMP87CH74A) (TMP87CM74A) (TMP87PM74)
(TMP87CH75) (TMP87CM75) (TMP87PM75)
(TMP8701CH) (TMP8701CK) (TMP8701CM)
(TMPA8700CH) (TMPA8700CK) (TMPA8700CM) (TMPA8700CP) (TMPA8700CS)

October 2004

Datasheet Modifications: I²C Bus Mode Control

The following changes (shown in red) will be made to the technical datasheets in the next revision.

Section: "I²C Bus Mode Control"

▪ **In the explanation of the Serial Bus Interface Control Register 1**

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

SCK	Serial clock selection	000 : Reserved 001 : Reserved 010 : 57.1 kHz 011 : 29.9 kHz 100 : 15.3 kHz 101 : 7.72 kHz 110 : 3.88 kHz 111 : reserved	(Note) (Note)	at fc = 8MHz (Output on SCL pin)	Write only

Note: This I²C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I²C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I²C specification is not guaranteed in that case.

▪ **In "(3) Serial clock"**

1. Add the following sentence about the communication baud rate.

a. Clock source

The SCK (bits 2 to 0 in the SBICR1) is used to select a maximum transfer frequency outputed on the SCL pin in the master mode. **Set a communication baud rate that meets the I²C bus specification, such as the shortest pulse width of t_{LOW}, based on the equations shown below.**

Four or more machine cycles are required for both the high and low levels of the pulse width of a clock which is input externally in both the master and slave mode.

$t_{LOW} = 2^n/f_c$

$t_{HIGH} = 2^n/f_c + 12/f_c$

$fscl = 1/(t_{Low} + t_{HIGH})$