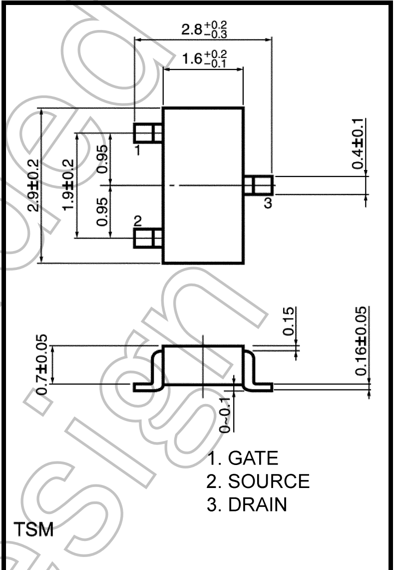
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K303T

High Speed Switching Applications

Unit: mm

- 4 V drive
- Low ON-resistance: R_{on} = 120 mΩ (max) (@V_{GS} = 4V)
  R_{on} = 83 mΩ (max) (@V_{GS} = 10V)



JEDEC	―
JEITA	―
TOSHIBA	2-3S1A

Weight: 10 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain–source voltage		V_{DS}	30	V
Gate–source voltage		V_{GSS}	± 20	V
Drain current	DC	I_D	2.9	A
	Pulse	I_{DP}	5.8	
Drain power dissipation		P_D (Note 1)	700	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/ voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

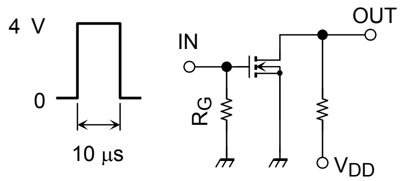
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain–source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0	30	―	―	V
Drain cutoff current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0	―	―	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	―	―	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 5 V, I_D = 1 mA	1.1	―	2.6	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 5 V, I_D = 1.5 A (Note2)	2.5	4.9	―	S
Drain–source ON-resistance		$R_{DS(ON)}$	I_D = 1.5 A, V_{GS} = 10 V (Note2)	―	64	83	mΩ
			I_D = 1.0 A, V_{GS} = 4 V (Note2)	―	88	120	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	―	180	―	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	―	100	―	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	―	38	―	pF
Total Gate Charge		Q_g	V_{DS} = 15 V, I_{DS}= 2.9 A, V_{GS} = 4 V	―	3.3	―	nC
Gate–Source Charge		Q_{gs}		―	1.4	―	
Gate–Drain Charge		Q_{gd}		―	1.9	―	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 1.5 A, V_{GS} = 0 to 4 V, R_G = 10 Ω	―	13	―	ns
	Turn-off time	t_{off}		―	14	―	
Drain–source forward voltage		V_{DSF}	I_D = − 2.9 A, V_{GS} = 0 V (Note2)	―	− 0.9	− 1.25	V

Note2: Pulse test

Start of commercial production
2007-09

Switching Time Test Circuit

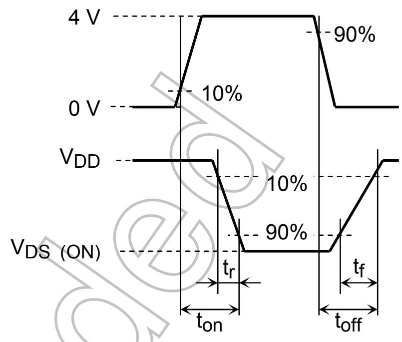
(a) Test Circuit



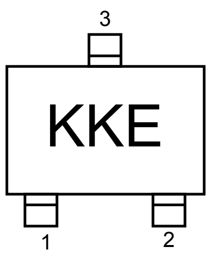
V_{DD} = 10 V
R_G = 10 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

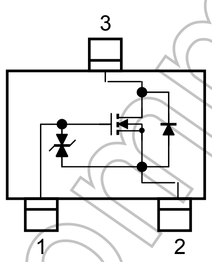
(c) V_{OUT}



Marking



Equivalent Circuit (top view)



Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = 1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.

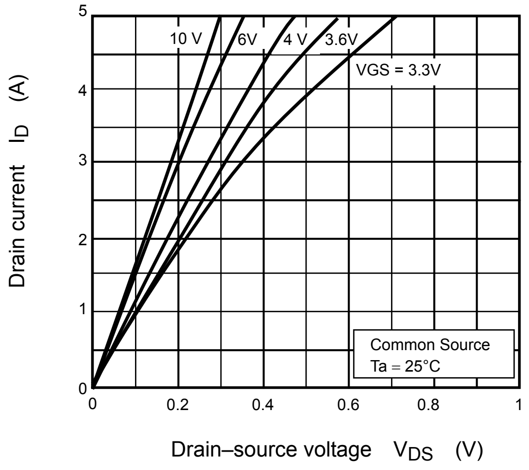
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

Take this into consideration when using the device.

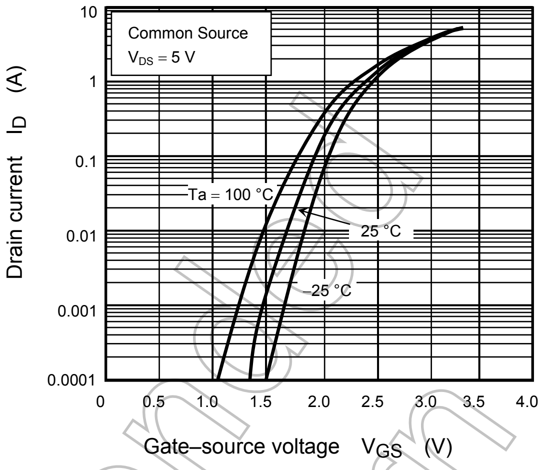
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

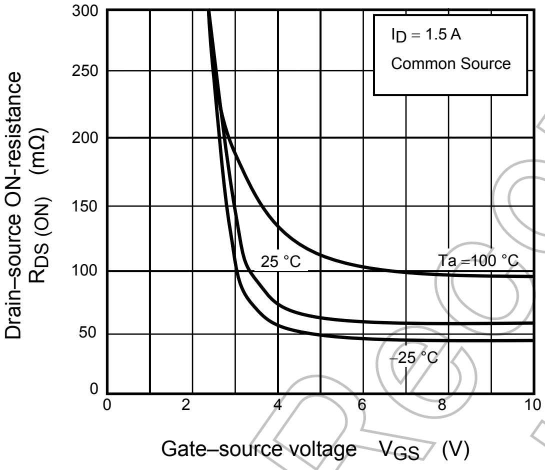
I_D – V_{DS}



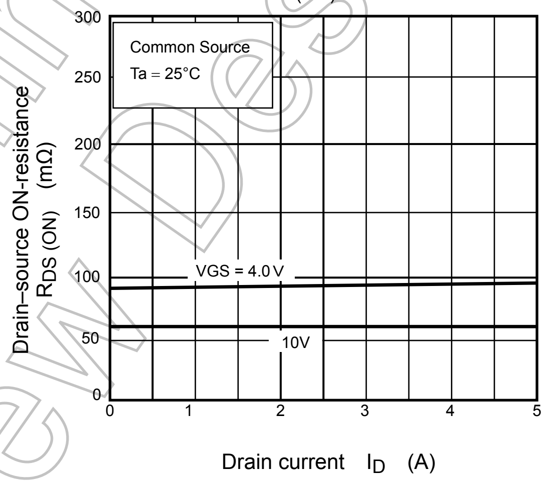
I_D – V_{GS}



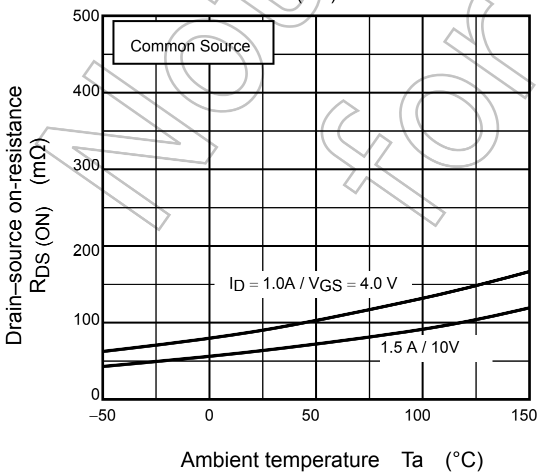
$R_{DS\,(ON)}$ – V_{GS}



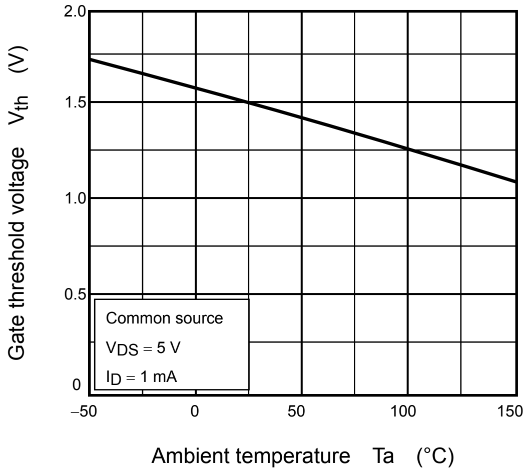
$R_{DS\,(ON)}$ – I_D

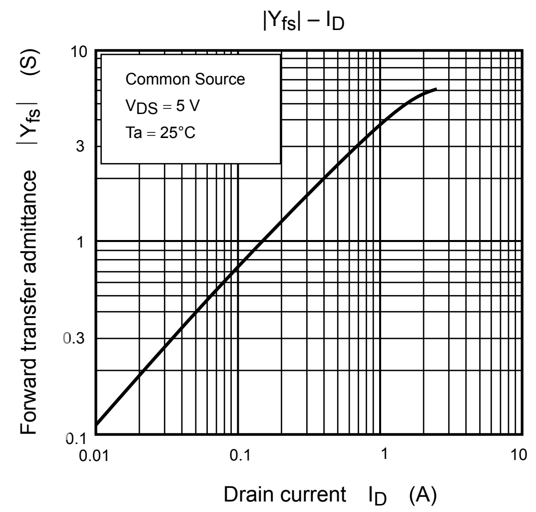


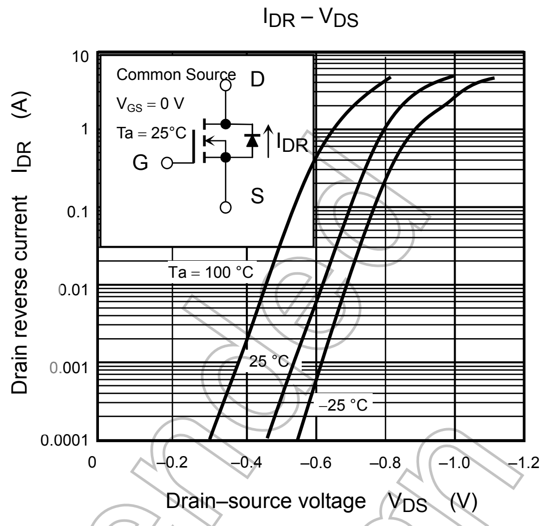
$R_{DS\,(ON)}$ – Ta

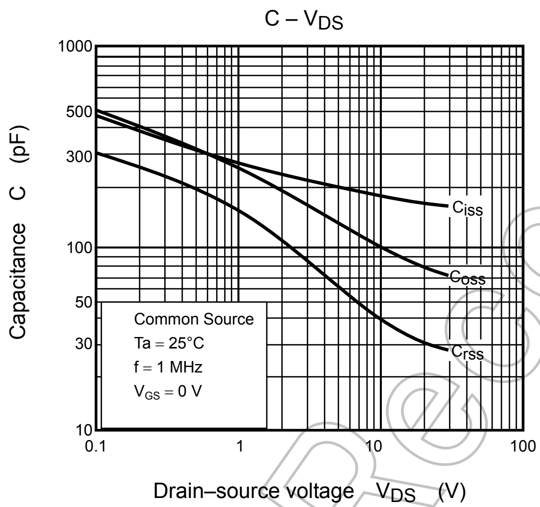


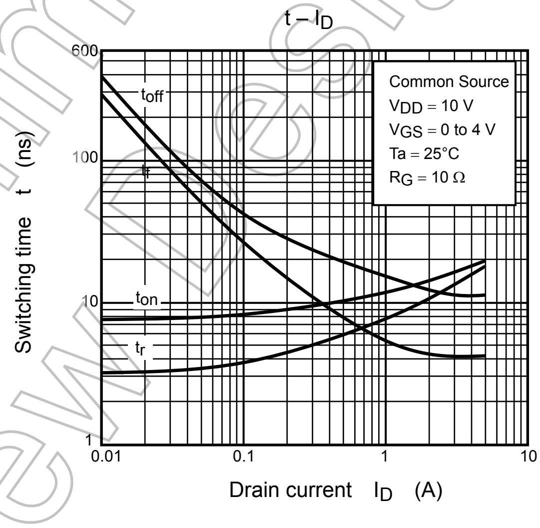
V_{th} – Ta

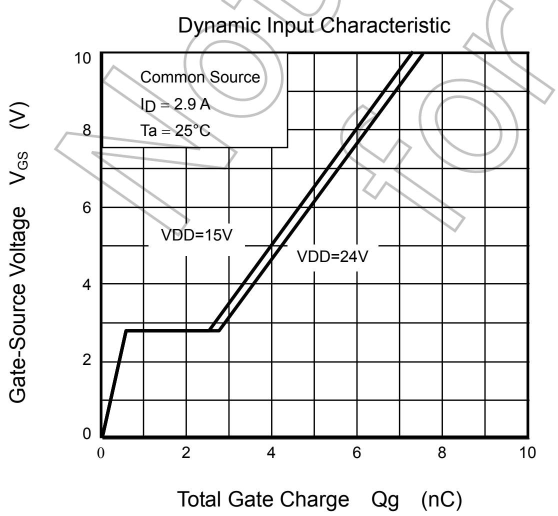


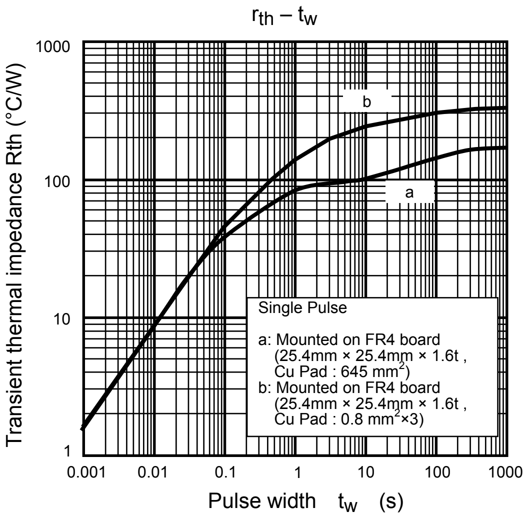

|Yfs| – ID
Common Source
VDS = 5 V
Ta = 25°C
Forward transfer admittance |Yfs| (S)
Drain current ID (A)

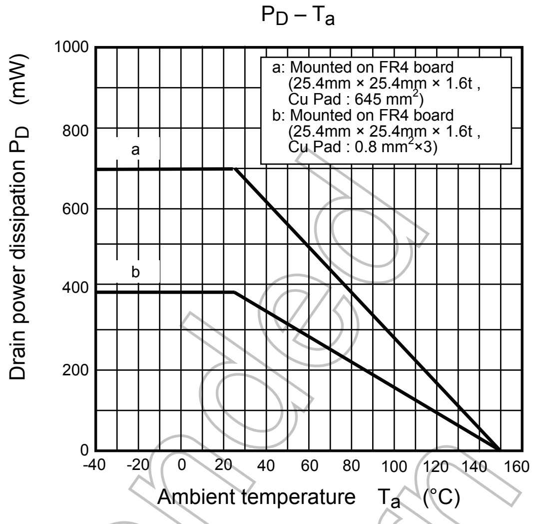

IDR – VDS
Common Source
VGS = 0 V
Ta = 25°C
D
G
S
IDR
Ta = 100 °C
25 °C
−25 °C
Drain reverse current IDR (A)
Drain–source voltage VDS (V)


C – VDS
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
Drain–source voltage VDS (V)


t – ID
toff
tf
ton
tr
Common Source
VDD = 10 V
VGS = 0 to 4 V
Ta = 25°C
RG = 10 Ω
Switching time t (ns)
Drain current ID (A)


Dynamic Input Characteristic
Common Source
ID = 2.9 A
Ta = 25°C
VDD=15V
VDD=24V
Gate-Source Voltage VGS (V)
Total Gate Charge Qg (nC)


r_{th} – t_w
Transient thermal impedance Rth (°C/W)
Pulse width t_w (s)
b
a
Single Pulse
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6t ,
Cu Pad : 645 mm^2)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6t ,
Cu Pad : 0.8 mm^2×3)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000


P_D – T_a
Drain power dissipation P_D (mW)
Ambient temperature T_a (°C)
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6t ,
Cu Pad : 645 mm^2)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6t ,
Cu Pad : 0.8 mm^2×3)
a
b
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160

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