32-bit RISC Microcontroller

TXZ+ Family

Reference manual

Operational Amplifier (OPAMP-B)

Revision 1.0

2020-10

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
AMP	Amplifier
OPAMP	Operational Amplifier

1. Outline

The OPAMP amplifies a port input voltage and outputs it to the 12-bit analog to digital converter (ADC). This circuit is used to amplify the voltage of the shunt resistor that detects the motor current.

Function classification	Function	Operation explanation
Input	Voltage Input (Differential input type)	Differential input of the voltage both ends of the shunt resistor that detects the motor current.
	Amplifier function control	When not using OPAMP, the input can be out put directly to the next stage by bypassing the OPAMP.
Amplification	Amplification of input voltage	It amplifies the differential input voltage. The gain can be selected from 12 levels. Gain: 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 6x, 7x, 8x, 10x, 12x, 15x
Output	Voltage Output	It outputs the amplified voltage to the ADC.

2. Configuration

This OPAMP has two OPAMP inputs and one OPAMP output, consists of the OPAMP main body, bypass circuit and OPAMP control register.

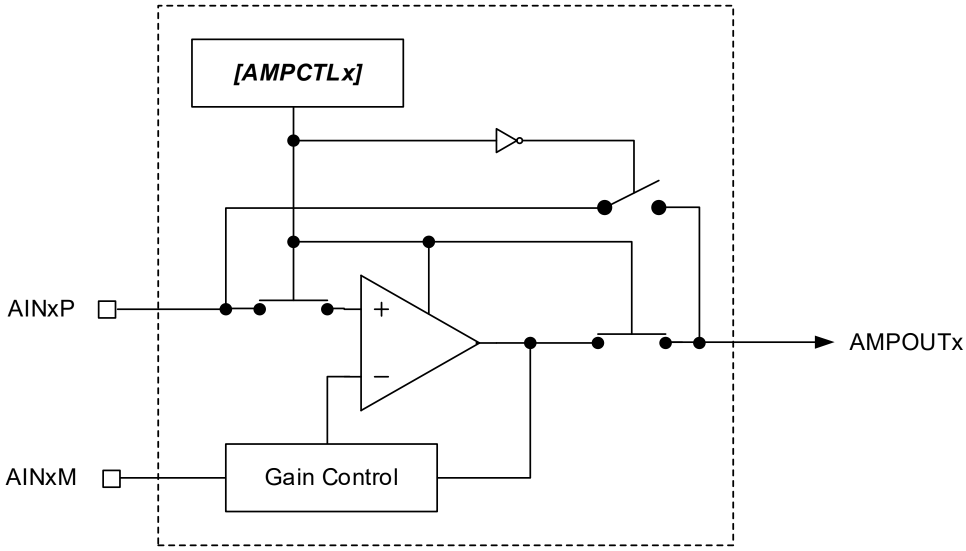

Figure 2.1 Configuration diagram of OPAMP module

Table 2.1 List of Signals

No.	Signal Name		I/O	Related Reference Manual
1	AINxP	Analog Input x pin (OPAMP x Differential input (+))	Input	Input/Output Ports 12-bit Analog to Digital Converter Product Information
2	AINxM	Analog Input x pin (OPAMP x Differential input(-))	Input	Input/Output Ports 12-bit Analog to Digital Converter Product Information
3	AMPOUTx	OPAMP x output	Output	12-bit Analog to Digital Converter Product Information

Note: For the connection destination for each product, please refer to the reference manual "Product Information".

3. Operation Description

3.1. Clock supply

When OPAMP is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB])***, fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to reference manual "Clock Control and Operation Mode".

3.2. Voltage Input

OPAMP is a differential input type, making it less susceptible to wiring noise etc. Enter the voltage both ends of the shunt resistor that detects the motor current.

3.3. OPAMP function control

By setting the OPAMP control register ***[AMPCTLx]***<AMPEN> = 1 (valid), the OPAMP function is enabled.

By setting the OPAMP control register ***[AMPCTLx]***<AMPEN> = 0 (invalid), the input to the amplifier non-inverting input (AINxP terminal) is bypassed and output from AMPOUTx. After reset, ***[AMPCTLx]***<AMPEN> = 0 (invalid).

If you do not use an OPAMP, such as using an external connection amplifier, the input can be out put directly to the next stage by bypassing the OPAMP.

3.4. Gain control

The OPAMP can set the gain of 12 steps. Set the gain with the OPAMP control register ***[AMPCTLx]*** <AMPGAIN[3: 0]>.

Gains are 2, 2.5, 3, 3.5, 4, 4.5, 6, 7, 8, 10, 12 and 15.

3.5. Voltage Output

When using the OPAMP, the voltage amplified with the set gain is output.

The output of the OPAMP is output to the ADC.

When bypassing the OPAMP, the analog input is directly connected to the ADC.

3.6. Connection diagram of OPAMP

- Example of TMPM4M group(1),TMPM4K group(2)

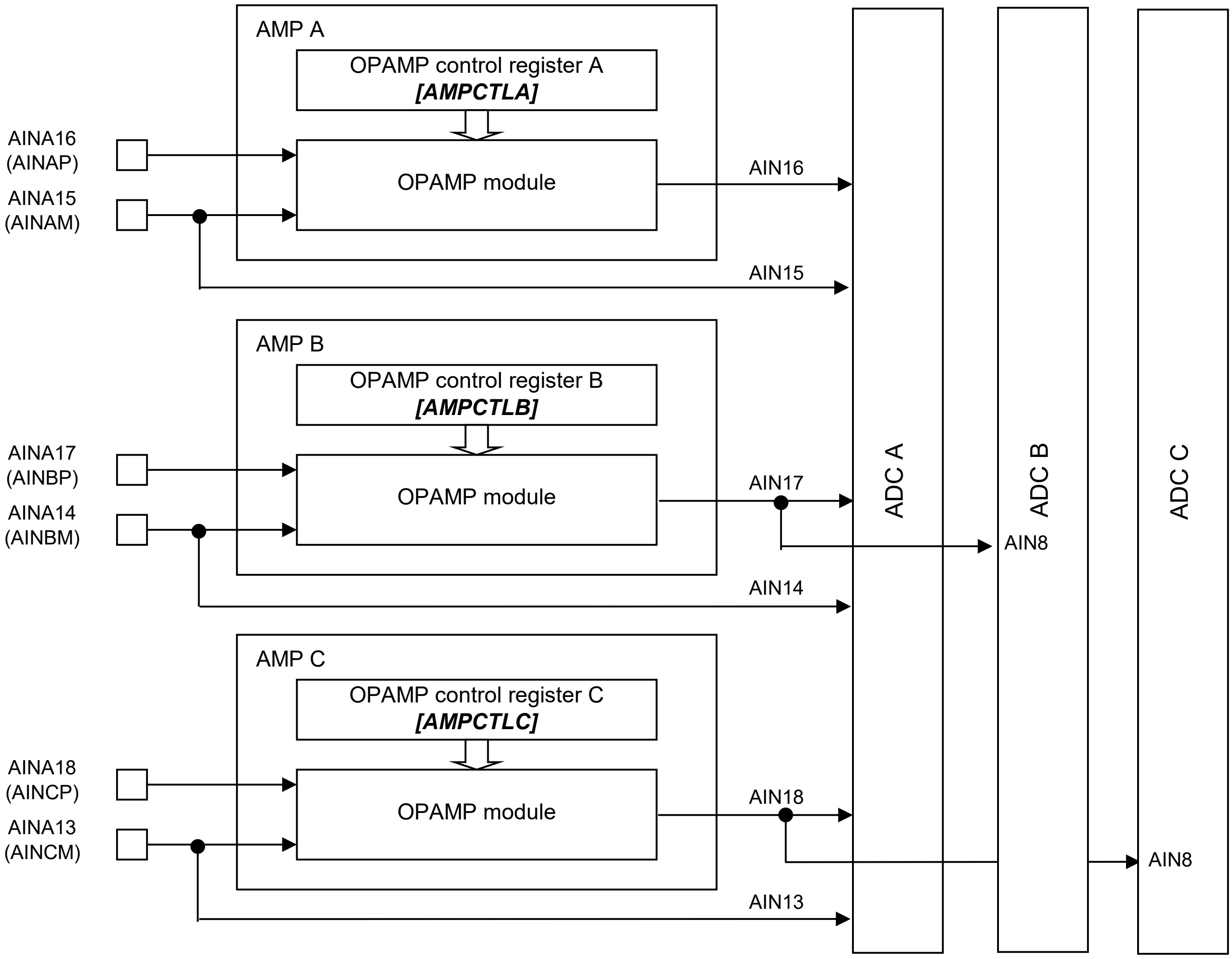

Figure 3.1 Connection diagram of OPAMP

Note: For the connection destination for each product, please refer to the reference manual "Product Information".

4. Registers

4.1. Register List

The following table lists the control registers and their addresses:

Peripheral function		Channel/Unit	Base address		
			TYPE1	TYPE2	TYPE3
Operational Amplifier	OPAMP	-	0x400BC000	0x400BD000	0x4005D000

Note: The base address type and channel/unit number vary according to a product. Please refer to reference manual "Product Information" for the details.

Register Name		Address(Base+)
OPAMP Control Register A	***[AMPCTLA]***	0x0000
OPAMP Control Register B	***[AMPCTLB]***	0x0004
OPAMP Control Register C	***[AMPCTLC]***	0x0008

4.2. Detail of Registers

4.2.1. *[AMPCTLA]* (OPAMP Control Register A)

An example of ***[AMPCTLA]***. ***[AMPCTLB]*** and ***[AMPCTLC]*** have the same configuration.

Bit	Bit Symbol	After reset	Type	Function
31:5	-	0	R	Read as "0".
4:1	AMPGAIN[3:0]	0000	R/W	Gain setting(Note3) 0000: 2.0x 0101:4.5x 1010:12.0x 0001: 2.5x 0110:6.0x 1011:15.0x 0010: 3.0x 0111:7.0x 0011: 3.5x 1000:8.0x 0100: 4.0x 1001:10.0x Please do not set other than above.
0	AMPEN	0	R/W	Enables/disables the Amp function 1: Enabled 0: Disabled (Note1)(Note2)

Note1: To change the gain setting, please do with <AMPEN>=0.

Note2: When the amplifier is enabled, it takes about 10 μs until the circuit stabilizes.

Note3: Refer to "5.1. Example of use during motor control (shunt resistor voltage measurement operation)" for motor control examples.

5. Usage

5.1. Example of use during motor control (shunt resistor voltage measurement operation)

When the OPAMP is used for motor control use, it is used to amplify the voltage between the both ends of the shunt resistor that detects the motor current.

In this case, assuming the following circuit, if the shunt voltage V1 is taken as a reference, the voltage amplified with the magnification set by the following calculation formula is output from the OPAMP output AMPOUT.

(Formula)

AMPOUT=R2/R1×(V1 - V0) + Vref

** Condition(1) R2/R1 = R2'/R1'

Condition(2) Vref(Reference Power voltage)=AVDD/2

Condition(3) AINxM input is 0V(Equivalent to analog GND)

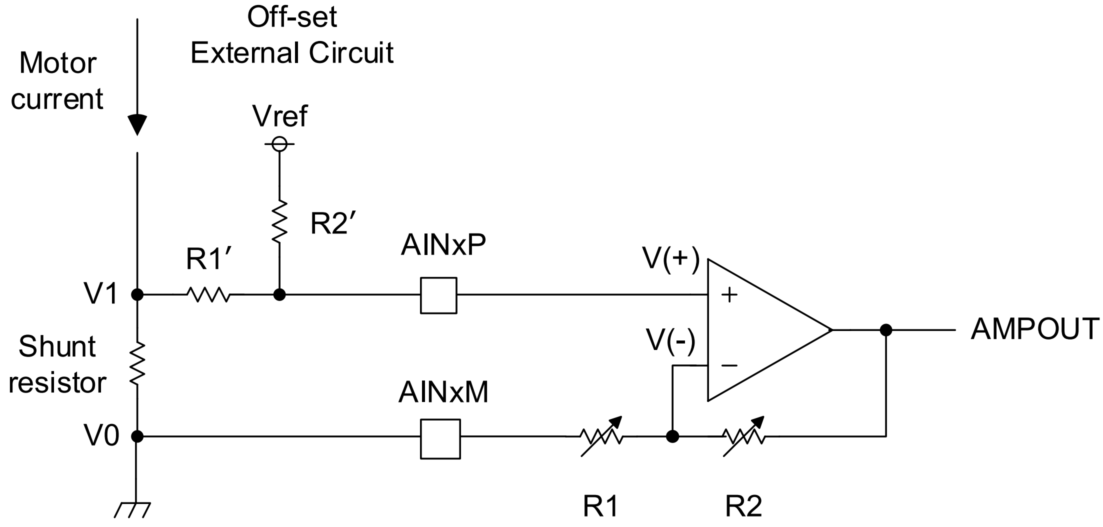

Figure 5.1 Assumed circuit at motor control operation

Table 5.1 Relationship between gain setting and amplifier output during motor control operation

Gain setting	AMP output from AMPOUT	R1(Ω)	R2(Ω)
2×	1×	7500	7500
2.5×	1.5×	6000	9000
3×	2×	5000	10000
3.5×	2.5×	4286	10714
4×	3×	3750	11250
4.5×	3.5×	3333	11667
6×	5×	2500	12500
7×	6×	2143	12857
8×	7×	1875	13125
10×	9×	1500	13500
12×	11×	1250	13750
15×	14×	1000	14000

Note: Internal resistor R1 , R2 are Typical value.

5.2. Usage examples for single amplifier operation

When using the OPAMP by itself, input it directly to the OPAMP V (+).With reference to the input V (+) of the OPAMP, the voltage amplified with the magnification set by the following calculation expression is output from the OPAMP output AMPOUT.

(Formula)

AMPOUT = (1 + R2/R1) × AINxP

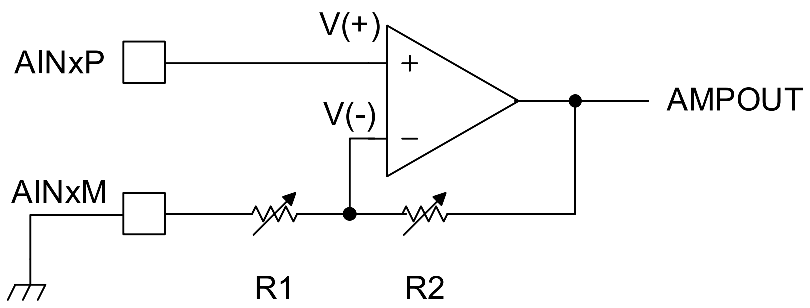

Figure 5.2 Gain setting circuit for single amplifier operation

Table 5.2 Relationship between gain setting and amplifier output when single amplifier operation

Gain setting	Amp output from AMPOUT	R1(Ω)	R2(Ω)
2×	2×	7500	7500
2.5×	2.5×	6000	9000
3×	3×	5000	10000
3.5×	3.5×	4286	10714
4×	4×	3750	11250
4.5×	4.5×	3333	11667
6×	6×	2500	12500
7×	7×	2143	12857
8×	8×	1875	13125
10×	10×	1500	13500
12×	12×	1250	13750
15×	15×	1000	14000

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2020-10-16	First release

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