32-bit RISC microcontroller

TXZ+ Family

Reference Manual
Voltage Detection Circuit
(LVD-D)

Revision 1.0

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

Preface 4
Related document 4
Conventions 5
Terms and Abbreviations 7
1. Outline 8
2. Configuration 8
3. Details of a function and operation 9
3.1. Setting 9
3.2. Change of a setup 9
3.3. Detection/release timing 10
4. Register explanation 12
4.1. Register list 12
4.2. Details of a register 12
4.2.1. *[LVDCR]* (LVD control register) 12
5. Revision history 13
RESTRICTIONS ON PRODUCT USE 14

List of figures

Figure 2.1 The Block Diagrams of LVD 8
Figure 3.1 LVD release timing..... 10
Figure 3.2 LVD detection, Release timing 11
Figure 3.3 LVD detection Minimum pulse width 11

List of Tables

Table2.1 List of Signals..... 8
Table5.1 Revision history..... 13

Preface

Related document

Document name
Product Information
Clock Control and Operation Mode
Exception

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

INT	Interrupt
LVD	Voltage Detection Circuit
POR	Power On Reset Circuit

1. Outline

The main functions of a voltage detecting circuit (LVD) are as follows.

Function classification	Function	Functional Description	Remarks
Supply voltage detection function	Reset Output	It is reset generating below in setting detection voltage.	Either the reset output or an interrupt request output is chosen
	Interrupt request	An interrupt request is generated below in setting detection voltage.	
	Monitor	A monitor is possible as voltage detection status.	
	Detection voltage selection	The selection out of eight kinds is possible.	

2. Configuration

A voltage detection circuit consists of a reference voltage generation circuit, a detection voltage selection circuit, a Comparator, and a control register.

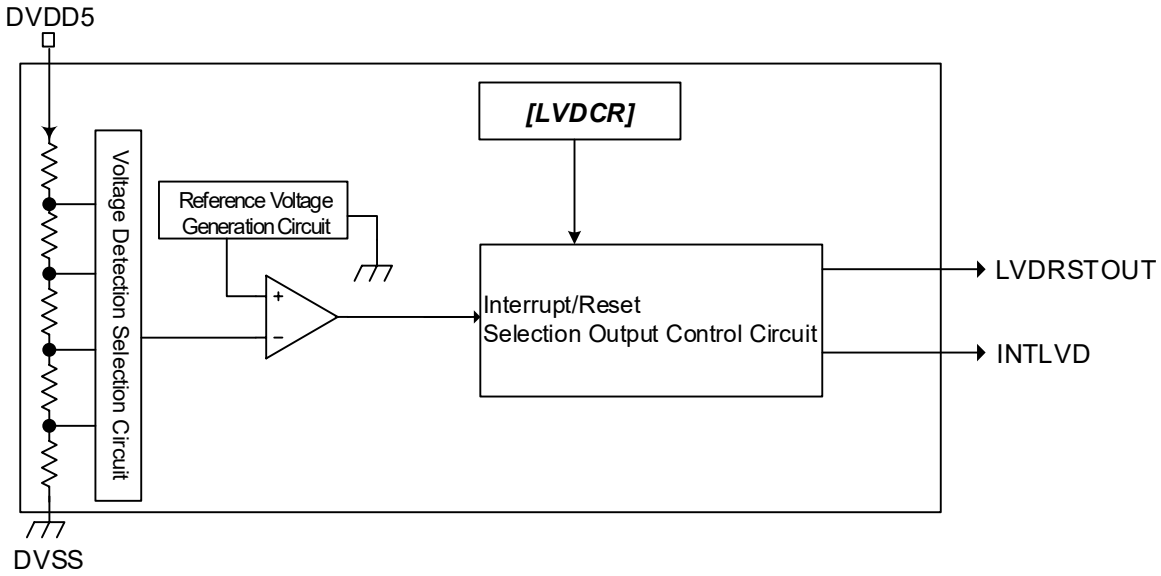

Figure 2.1 The Block Diagrams of LVD

Table2.1 List of Signals

No	Symbol	Signal name	I/O	Related Reference manual
1	DVDD5	Power supply pin for detection	Input	Product Information
2	LVDRSTOUT	LVD reset Output	Output	Clock Control and Operation Mode
3	INTLVD	LVD interrupt request signal	Output	Exception

3. Details of a function and operation

A voltage detection circuit supervises the voltage of DVDD5.

The reference voltage which occurred in the reference voltage generating circuit is compared with the output of the detection voltage made from DVDD5. Detection voltage can be chosen.

According to a comparison result, interrupt/reset selection output control circuit outputs reset or interrupt.

At the power up, while the voltage of DVDD5 is lower than release voltage, reset (LVDRSTOUT) is outputted. Reset will be released if release voltage is exceeded.

3.1. Setting

In the voltage detection circuit, the enable/disable operation is carried out by the ***[LVDCR]***<EN>, the ***[LVDCR]***<LVL> can select the detection (release) voltage, the ***[LVDCR]***<SEL> can select either LVDRSTOUT or INTLVD, and the ***[LVDCR]***<OUTEN> can set the output control .

When ***[LVDCR]***<EN> is set to “1” after setting selection of the detection (release) voltage and selection of LVDRSTOUT and interrupt, the operation is enabled and the detection (release) operation starts.

If the voltage of DVDD5 becomes lower than detection voltage, either LVDRSTOUT selected by ***[LVDCR]***<SEL> or INTLVD is outputted.

In addition, also where LVDRSTOUT/ INTLVD is forbidden by ***[LVDCR]***<OUTEN>, a voltage condition can be monitored by ***[LVDCR]***<ST>.

3.2. Change of a setup

When changing of detection (release) voltage, and a selection change of a LVDRSTOUT/ INTLVD interrupt Output, change a setup after setting ***[LVDCR]*** <OUTEN> to "0" and forbidding an Output.

The selection of the detection disable / enable by LVD motion control (***[LVDCR]*** <EN>) should be set under the power control (***[LVDCR]*** <OUTEN>) is set to “0”.

Moreover, when ***[LVDCR]***<EN>is set to "1", set ***[LVDCR]*** <OUTEN> to "1" after waiting 1 ms or more.

Change the detection (release) voltage (***[LVDCR]*** <LVL [2:0]>) after the output control (***[LVDCR]*** <OUTEN>) is set to "0". And waiting 100 μs or more after changing ***[LVDCR]***<LVL [2:0]>, set ***[LVDCR]***<OUTEN> to "1".

3.3. Detection/release timing

Detection of the voltage detection circuit and releasing operation are shown in the following figure.

1) Power On

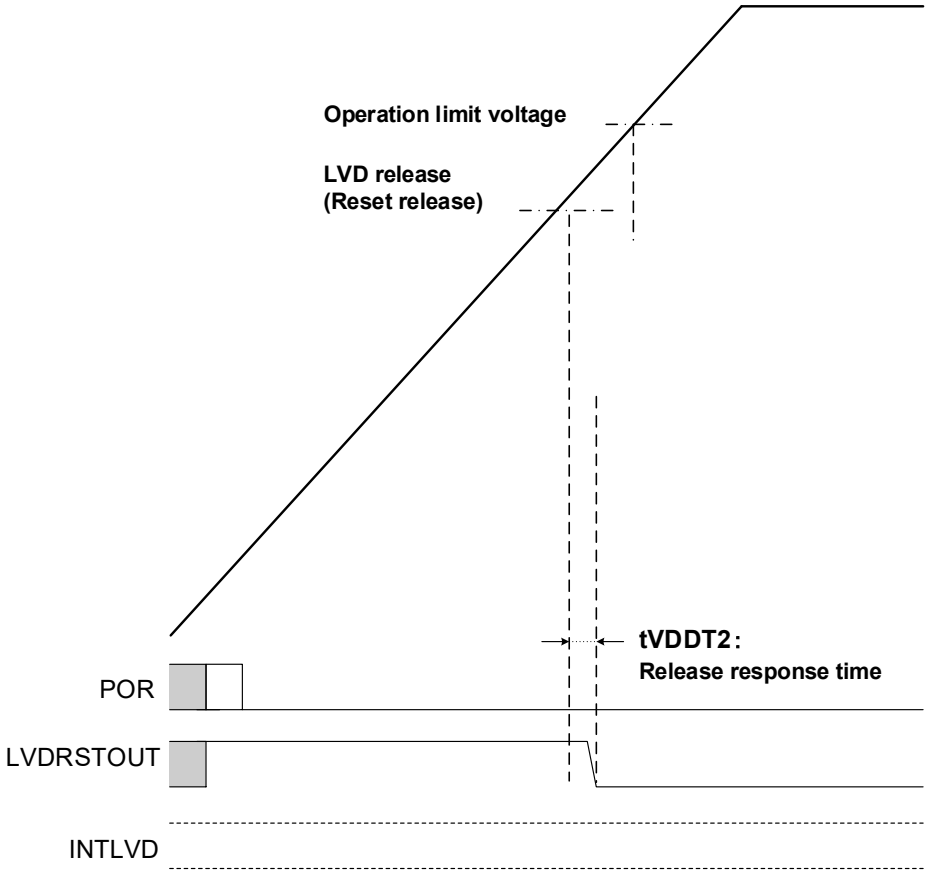

Figure 3.1 LVD release timing

2) LVD detection, Release timing

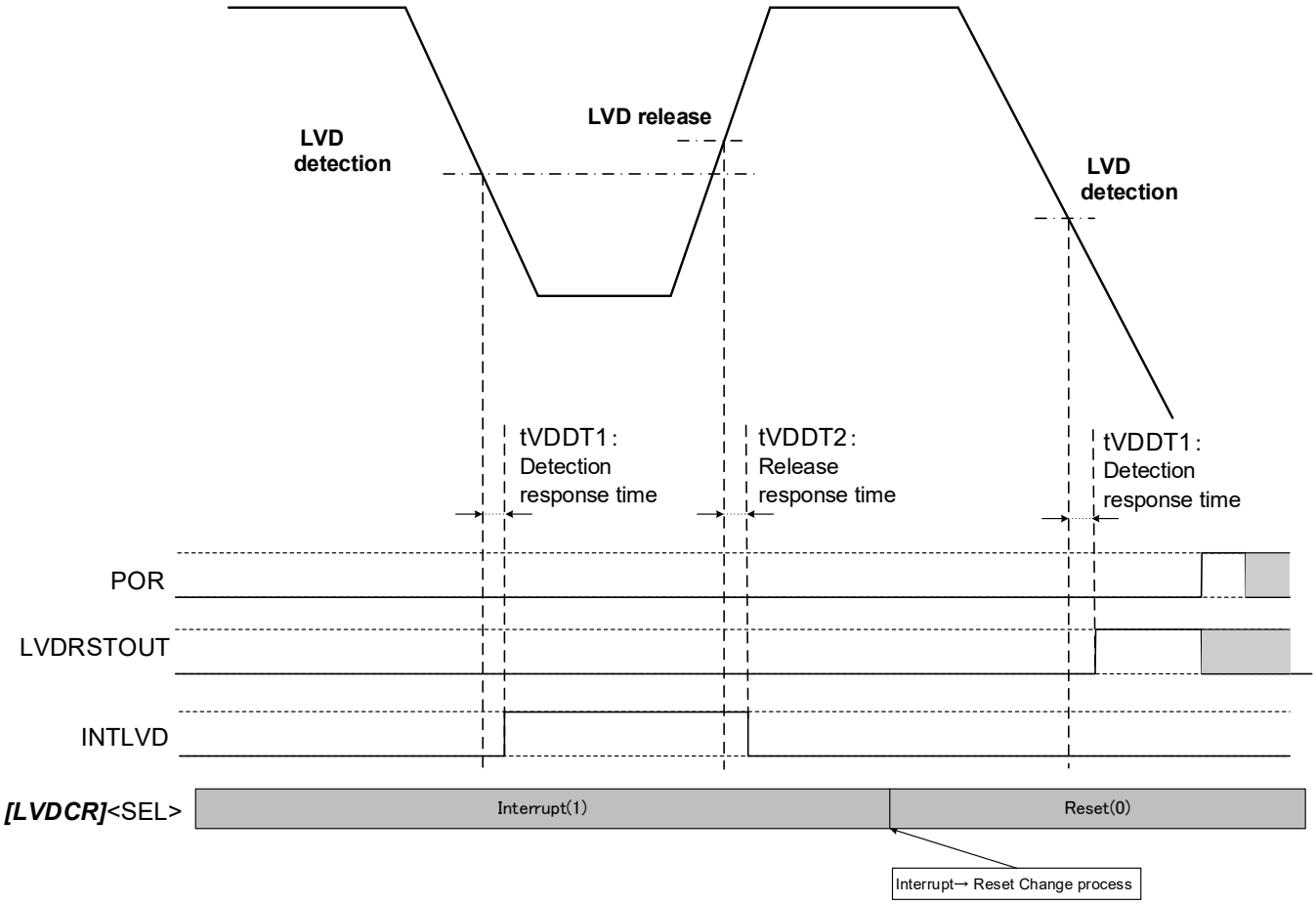

Figure 3.2 LVD detection, Release timing

3) LVD detection Minimum pulse width

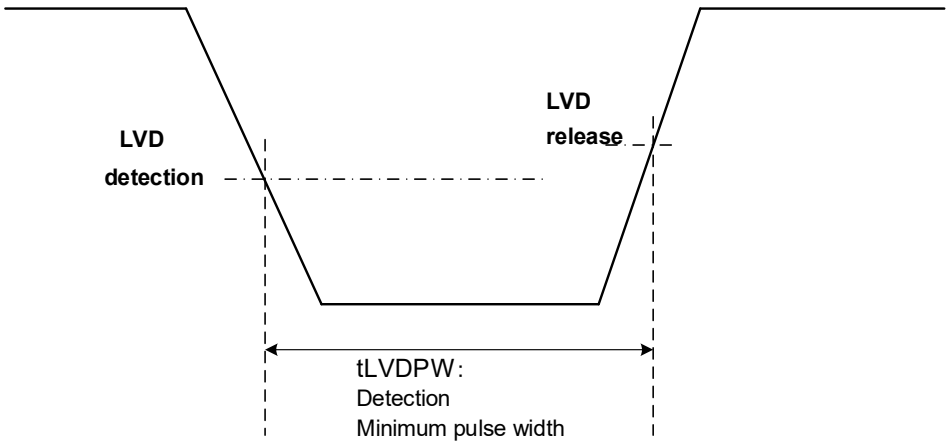

Figure 3.3 LVD detection Minimum pulse width

4. Register explanation

4.1. Register list

The register and address of LVD are shown below.

Peripheral function		Channel/Unit	Base address
			TYPE1
Voltage detection circuit	**LVD**	-	0x4003EC00

Register name		Address (Base+)
LVD control register	***[LVDCR]***	0x0000

Note: The ***[LVDCR]*** cannot be bit band accessed. Only byte access is possible.

4.2. Details of a register

4.2.1. *[LVDCR]* (LVD control register)

Bit	Bit Symbol	After reset	Type	Function	
7	ST	0	R	Voltage detection status (notes) 0: A supply voltage is more than detection voltage. 1: A supply voltage is below detection voltage.	
6:4	LVL[2:0]	000	R/W	Detection voltage 000: 2.65V 001: 2.7V 010: 2.8V 011: 2.9V 100: 4.0V 101: 4.2V 110: 4.4V 111: 4.6V	Release voltage 000: 2.7V 001: 2.75V 010: 2.85V 011: 2.95V 100: 4.05V 101: 4.25V 110: 4.45V 111: 4.65V
3	-	0	R	Read as "0".	
2	SEL	0	R/W	Selection of RESET or INTLVD interrupt 0:RESET(LVDRSTOUT) 1: Interruption (INTLVD)	
1	OUTEN	1	R/W	Output control of RESET/ INTLVD interrupt 0: Output disable 1: Output enable	
0	EN	1	R/W	LVD operation control 0: Disable Detection 1: Enable Detection	

Note: When reading ***[LVDCR]***<ST>, read out of multiple times is performed. Check the read value becomes the same.

5. Revision history

Table5.1 Revision history

Revision	Date	Description
1.0	2020-10-02	First Release

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