Tips for Selecting Level Shifters (Voltage Translation ICs)

Outline:

This application note discusses how to select the right level shifter (also known as voltage translation IC). An electronic circuit board that consists of multiple voltage domains requires up, down, or up/down translation.

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1. Introduction: Why are level shifters necessary?

Nowadays, electronic systems are becoming ever faster and more versatile while becoming progressively smaller and less power-consuming. This trend is driving the need for semiconductor devices with the same characteristics. To meet these requirements, semiconductor fabs have been shrinking manufacturing processes, especially for LSI chips at the heart of electronic systems. Accompanying process shrinking, migration to low-voltage devices is progressing partly because of the low withstand voltage of small-geometry processes (due to the effects of internal electric fields) and partly because of the market demand for reducing power consumption. In contrast, peripheral ICs still operate at either 5 V or 3.3 V to maintain compatibility with the interface standards for external systems.

Therefore, core and peripheral ICs might operate at different voltages. In some cases, the output signals of a driver IC might not be compatible with the input voltage specification of a receiver IC.

Conversely, some system manufacturers use legacy ICs at the core of a system and state-of-the-art low-voltage ICs at the periphery in order to reduce overall system cost. In this case as well, core and peripheral ICs operate at different voltages. Therefore, electronic boards generally consist of multiple voltage domains. To interface between two voltage domains, it is necessary to shift the output voltage level from a driver to a level compatible with the input specification of the receiver. The device that plays this role is a level shifter (also called a voltage translator or a voltage translation IC by some manufacturers). Considerable skill is required to select level shifters that meet system specifications such as voltage translation levels, propagation delay times, and packaging requirements.

This application note explains how to select appropriate level shifters according to the required specifications.

When two ICs with different supply voltages are connected, the driver IC might not satisfy the input voltage specification of the receiver IC.

→ A level shifter is used to solve this problem.

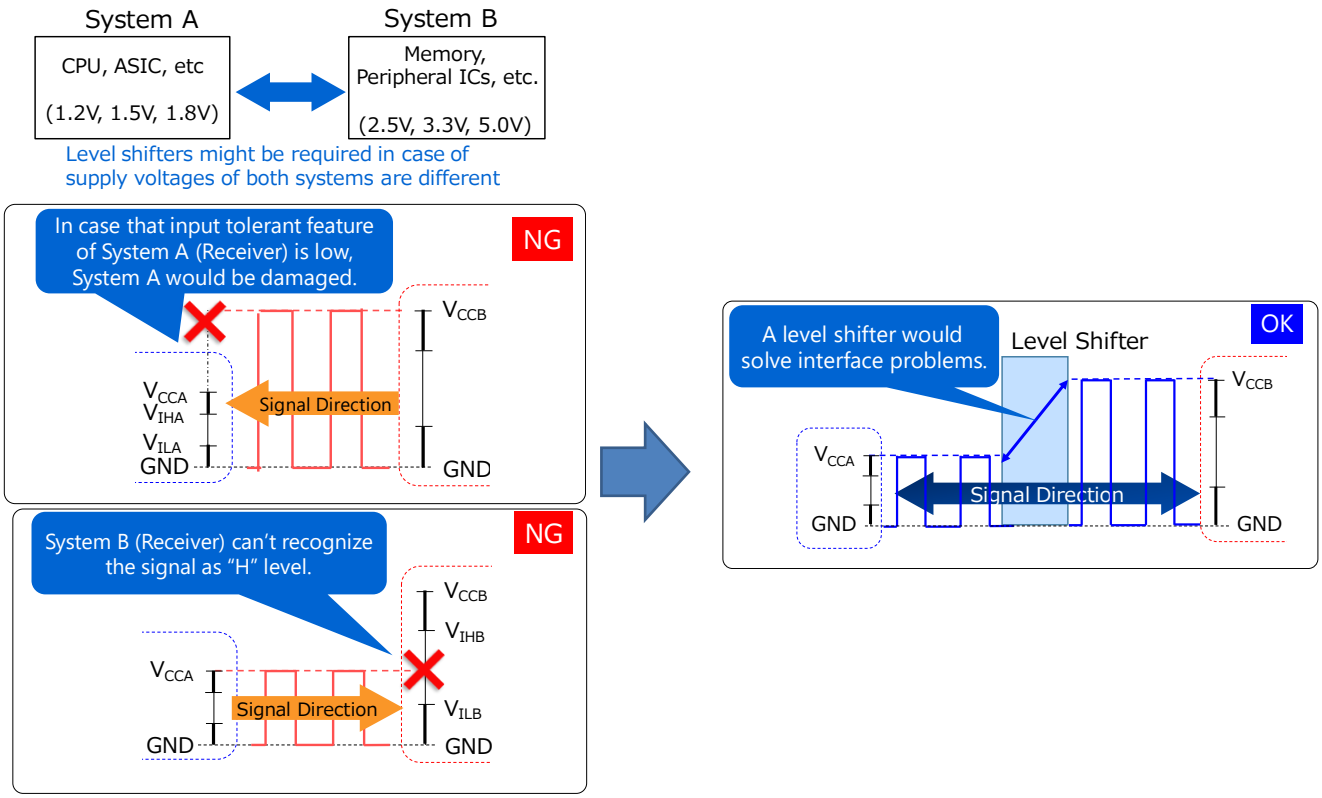


Figure 1 Why are level shifters necessary?

2. Types of level shifters

Level shifters (voltage translation ICs) are broadly divided into the following two types:

(1) Dedicated level shifter ICs

- Level shifter (buffer-type)

  Examples:

  Single-supply/unidirectional: 74LV4T125FT, 74LV4T126FT, 7UL1T34FU

  Dual-supply/bidirectional: TC7MP3125FT, TC7MPN3125FT

- Dual-supply level shift bus switches

  Examples:

  Dual-supply/bidirectional: TC7MPB9307FT, TC7QPB9306FT, TC7WPB9306FK, TC7SPB9306TU

(2) CMOS and one-gate logic (L-MOS*) ICs with one of the following level-shifting functions:

*: One-gate logic ICs are hereinafter simply referred to as L-MOS ICs.

- TTL-level input
- Input-tolerant function
- Open-drain output

Each of them is detailed in the following sections.

2.1 TTL-level input

Transistor-transistor logic (TTL) is built from bipolar transistors that operate at 5 V. Although CMOS logic ICs are the most commonly used at present, TTL logic such as the 74LS and 74ALS series remains in use. There is an industry standard for the TTL input level to ensure that signals can be properly passed from one device to another in a logic system operating from a 5-V power supply. The TC74HCT, TC74ACT and TC74VHCT series ending with the letter “T” have a 5-V TTL-level input.

Variations of the basic TTL series include low-voltage TTL (LVTTL) compatible with 3-V power supplies composed of CMOS devices. LVTTL, which is standardized by JEITA ED-5001A, has the same threshold voltage as TTL. The 74LCX and 74VCX series satisfy the LVTTL requirements.

Generally, the input threshold of typical CMOS logic is designed to be 1/2 x VCC, and the standard on the data sheet is VIH (0.7 x VCC) / VIL (0.3 x VCC). Therefore, in the case of 5-V CMOS logic, it is V_{IH} (3.5 V) / V_{IL} (1.5 V). The output voltage of 5-V TTL logic is standardized at V_{OH} (2.4 V) / V_{OL} (0.4 V). When an output of a 5-V TTL logic IC is connected to an input of a 5-V CMOS logic IC, the CMOS logic IC does not recognize the V_{OH} level (2.4 V) of the 5-V TTL logic IC as logic High (because $V_{OH} < V_{IH}$).

In contrast, when V_{CC} = 5 V, a CMOS logic IC with TTL-level inputs has a minimum V_{IH} of 2.0 V and a maximum V_{IL} of 0.8 V, which are lower than the input thresholds of typical CMOS logic ICs.

Therefore, a CMOS logic IC can recognize the V_{OH} level of a 5-V TTL logic IC as logic High because $V_{OH} > V_{IH}$ (see Figure 2).

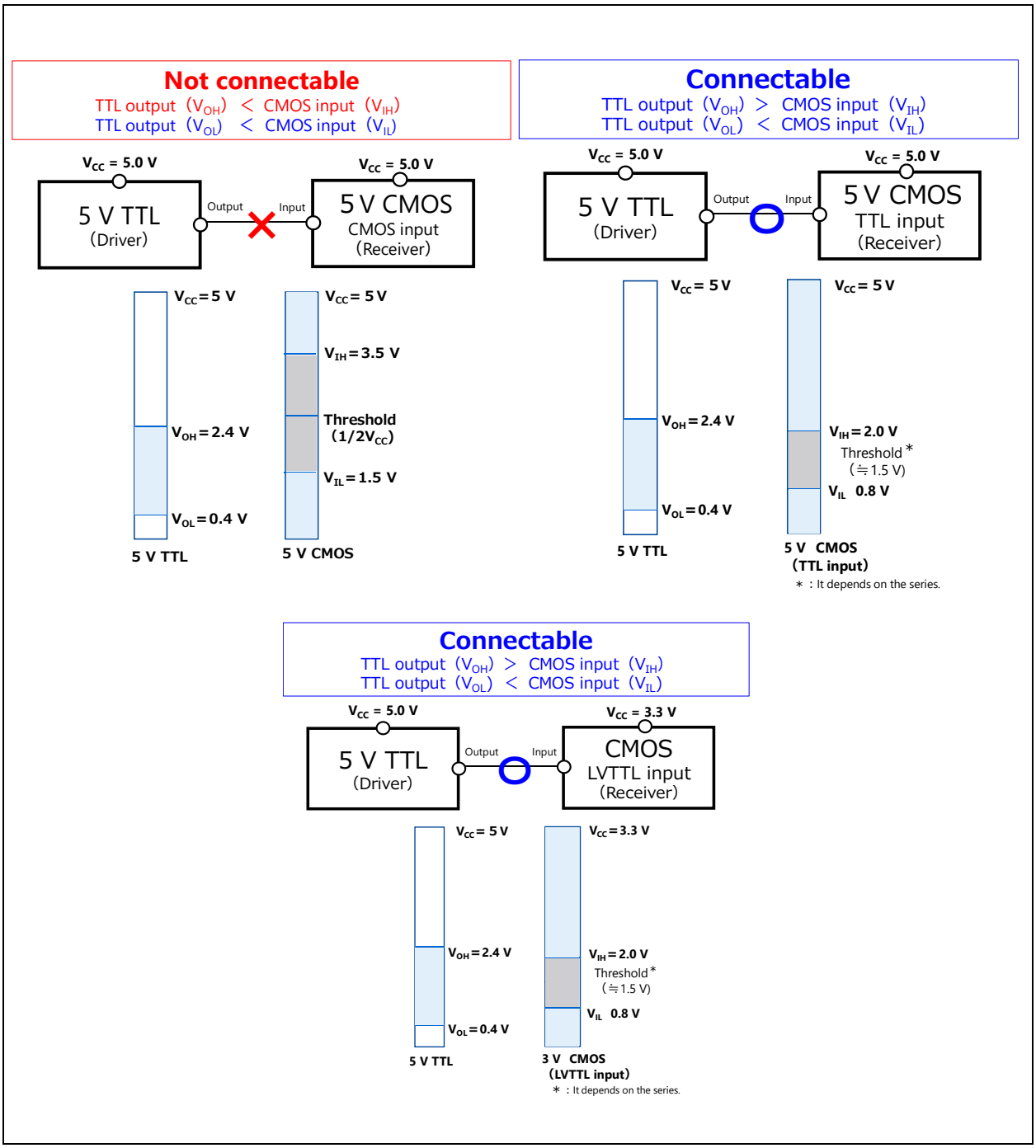


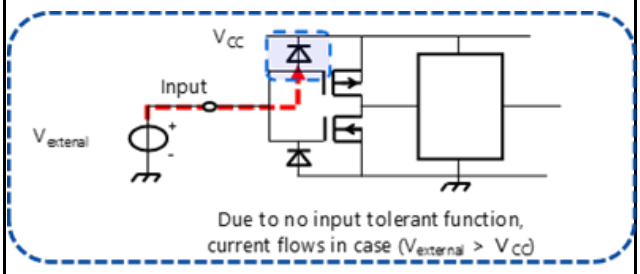
Figure 2 TTL-level inputs (5-V TTL and 3.3-V LVTTL)

2.2 Input-tolerant function

The word “tolerant” means “able to endure.” The input-tolerant function prevents current from flowing from an input to the power supply when the input voltage is higher than the supply voltage (V_{CC}). For example, current does not flow to the power supply even if an input signal is applied when V_{CC}= 0 V. This is realized by an input protection circuit without a diode returned to V_{CC}. Check the datasheet for the input voltage range to determine whether a logic IC has an input-tolerant function. ICs with this function have a maximum input voltage equal to V_{CC} maximum (5.5 V in the case of the 74VHC series) regardless of the V_{CC} level. In contrast, the input voltage range of ICs without an input-tolerant function is specified as 0 V to V_{CC}.

Equivalent input circuit and operating range

(TC74HC series without an input-tolerant function)



TC74HC Series Operating Ranges (ex. TC74HC244)

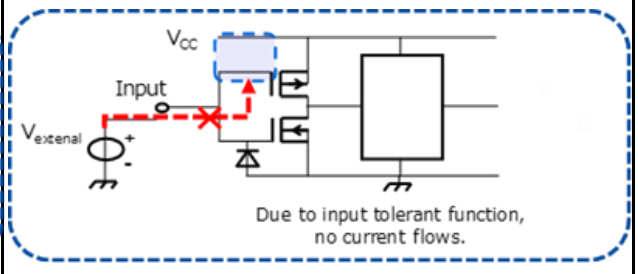
Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Equivalent input circuit and operating range

(74VHC series with an input-tolerant function)



74VHC Operating Ranges (ex.74VHC244)

Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		−40 to 125	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V	0 to 100	ns/V
		V_{CC} = 5 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Figure 3 Equivalent input circuits and operating ranges of ICs with and without an input-tolerant function

2.3 Open-drain ICs (unidirectional up and down translation)

Level-shifting from the output voltage of an IC to an arbitrary supply voltage level can be accomplished by connecting one end of a pull-up resistor to the output of an open-drain IC and the other end of the pull-up resistor to the power supply.

However, in order to pull up the output of an IC to a supply voltage higher than its own supply voltage (when $V_{CCA} < V_{CCB}$), it is necessary to use an IC with an output-tolerant function so that current does not flow from V_{CCB} to V_{CCA}.

The output-tolerant function is also called power-down protection. Without power-down protection, current flows from V_{CCB} to V_{CCA} as shown in Figure 4 when $V_{CCB} > V_{CCA}$. The output with power-down protection allows a voltage of up to the maximum V_{OUT} level (5.5 V in the case of the 74VHCT series) to be applied. A NAND gate (03), an inverter (05), and a buffer (07) are available with an open-drain output.

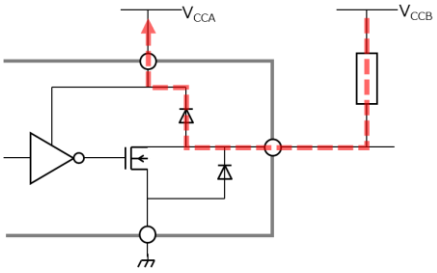
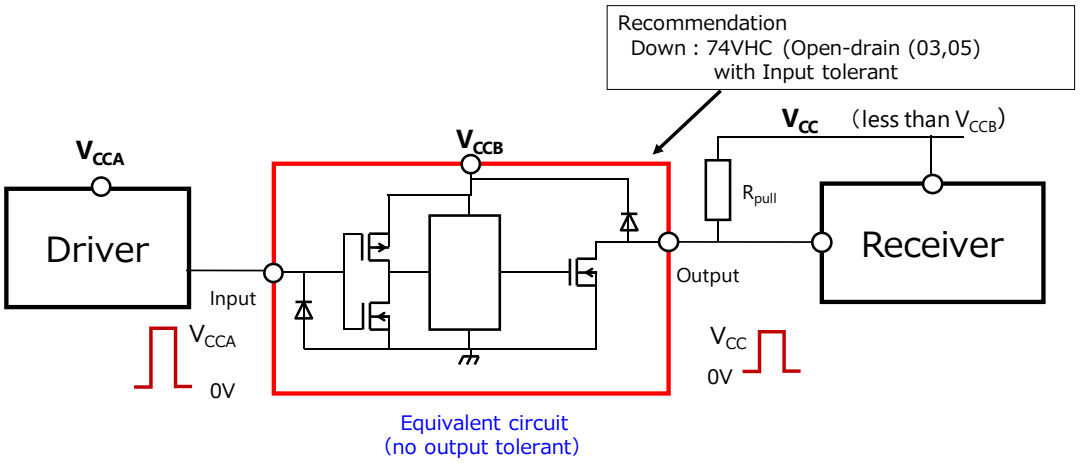


Figure 4 IC without an output-tolerant function (power-down protection)

In addition, an appropriate pull-up resistor should be selected since steady-state current flows through the pull-up resistor during output is low state. The IC draws more current when it drives a logic Low than when it drives a logic High. Since the output rise time is affected by the pull-up resistor, it might differ from the output fall time.

ICs without an output-tolerant function allow only down translation to V_{CCB}.



ICs with an output-tolerant function allow both up and down translation to the maximum V_{OUT} level regardless of V_{CCB}.

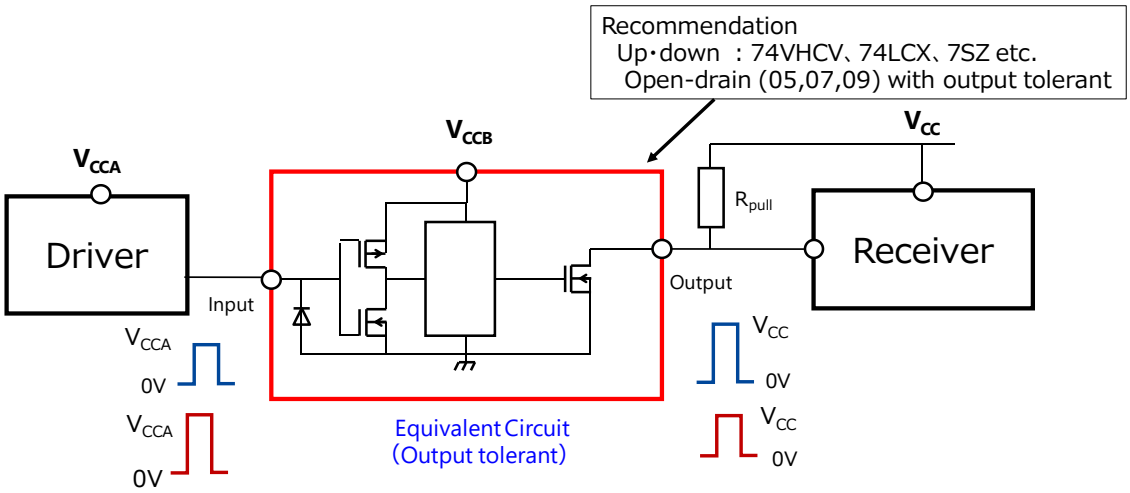


Figure 5 Examples of up and down translation using ICs with an open-drain output

3. How to select level shifters

Generally, you can follow these six steps to select a level shifter that satisfies system requirements.

At Steps 1 to 3, you narrow down your choice to one or a few product series. At Steps 4 to 6, you select a specific level shifter.

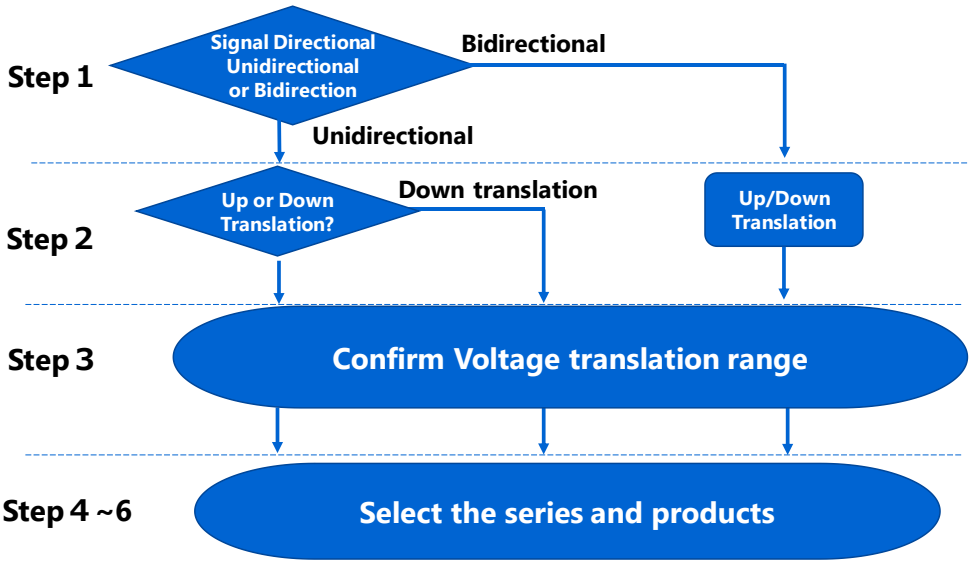


Figure 6 Steps for selecting a level shifter

Step 1. Determine the signal direction (unidirectional or bidirectional).

Step 2. In the case of a unidirectional signal, select either up translation or down translation. In the case of a bidirectional signal, up/down translation is generally selected.

Step 3. Determine the voltage translation levels required from a driver's output to a receiver's input. Then, check the level-shifting range of each product series and select one that meets the requirements specification. Some ICs operate from a single power supply while others operate from dual power supplies. Single-supply CMOS logic and L-MOS ICs provide a level-shifting function (TTL-level input, input-tolerant function, or open-drain output). To select the right IC, check the supply voltage range and the input V_{IH} specification. In contrast, dedicated level shifters provide dual power supplies. Level-shifting can be easily accomplished by setting one of the power supplies to a driver's output level and the other to a receiver's input level.

Step 4. Check the number of level-shifting circuits required.

Step 5. Check the required propagation delay times (t_{PLH} and t_{PHL} *or* t_{PLZ} and t_{PZL}) of the IC. Also check the output drive capability (I_{OH} and I_{OL}) of the IC. You have two choices particularly for bidirectional up/down translation: dual-supply level shifters (buffer-type) and level shift bus switches. Level shifters (buffer-type) provide an output drive capability whereas level shift bus switches, which are designed to connect/disconnect a signal path or demultiplex a signal, do not have an output drive capability.

Step 6. Check the required package.

4. Examples of selecting Toshiba's level shifters

Toshiba offers various level shifters to meet diverse customer requirements.
This section presents examples of how to select Toshiba's level shifters according to the flow shown in the previous section. The following subsections detail the selection process for the eight cases shown in Table 2.

Table 1 Eight scenarios for selecting Toshiba's level shifters

	Step1	Step2	Step3	
	Signal Direction	Translation Up / Down	Voltage translation range	Number of power supply
Case 1	Uni-Directional	Up	2 V(TTL) → 5±0.5 V	Single
Case 2			Arbitrary range from VIH minimum to VOUT maximum (Open-drain) Ex) 1.65 V → 5.5 V, 0.9 V → 3.6 V	
Case 3			Input TTL/LVTTL level → V_{CC}(opr.) Ex) 2 V → 5±0.5 V, 1.2 V → 2.5±0.2 V	
Case 4			0.72 V → 3.6 V Up translation from a voltage lower than is possible with an L-MOS IC (7UL1T or 7UL2T of the LVP series)	Dual
Case 5		Down	Maximum voltage tolerated by the input to V_{CC}(opr.) Ex) 5 V → 2 V, 3.6 V → 0.9 V	Single
Case 6			Arbitrary range from a voltage range tolerated by the input (3.6 to 5.5 V) to V_{CC}(opr.) (Open-drain) Ex) 5.5 V → 1.65 V, 3.6 V → 0.9 V	
Case 7	Bi-Directional	Up/Down	V_{CCA} ⇔ V_{CCB} (Level shifter (Buffer-type)) Ex) A (0.72 V) → B (3.6 V), B (3.6 V) → A (1.1 V)	Dual
Case 8			V_{CCA} ⇔ V_{CCB} (Level shift bus switch) Ex) A (1.4 V) → B (5.5 V), B (5.5 V) → A (1.65 V)	

4.1 Case 1: Example of up translation using an IC with a TTL-level input (unidirectional/single power supply)

Using a logic IC with a single power supply and TTL-level input thresholds (V_{IH} = 2.0 V and V_{IL} = 0.8 V)

The power supply (V_{CC}) range is 4.5 to 5.5 V.

Not only buffers and bus transceivers but also gates and flip-flops are available with a TTL-level input(s).

Step 1. Unidirectional
Step 2. Up translation
Step 3. Level-shifting range: 2 V (TTL) to 5±0.5 V
Step 4. Select either a CMOS logic or L-MOS IC according to the number of level-shifting circuits required.
Step 5. Select an IC with the required propagation delay times from a product list.
When high-speed operation is necessary, select the 74AC (74ACT) or 74VHC (74VHCT) series.
Step 6. Select the optimum package according to the available board space.

Table 2 Case 1 (up translation, unidirectional, single power supply): 2 V (TTL) to 5±0.5 V

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range(V)	t_{PLH}/t_{PHL} (ns) #1	$\|I_{OH}\|/I_{OL}$ (mA)
CMOS Logic IC	74HC	TC74HCTxxx	1~8	DIP/SOP/TSSOP	4.5~5.5	2	5.5	2→5.5	28	6 @V_{CC}=4.5 V
		74HCTxxx		SOIC/TSSOP	4.5~5.5	2	5.5	2→5.5		
	74AC	TC74ACTxxx	4,6,8	DIP/SOP/TSSOP	4.5~5.5	2	5.5	2→5.5	9	24 @V_{CC}=4.5 V
	74VHC	TC74VHCTxxx	1~8	DIP/SOP/TSSOP/US	4.5~5.5	2	5.5	2→5.5	9.5	8 @V_{CC}=4.5 V
		74VHCTxxx	1~8	TSSOP	4.5~5.5	2	5.5	2→5.5		
Product Category		**Product Name**	**Number of circuits**	**Package**	**V_{CC}(opr.)(V)**	**V_{IH}(min)(V)**	**V_{OUT}(max)(V)**	**Voltage translation range(V)**	**t_{PLH}/t_{PHL} (ns) #1**	**$\|I_{OH}\|/I_{OL}$ (mA)**
One-gate Logic (L-MOS)	TTL-level input	TC7WTxxx	2	SM8	4.5~5.5	2	5.5	2→5.5	28	6 @V_{CC}=4.5 V
		TC7SETxxx	1	SMV/USV	4.5~5.5	2	5.5	2→5.5	11.9	8 @V_{CC}=4.5 V

#1 Maximum delay times at V_{CC}(opr.) max, T_a = 85°C, and C_L = 50 pF. Functions: CMOS logic IC (244) / L-MOS IC (125)

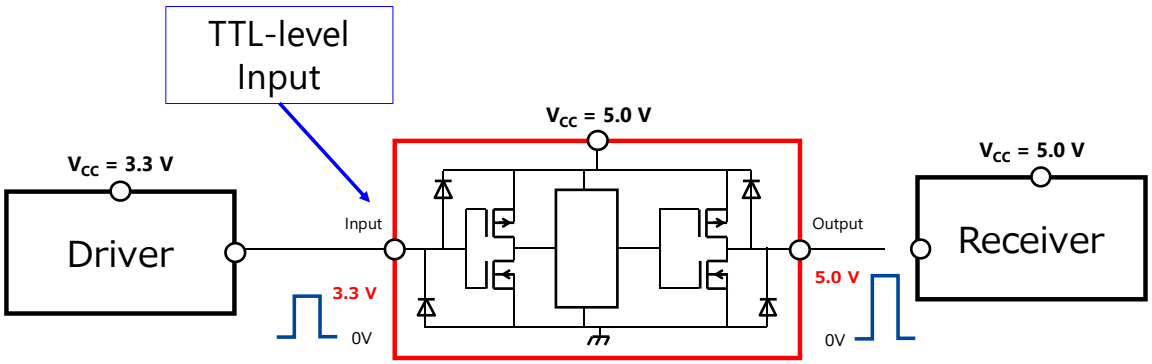


Figure 7 Example of up translation using an IC with a TTL-level input

4.2 Case 2: Example of up translation using an IC with an open-drain output (unidirectional, single power supply)

Using an open-drain output with an output-tolerant function (power-down protection)

Step 1. Unidirectional
Step 2. Up translation
Step 3. Level-shifting range: Arbitrary range from V_{IH} minimum to V_{OUT} maximum
Examples: 1.65 V to 5.5 V, 0.9 V to 3.6 V
Step 4. Select a CMOS logic or L-MOS IC according to the number of level-shifting circuits required.
Step 5. Select an IC with the required propagation delay times from a product list.
Step 6. Select the optimum package according to the available board space.

If level-shifting from an ultralow voltage (0.9 V) is necessary, select the L-MOS LVP series (7UL).

Table 3 Case 2 (unidirectional, up translation, single power supply): Arbitrary range from V_{IH} minimum to V_{OUT} maximum

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLZ}/t_{PZL} (ns) #2	$\|I_{OH}\|/I_{OL}$ (mA)
CMOS Logic IC	74VHC	74VHCV05/07	6	TSSOP	1.8~5.5	1.65	5.5	1.65→5.5	8.5	16 @V_{CC}=4.5 V
		TC74VHCV05/07		US	1.8~5.5	1.65	5.5	1.65→5.5		
	74LCX	74LCX05/07		TSSOP	1.65~5.5	1.65*0.9	5.5	1.5→5.5	4	24 @V_{CC}=3.0 V
		TC74LCX05/07		US	1.65~5.5	1.65*0.9	5.5	1.5→5.5		
Product Category		**Product Name**	**Number of circuits**	**Package**	**V_{CC}(opr.)(V)**	**V_{IH}(min)(V)**	**V_{OUT}(Max)(V)**	**Voltage translation range (V)**	**t_{PLZ}/t_{PZL} (ns) #2**	**$\|I_{OH}\|/I_{OL}$ (mA)**
One-gate Logic (L-MOS)	VHS	TC7SH09	1	SMV/USV	2.0~5.5	1.5	5.5	1.5→5.5	8	8 @V_{CC}=4.5 V
	SHS	TC7SZ05/07	1	SMV/USV/ESV/fSV	1.65~5.5	1.65*0.75	5.5	1.3→5.5	4.5	24 @V_{CC}=3.0 V
		TC7PZ05/07	2	US6	1.65~5.5	1.65*0.75	5.5	1.3→5.5	3.9	
		TC7WZ05/07	3	US8	1.65~5.5	1.65*0.75	5.5	1.3→5.5	3.9	
	LVP	7UL1G07	1	USV	0.9~3.6	0.9	3.6	0.9→3.6	12.8/4.1	8 @V_{CC}=3.0 V

#2 Maximum delay times at V_{CC}(opr.) max, T_a = 85°C, and C_L = 50 pF (30 pF in the case of the 7UL1G).
Functions: CMOS logic IC (05) / L-MOS ICs (05, 07, 09)

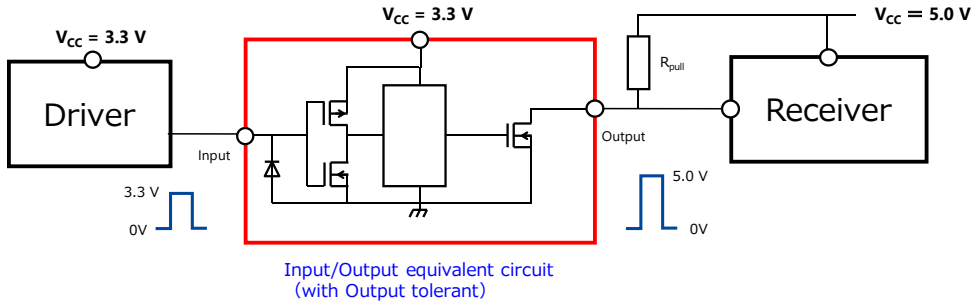


Figure 8 Example of up translation using an IC with an open-drain output (74LCX05)

4.3 Case 3: Example of up translation using an IC with an LVTTL-level input (unidirectional, single power supply)

Using an LVTTL-level input

Step 1. Unidirectional

Step 2. Up translation

Step 3. Level-shifting range: TTL/LVTTL input level to V_{CC}(opr.)
74LV4T: 2 V to 5±0.5 V, 1.2 V to 2.5±0.2 V
7UL1T/2T: 1.2 V to 2.5±0.2 V
Select a product according to the level-shifting range and the logic function required.

Step 4. Select a dedicated level shifter (74LV series) or an L-MOS IC (7UL1T or 7UL2T of the LVP series) according to the number of level-shifting circuits required.

Step 5. Select an IC with the required propagation delay times from a product list.

Step 6. Select the optimum package according to the available board space.

Table 4 Case 3 (unidirectional, up translation, single power supply): TTL/LVTTL input level to V_{CC}(opr.)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #3	$\|I_{OH}\|/I_{OL}$ (mA)
One-gate Logic (L-MOS)	LVP	7UL1Txxx	1	USV	2.3~3.6	1.1	3.6	1.1→3.6	4.7/5.0	8 @V_{CC}=3.3 V
		7UL2Txxx	2	US8	2.3~3.6	1.1	3.6	1.1→3.6	7.5/5.2	

#3 Maximum delay times at V_{CC}(opr.) max, V_{IN} =1.65 V, T_a = 85 °C, and C_L = 15 pF.

Product Category	Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #4	$\|I_{OH}\|/I_{OL}$ (mA)
Level Shifter	74LV4Txxx	4	TSSOP/US	4.5~5.5	2	5.5	2→5.5	5.6	16 @V_{CC}=4.5 V
				3.0~3.6	1.35	3.6	1.35→3.6	8.1	8 @V_{CC}=3.0 V
				2.3~2.7	1.2	2.7	1.2→2.7	12.4	3 @V_{CC}=2.3 V
				1.65~1.95	1	1.95	1→1.95	33.2	2 @V_{CC}=1.65 V

#4 Maximum delay times at V_{CC}(opr.) max, V_{IH} minimum, T_a = 85 °C, and C_L = 30 pF. Function: CMOS Logic IC (125)

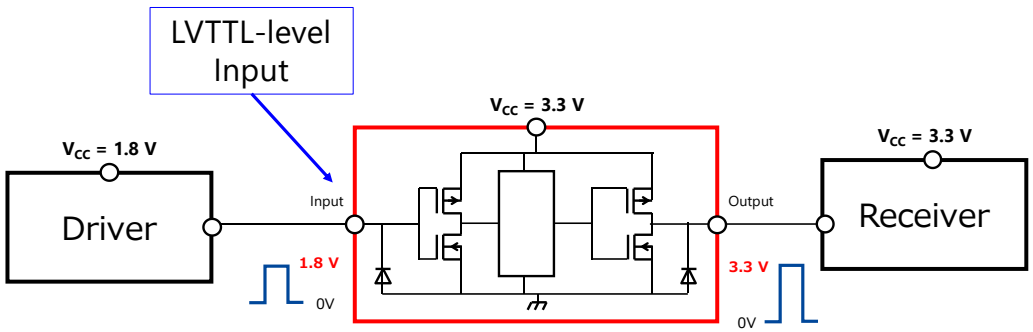


Figure 9 Example of up translation from ultralow voltage using an IC with an LVTTL-level input (7UL1T34)

4.4 Case 4: Example of up translation using a dedicated level shifter IC (buffer-type) IC (unidirectional, dual power supplies)

Step 1. Unidirectional

Step 2. Up translation

Step 3. Level-shifting range: V_{IH} minimum to 3.6 V
Up translation from a voltage lower than is possible with an L-MOS IC (7UL1T or 7UL2T of the LVP series)

Step 4. Select a dedicated level shifter IC (TC7SP/SPN or TC7WP/WPN) according to the number of level-shifting circuits required.

Step 5. Select an IC with the required propagation delay times from a product list.

Step 6. Select the optimum package according to the available board space.

Table 5 Case 4 (unidirectional, up translation, dual power supplies: V_{IH} minimum to 3.6 V)

Product Category	Product Name	Number of circuits	Package	V_{CCA}(V)	V_{CCB}(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #5	$\|I_{OH}\|/I_{OL}$ (mA)
Level Shifter	TC7SP3125	1	UF6	1.1~2.7	1.65~3.6	V_{CCA}*0.65	3.6	0.72→3.6	22	12 @V_{CCA}=1.1 V, V_{CCB}=3.0 V
	TC7SPN3125								29	3 @V_{CCA}=1.1 V, V_{CCB}=3.0 V
	TC7SPN334		MP6C		V_{CCA}~3.6				6.2	3 @V_{CCA}=1.1 V, V_{CCB}=3.0 V
	TC7WP3125	2	US8		1.65~3.6				22	12 @V_{CCA}=1.1 V, V_{CCB}=3.0 V
	TC7WPN3125								29	3 @V_{CCA}=1.1 V, V_{CCB}=3.0 V

#5 Maximum delay times at V_{CC}(opr.) max, V_{IH} minimum, T_a = 85 °C, and C_L = 30 pF

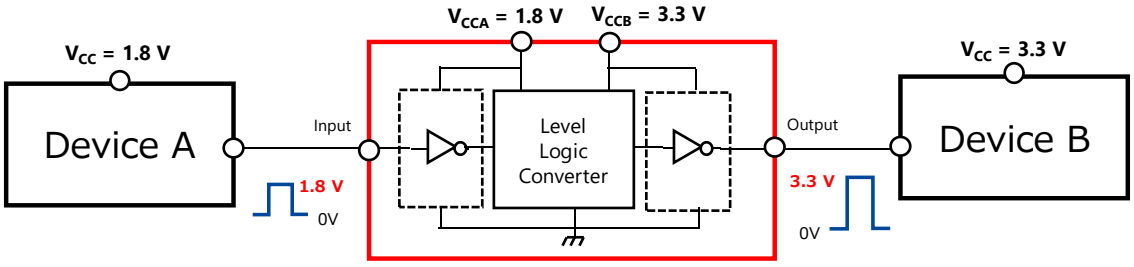


Figure 10 Example of up translation using a dual-supply dedicated level shifter IC (TC7SP3125)

4.5 Case 5: Down translation using an IC with an input-tolerant function (unidirectional, single power supply)

Using a CMOS logic or L-MOS IC

Step 1. Unidirectional

Step 2. Down translation

Step 3. Level-shifting range: Maximum voltage tolerated by the input to V_{CC}(opr.)

Step 4. Select a CMOS logic or L-MOS IC according to the number of level-shifting circuits required.

Step 5. Select an IC with the required propagation delay times from a product list.

Step 6. Select the optimum package according to the available board space.

Table 6 Case 5 (unidirectional, down translation, single power supply): Maximum voltage tolerated by the input to V_{CC}(opr.)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #6	$\|I_{OH}\|/I_{OL}$ (mA)
CMOS Logic IC	74VHC	TC74VHCxxx	1~9	DIP/SOP/TSSOP/US	2~5.5	5.5	5.5→2	10 @V_{CC}=3.3 V, CL=15 pF	8 @V_{CC}=4.5 V
		74VHCxxx		SOP/TSSOP/US	2~5.5	5.5	5.5→2		
		TC74VHCV***	4~8	TSSOP/US	1.8~5.5	5.5	5.5→1.8	10 @V_{CC}=3.3 V, CL=15 pF 15 @V_{CC}=2.3 V, CL=15 pF	16 @V_{CC}=4.5 V
		74VHCV***		TSSOP/US	1.8~5.5	5.5	5.5→1.8		
	74LCX	TC74LCX***	1~16	SOP/TSSOP/US	1.65~3.6	3.6	3.6→1.65	8.5 @V_{CC}=2.3 V, CL=30 pF 25 @V_{CC}=1.65 V, CL=30 pF	24 @V_{CC}=3.0 V
	74VCX	TC74VCX***	1 ~16	TSSOP/US	1.2~3.6	3.6	3.6→1.2	4.2 @V_{CC}=2.3 V, CL=30 pF 42 @V_{CC}=1.2 V, CL=15 pF	24 @V_{CC}=3.0 V

#6 T_a = 85°C, Function: CMOS logic IC (244)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant (V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #7	$\|I_{OH}\|/I_{OL}$ (mA)
One-Gate Logic (L-MOS)	VHS	TC7SHxxx	1	SMV/USV	2.0~5.5	5.5	5.5→2	9.5 @V_{CC}=3.3 V, CL=15 pF	8 @V_{CC}=4.5 V
		TC7WHxxx	1,2,3	SM8/US8					
	SHS	TC7SZxxx	1	USV/ESV/fSV	1.65~5.5	5.5	5.5→1.65	11.5 @V_{CC}=1.65 V, CL=15 pF 8 @V_{CC}=2.3 V, CL=15 pF	24 @V_{CC}=3.0 V
		TC7PZxxx	2	US6	1.65~5.5	5.5	5.5→1.65	10 @V_{CC}=1.65 V, CL=15 p F 7 @V_{CC}=2.3 V, CL=15 pF	
		TC7WZxxx	3	SM8/US8	1.65~5.5	5.5	5.5→1.65	11.5 @Vcc=1.65 V ,CL=15 pF 8 @Vcc=2.3 V, CL=15 pF	
	LVP	7UL1GxxxFU	1	USV	0.9~3.6	3.6	3.6→0.9	7.1 Vcc=1.65 V, CL=15 p F 5 V_{CC}=2.3 V, CL=15 pF	8 @V_{CC}=3.0 V

#7 T_a = 85°C, Functions: TC7PZ(04) for L-MOS, 125 for the other series

Product Category	Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant (V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #8	$\|I_{OH}\|/I_{OL}$ (mA)
Level Shifter	74LV4Txxx	4	TSSOP/US	4.5~5.5	5.5	5.5→4.5	5.6	16 @V_{CC}=4.5 V
				3.0~3.6		5.5→3.0	8.1	8 @V_{CC}=4.5 V
				2.3~2.7		5.5→2.3	12.4	3 @V_{CC}=2.3 V
				1.65~1.95		5.5→1.65	33.2	2 @V_{CC}=1.65 V

#8 Maximum delay times at T_a = 85°C and C_L = 30 pF, Function: Level-shifter (125)

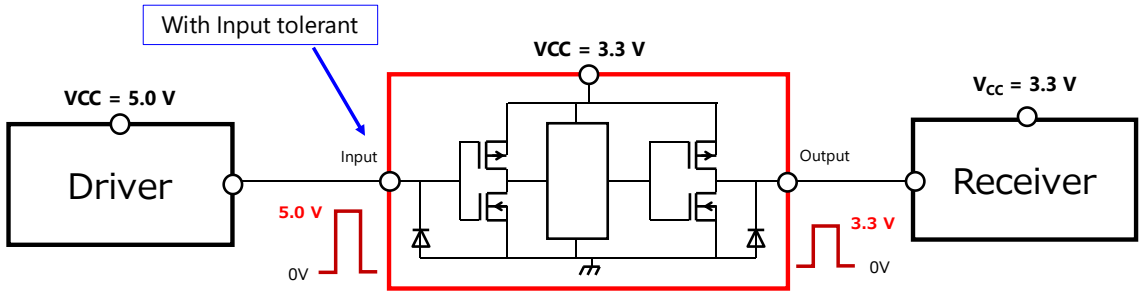


Figure 11 Example of down translation using an IC with an input-tolerant function (TC7SZ34)

4.6 Case 6: Example of down translation using an IC with an input-tolerant function and an open-drain output (unidirectional, single power supply)

Using a CMOS logic or L-MOS IC with an input-tolerant function and an open-drain output

Step 1. Unidirectional

Step 2. Down translation

Step 3. Level-shifting range: Arbitrary range from a voltage range tolerated by the input (3.6 to 5.5 V) to V_{CC}(opr.)

- If level-shifting from an ultralow voltage (0.9 V) is necessary, select the L-MOS LVP series (7UL1G07).

Step 4. Select a CMOS logic or L-MOS IC according to the number of level-shifting circuits required.

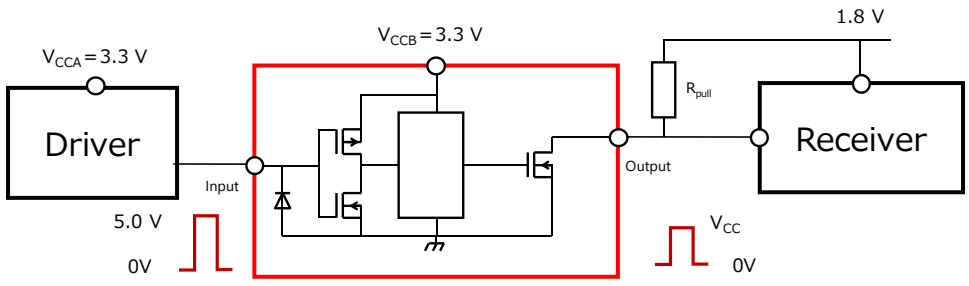
Step 5. Select an IC with the required propagation delay times (t_{PLZ} and t_{PZL}) from a product list.

Step 6. Select the optimum package according to the available board space.

Table 7 Case 6 (unidirectional, down translation, single power supply): Arbitrary range from a voltage range tolerated by the input (3.6 to 5.5) to V_{CC}(opr.)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #9	$\|I_{OH}\|/I_{OL}$ (mA)
CMOS Logic IC	74VHC	74VHC03	4	TSSOP	2~5.5	5.5	5.5→2	13 @V_{CC}=3.3 V, CL=50 pF	8 @VCC=4.5 V
		TC74VHC03		SOP/US				12 @Vcc=3.3 V, CL=50 pF	
		74VHC05/07	6	TSSOP					
		TC74VHC05/07		SOP/US					
		74VHCV05/07		TSSOP	1.8~5.5		5.5→1.8	18/15 @Vcc=2.3 V, CL=30 pF	16 @V_{CC}=4.5 V
		TC74VHCV05/07		US					
	74LCX	74LCX05/07		TSSOP	1.65~5.5		5.5→1.65	13 @Vcc=2.3 V ,CL=30 pF 26 @Vcc=1.65 V, CL=30 pF	24 @V_{CC}=4.5 V
		TC74LCX05/07		US					
Product Category		**Product Name**	**Number of circuits**	**Package**	**V_{CC}(opr.)(V)**	**Input tolerant (V)**	**Voltage translation range (V)**	**t_{PLH}/t_{PHL} (ns) #10**	**$\|I_{OH}\|/I_{OL}$ (mA)**
One-Gate Logic (L-MOS)	VHS	TC7SH09	1	SMV/USV	2.0~5.5	5.5	5.5→2	8.5 @Vcc=3.3 V, CL=15 pF	8 @V_{CC}=4.5 V
	SHS	TC7SZ05/07		SMV/USV/ESV/fSV	1.65~5.5	5.5	5.5→1.65	11 @Vcc=1.65 V, CL=50 pF	24 @V_{CC}=4.5 V
		TC7PZ05/07	2	US6	1.65~5.5	5.5		10.5 @Vcc=1.65 V, CL=50 pF	
		TC7WZ05/07	3	US8	1.65~5.5	5.5			
	LVP	7UL1G07	1	USV	0.9~3.6	3.6	3.6→0.9	10.5/7.9 @Vcc=1.65 V, CL=15 pF	8 @V_{CC}=3.0 V

#9, #10 T_a = 85°C



Equivalent circuit (with Output tolerant)

Figure 12 Example of down translation using an IC with an input-tolerant function and an open-drain output (74VHCV05)

4.7 Case 7: Example of up/down translation using a dual-supply bidirectional level-shifting bus buffer

Using a dual-supply bidirectional bus buffer or a dedicated level shifter IC (buffer-type)

Toshiba provides dual-supply bus buffers that incorporate a level shifter and an output buffer with a drive capability.

These bus buffers allow the signal direction to be changed via the DIR input pin.

Step 1. Bidirectional

Step 2. Up/down translation

Step 3. Level-shifting range: $V_{CCA} \Leftrightarrow V_{CCB}$

Step 4. Select a product according to the number of level-shifting circuits required.

Dual-supply bidirectional bus buffers

- The TC74LCX163245 and TC74LCX164245 are available in versions called the TC74LCX**R**163245 and TC74LCX**R**164245, which incorporate an internal **26-Ω output series resistor** to reduce ringing.

  The TC74LCXR163245 and TC74LCXR164245 have half the drive capability of the TC74LCX163245 and TC74LCX164245.

  TC74LCX163245: I_{OUTA} = ±24 mA minimum, I_{OUTB} = ±24 mA minimum (V_{CCA} = 4.5 V, V_{CCB} = 3.0 V)

  TC74LCXR163245: I_{OUTA} = ±12 mA minimum, I_{OUTB} = ±12 mA minimum (V_{CCA} = 4.5 V, V_{CCB} = 3.0 V)

Dedicated level shifter ICs (buffer-type)

- The TC7MP3125 is available in a version called the TC7MPN3125, which has a reduced drive capability to suppress ringing.

  TC7MP3125: I_{OHA}/I_{OLA} = ±3 mA minimum, I_{OHB}/I_{OLB} = ±12mA minimum (V_{CCA} = 1.65 V, V_{CCB} = 3.0 V)

  TC7MPN3125: I_{OHA}/I_{OLA} = ±3 mA minimum, I_{OHB}/I_{OLB} = ±3 mA minimum (V_{CCA} = 1.8 V, V_{CCB} = 3.0 V)

Step 5. Select an IC with the required propagation delay times (t_{PLH} and t_{PHL}) from a product list.

Step 6. Select the optimum package according to the available board space.

Table 8 Case 7: A dual-supply bidirectional bus buffer or a dedicated level shifter IC (bidirectional, up/down translation, dual power supplies: $V_{CCA} \Leftrightarrow V_{CCB}$)

Product Category		Product Name	Number of circuits	Package	V_{IHA}(min)(V)	V_{CCB}(V)	V_{IHB}(min)(V)	Input tolerant (V)	Voltage translation range (V)	Supply Voltage Condition	t_{PLH}/t_{PHL} (ns) @Ta=85℃	$\|I_{OH}\|/I_{OL}$ (mA)
74LCX	TC74LCX163245FT	16	TSSOP	4.5~5.5	2	2.3~3.6	1.7	5.5	5.5→2.3 (A→B) 1.7→5.5 (B→A)	$V_{CCA} > V_{CCB}$	V_{CCA}=5.0±0.5, V_{CCB}=2.5±0.2 A→B (9.0) 30 pF, B→A (8.0) 50 pF	24 (A port/B port) V_{CCA}=4.5 V, V_{CCB}=3.0 V
	TC74LCXR163245FT										V_{CCA}=5±0.5, V_{CCB}=2.5±0.2 A→B (9.5) 30 pF, B→A (9.0) 50 pF	12 (A port/B port) V_{CCA}=4.5 V, V_{CCB}=3.0 V
	TC74LCX164245FT			2.3~3.6	1.7	4.5~5.5	2		1.7→5.5 (A→B) 5.5→2.3 (B→A)	$V_{CCA} < V_{CCB}$	V_{CCA}=2.5±0.2, V_{CCB}=5±0.5 A→B (9.0) 50pF, B→A (8.4) 30pF	24 (A port/B port) V_{CCA}=4.5V, V_{CCB}=3.0V
	TC74LCXR164245FT										V_{CCA}=2.5±0.2, V_{CCB}=5±0.5 A→B (10) 50 pF, B→A (9.0) 30 pF	12 (A port/B port) V_{CCA}=4.5 V, V_{CCB}=3.0 V
74VCX	TC74VCX163245FT	16	TSSOP	2.3~3.6	1.6	1.65~2.7	V_{CCB}*0.65	3.6	3.6→1.65 (A→B) 1.1→3.6 (B→A)	$V_{CCA} > V_{CCB}$	V_{CCA}=3.3±0.3, V_{CCB}=1.8±0.15 A→B (7.1) 30pF, B→A (5.5) 30pF	24 (A port/B port) V_{CCA}=3.0 V, V_{CCB}=2.5 V
	TC74VCX164245FT			1.65~2.7	V_{CCA}*0.65	2.3~3.6	1.6		1.1→3.6 (A→B) 3.6→1.65 (B→A)	$V_{CCA} < V_{CCB}$	V_{CCA}=1.8±0.15, V_{CCB}=3.3±0.3 A→B (5.5) 30pF, B→A (7.1) 30pF	18 (A port) /24 (B port) V_{CCA}=2.3 V, V_{CCB}=3.0 V
Level Shifter	TC7MP3125	4	TSSOP/US	1.1~2.7	1.1*0.65	1.65~3.6	1.65*0.65	3.6	1.1*0.65→3.6 (A→B) 3.6→1.1 (B→A)	$V_{CCA} < V_{CCB}$	V_{CCA}=1.8±0.15, V_{CCB}=3.3±0.3 A→B (7.8) 30 pF, B→A(8.9) 15 pF	3 (A port) /12 (B port) V_{CCA}=1.65 V, V_{CCB}=3.0 V
	TC7MPN3125										V_{CCA}=1.8±0.15, V_{CCB}=3.3±0.3 A→B (14.8) 30 pF, B→A(8.9) 15 pF	3 (A port) /3 (B port) V_{CCA}=1.65 V, V_{CCB}=3.0 V

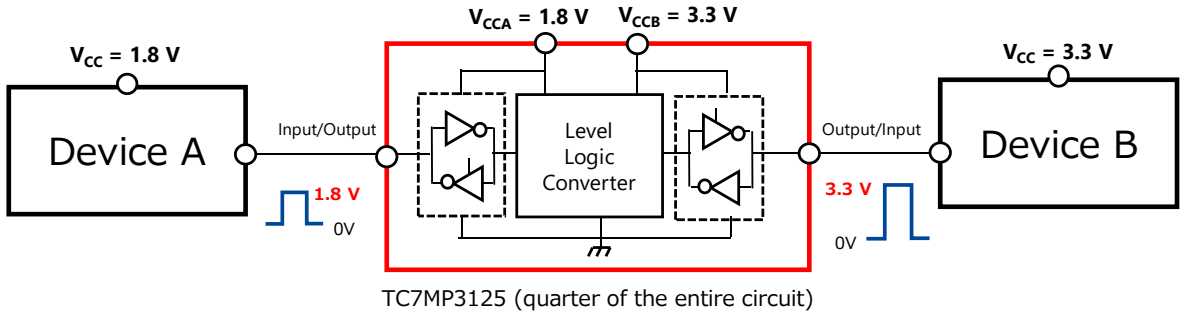


Figure 13 Case 7: Example of up/down translation using a dual-supply bidirectional dedicated level shifter IC (buffer-type) (TC7MP3125)

4.8 Case 8: Example of up/down translation using a dual-supply level shift bus switch

Using a dual-supply level shift bus switch

Toshiba provides dual-supply level shift bus switches that perform level shifting via an external pull-up resistor.

These bus switches can be used to interface between two voltage domains without the need for controlling the signal direction (DIR).

Bus switches are suitable for I^2C applications. Single-pole single-throw (SPST) and single-pole double-throw (SPDT) bus switches are available. For level-shifting, bus switches require that V_{CCA} be lower than V_{CCB}.

In addition, an appropriate pull-up resistor should be selected since steady-state current flows through the pull-up resistor. The IC draws more current when it drives a logic Low than when it drives a logic High. Since the output rise time is affected by the pull-up resistor, it differs from the output fall time.

Step 1. Bidirectional

Step 2. Up/down translation

Step 3. Level-shifting range: $V_{CCA} \Leftrightarrow V_{CCB}$

Step 4. Select a product according to the number of level-shifting circuits required.

Application example: Up/down translation (V_{CCA} = 1.65 to 5.0 V $\Leftrightarrow$ V_{CCB} = 2.3 to 5.5 V)

As SPST bus switches, the TC7SPB9306 with the active-High OE input and the TC7SPB9307 with the active-Low /OE input are available.

Multi-bit bus switches are also available.

The TC7WPBxxx are 2-bit bus switches, the TC7QPBxxx are 4-bit bus switches, and the TC7MPBxxx are 8-bit bus switches.

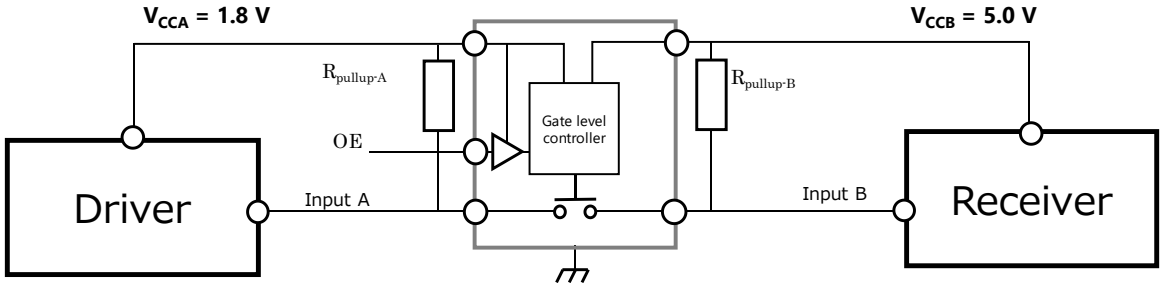
As SPDT bus switches, the TC7MPB9326 with the active-High OE input and the TC7MPB9327 with the active-Low /OE input are available. Both the TC7MPB9326 and TC7MPB9327 are two-bit bus switches.

Step 5. Select an IC with the required propagation delay times (t_{PLZ} and t_{PZL}) from a product list.

Step 6. Select the optimum package according to the available board space.

Table 9: Case 8 Dual-supply level shift bus switches (bidirectional, up/down translation, dual power supplies: $V_{CCA} \Leftrightarrow V_{CCB}$)

Product Category		Product Name	Number of circuits	Package	V_{CCA} (V)	V_{CCB} (V)	Input/Output Characteristics (translating up) (V_{OHU})	Voltage translation range (V)	Supply voltage condition	t_{PLZ}/t_{PZL} (ns) @Ta=85℃
Dual supply Level shift Bus Switch	TC7MPB9307	SPST	8	TSSOP/US	1.65~5.0	2.3~5.5	1.4@V_{CCA}=1.65 2.05@V_{CCA}=2.3 2.7@V_{CCA}=3.0	1.4→5.5 (A→B) 5.5→1.65 (B→A)	V_{CCA}<V_{CCB}	V_{CCA}=3.3±0.3、V_{CCB}=5±0.5 11/9 @RL=1 kΩ,CL=30 pF V_{CCA}=2.5±0.2, V_{CCB}=5±0.5 15/13 @RL=1 kΩ,CL=30 pF
	TC7MPB9326	SPDT								
	TC7MPB9327									
	TC7QPB9306	SPST	4							
	TC7QPB9307									
	TC7WPB9306		2	US8						
	TC7WPB9307		2							
	TC7SPB9306		1	UF6						
	TC7SPB9307		1							



Recommendation
1.8 V ⇔ 5 V (V_{CCA} < V_{CCB})
SPST : TC7SPB9306, TC7SPB9307
Line-up multiple circuits as follows
(TC7WPB, TC7QPB, TC7MPB)
SPDT : TC7MPB9326, TC7MPB9327

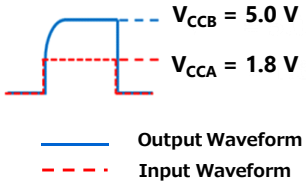
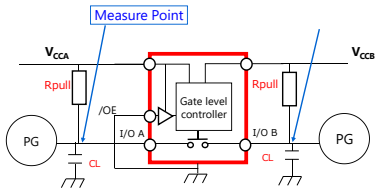


Figure 14 Example of voltage translation (Case 8: Dual-supply level-shifting bus switch)

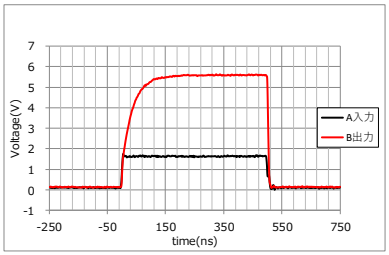
As a reference, the measured waveforms of a dual-supply level shift bus switch are shown below.

◆Dual supply level shifter switch (translation waveform)

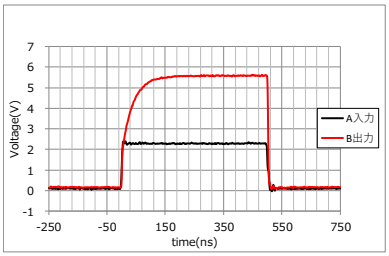
Target product : TC7SPB9307
Measure condition : CL=30 pF、Rpull=1 kΩ (A-port, B-port)
Input PG (Pulse Generator) tr=tf=3 ns
1.VCCA (1.65 V) ⇔ VCCB (5.5 V)
2.VCCA (2.3 V) ⇔ VCCB (5.5 V)
3.VCCA (3.0 V) ⇔ VCCB (5.5 V)



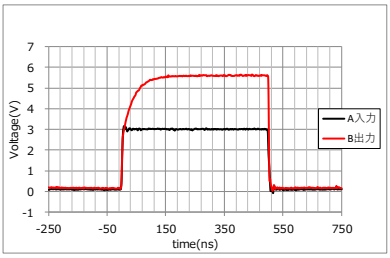
TC7SPB9307



V_{CCA} = 1.65 V, V_{CCB} = 5.5 V

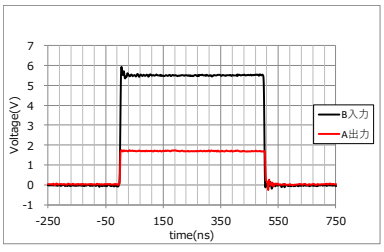


V_{CCA} = 2.3 V, V_{CCB} = 5.5 V

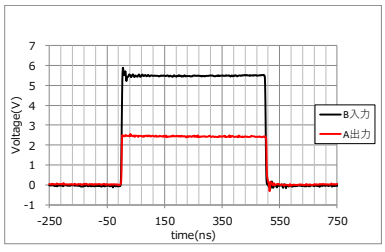


V_{CCA} = 3.0 V, V_{CCB} = 5.5 V

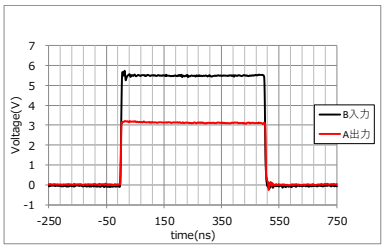
Measured waveforms when a signal flows from A to B (The B port is pulled up to V_{CCB} with a resistor.)



V_{CCA} = 1.65 V, V_{CCB} = 5.5 V



V_{CCA} = 2.3 V, V_{CCB} = 5.5 V



V_{CCA} = 3.0 V, V_{CCB} = 5.5 V

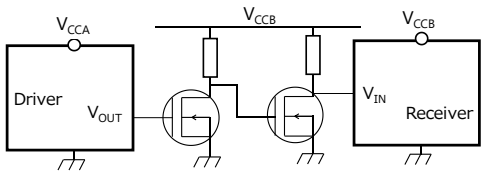
Measured waveforms when a signal flows from B to A (The A port is pulled up to V_{CCA} with a resistor.)

Figure 15 Example of level-shifting using a dual-supply level shift bus switch

5. Application examples

5.1 Replacing discrete MOSFETs with a dedicated level shifter

A level shifter can be built as shown below using two inexpensive MOSFETs. (A single MOSFET suffices if logical inversion is permitted.)



In this case, however, you need to select appropriate MOSFETs and pull-up resistors in order to satisfy the required specifications (input threshold, output voltage, propagation delay times, etc.). In contrast, level shifters simplify parts selection since their specifications are prescribed in datasheets for each supply voltage supported. It is recommended that dedicated level shifters be used for small applications.

5.2 Level-shifting for various interfaces (SPI, UART, I^2C, etc.)

It is possible to interface between two devices using a specific protocol if they have the same signal levels.

It is recommended, however, that a level shifter be used if two devices operate at different supply voltages.

Table 10 Level-shifting for various industry-standard interfaces (recommended products)

Interface Standard	Number of lines	Signal Direction	Speed	Recommendation (In case of less than 2 Slaves)
UART	4	TX (Device A → Device B) RX (Device A ← Device B) RTS (Device A → Device B) CTS (Device A ← Device B)	9600bps, 115200bps (Standard) (max. 1Mbps approximately)	TC7MP3125/MPN3125 TC7QPB9306/9307 TC7MPB9307
	2	TX (Device A → Device B) RX (Device A ← Device B)	9600bps,115200bps (Standard) (max. 1Mbps approximately)	TC7MP3125/MPN3125 TC7WPB9306/9307 TC7QPB9306/9307
I2C	2	SCL (Master → Slave) SDA (Master ⇔ Slave)	Standard-mode(Sm) :max. 100kbps Fast-mode (Fm) :max. 400 kbps Fast-mode Plus (Fm+) :max. 1Mbps High-speed (Hs-mode) :max. 3.4Mbps → above 4modes: 8bit serial bidirectional data transfer Ultra Fast-mode (UFm) :max. 5Mbps → above mode: 8bit serial unidirectional data transfer	TC7WPB9306/9307 TC7QPB9306/9307 TC7MPB9307
SPI	4	MISO (Slave → Master) MOSI (Master → Slave) SCL (Master → Slave) SS (Master → Slave)	Several Mbps	TC7MP3125/MPN3125 7UL1G34 7UL1T34 TC7QPB9306/9307 TC7MPB9307

5.2.1 Example of level-shifting for a four-line UART interface

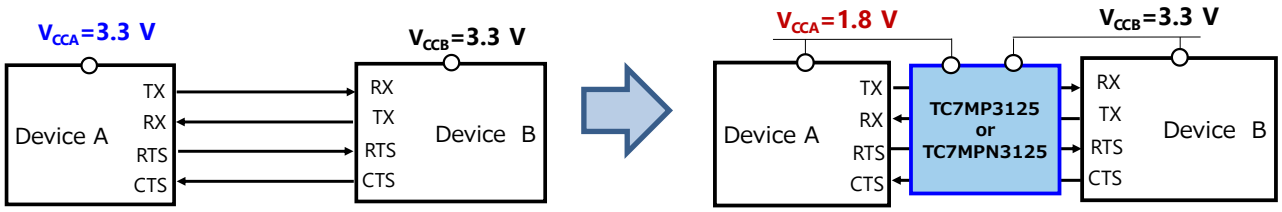


Figure 16 Example of level-shifting for a four-line UART interface

Suppose, for example, that you want to reduce the supply voltage of Device A from 3.3 V to 1.8 V. However, when V_{CCA} = 1.8 V, the output voltage (V_{OUT}) of the TX and RTS pins of Device A becomes lower than the input threshold (V_{IH}) of Device B, causing it to malfunction. In addition, the output voltage of the TX and CTS pins of Device B becomes higher than the supply voltage of Device A, possibly causing damage to Device A.
In this case, level-shifting can be easily accomplished by inserting a level shifter between these two devices.
In the above case, the TC7MP3125 or TC7MPN3125 bus transceiver is ideal since they both allow the signal direction to be controlled per group of two bits.
Moreover, these bus transceivers do not require any external part.

Visit the following URLs to view or download their datasheets:
TC7MP3125 : 2-Bit × 2 Dual Supply Bus Transceiver
TC7MP3125FT Package (TSSOP16B)
TC7MP3125FK Package (US16)
TC7MPN3125 : 2-Bit × 2 Dual Supply Bus Transceiver
(Low noise type by reducing B port drive capability)
TC7MPN3125FT Package (TSSOP16B)
TC7MPN3125FK Package (US16)

5.2.2 Example of level-shifting for a two-line UART interface

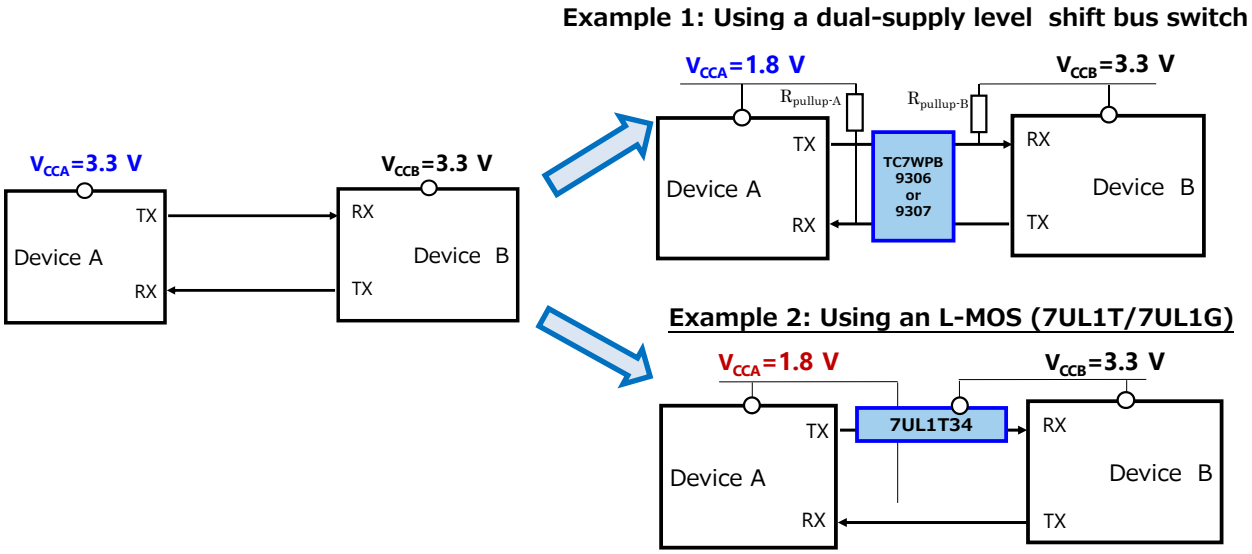


Figure 17 Example of level-shifting for a two-line UART interface

Suppose, for example, that you want to reduce the supply voltage of Device A from 3.3 V to 1.8 V. However, when V_{CCA} = 1.8 V, the output voltage (V_{OUT}) of the TX pin of Device A becomes lower than the input threshold (V_{IH}) of Device B, causing it to malfunction. In addition, the output voltage of the TX pin of Device B becomes higher than the supply voltage of Device A, possibly causing damage to Device A.

In this case, level-shifting can be easily accomplished by inserting a level shifter between these two devices.

Example 1: The 7UL1T34 is ideal for up translation (from 1.8 V to 3.3 V) whereas the 7UL1G34 is ideal for down translation (from 3.3 V to 1.8 V).

Example 2: The TC7WPB9306 or TC7WPB9307 bus transceiver is also ideal. However, these bus transceivers require external pull-up resistors to pull the output signals to the V_{CC} level.

Visit the following URLs to view or download the datasheets for these bus/buffer transceivers:

TC7WPB9306FK : 2-Bit Dual-Supply Bus Switch（Control input: OE）, Package（US8）

TC7WPB9307FK : 2-Bit Dual-Supply Bus Switch（Control input: /OE）, Package（US8）

7UL1G34FU : Non-inverter, Package（USV）

7UL1T34FU : Non-Inverter with Level Shifting, Package（USV）

5.2.3 Example of level-shifting for an I²C interface

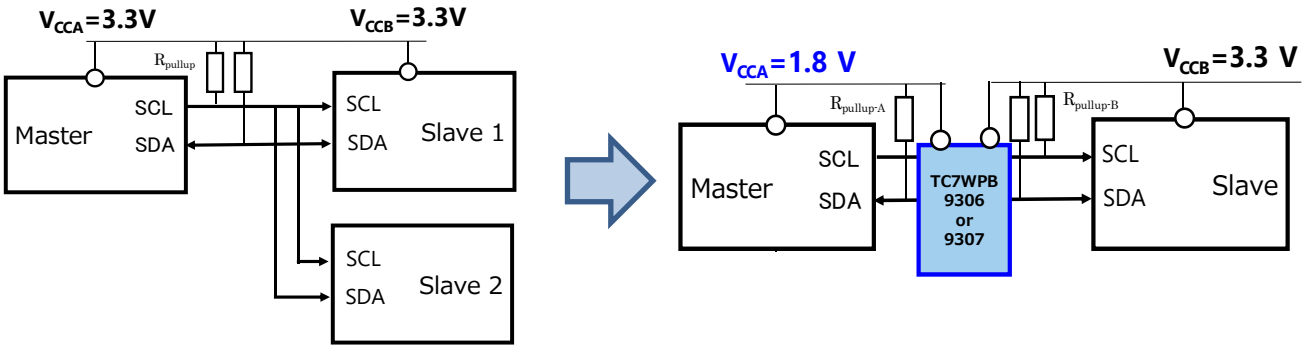


Figure 18 Example of level-shifting for an I²C interface

Suppose, for example, that you want to reduce the supply voltage of the master device from 3.3 V to 1.8 V. However, when V_{CCA} = 1.8 V, the output voltage (V_{OUT}) of the SCL and SDA pins of the master device becomes lower than the input threshold (V_{IH}) of the slave devices, causing them to malfunction. In addition, the output voltage of the SDA pin of the slave devices becomes higher than the supply voltage of the master device, possibly causing damage to the master device.
In this case, level-shifting can be easily accomplished by inserting a level shifter between the master and slave devices.
In the above case, the TC7WPB9306 is ideal for SDA and SCL.
External pull-up resistors (of the order of 1 kΩ) are required to pull up the outputs to the V_{CC} level.
Visit the following URLs to view or download the datasheets for the TC7WPB9306 and TC7WPB9307 bus transceivers:

TC7WPB9306FK : 2-Bit Dual-Supply Bus Switch（Control input: OE）, Package（US8）
TC7WPB9307FK : 2-Bit Dual-Supply Bus Switch（Control input: /OE）, Package（US8）

5.2.4 Examples of level-shifting for an SPI interface

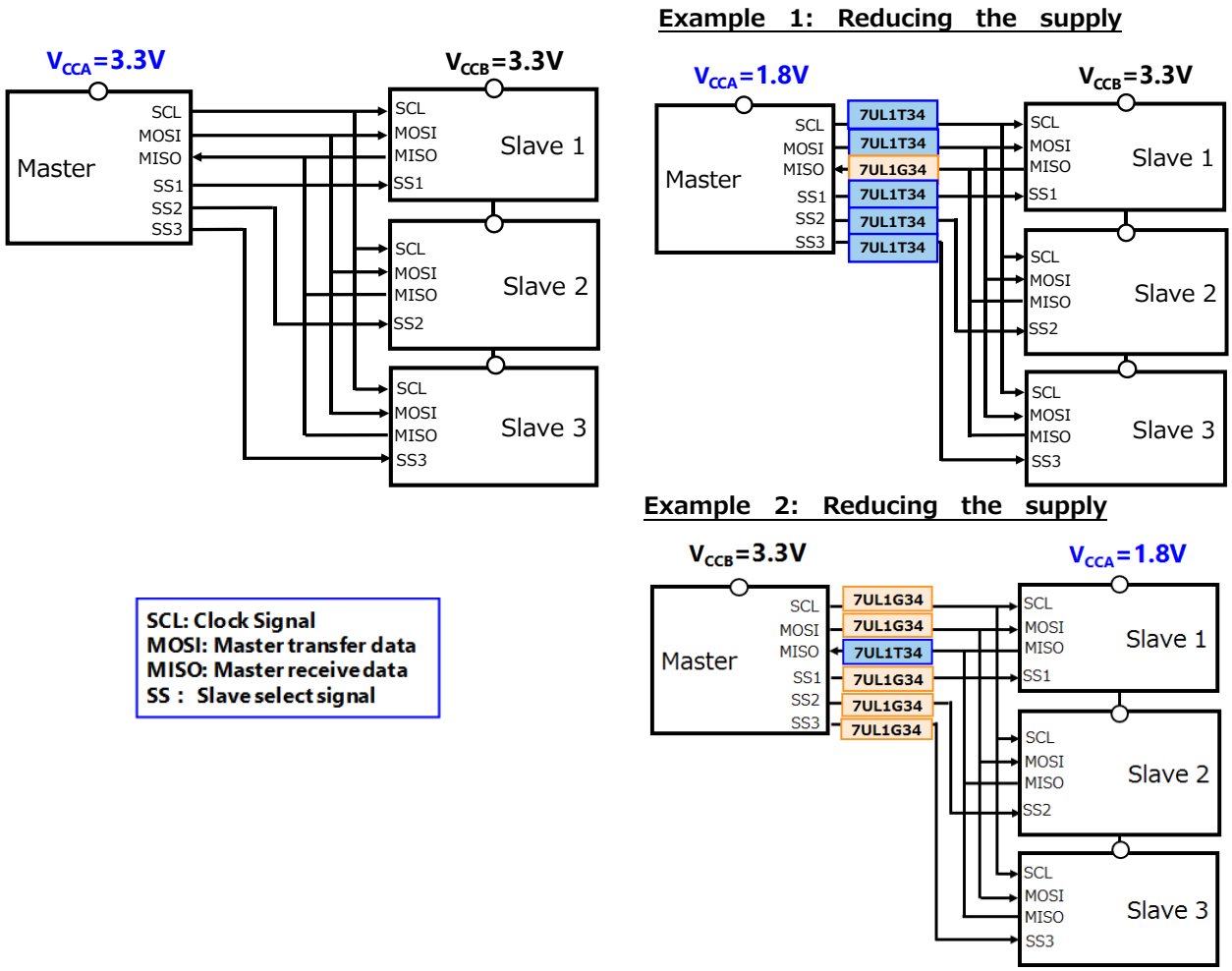


Figure 19 Examples of level-shifting for an SPI interface

Example 1: Suppose, for example, that you want to reduce the supply voltage of the master device from 3.3 V to 1.8 V. However, when V_{CCA} = 1.8 V, the output voltage (V_{OUT}) of the SCL, MOSI, and SS1 to SS3 pins of the master device becomes lower than the input threshold (V_{IH}) of the slave devices, causing them to malfunction. In addition, the input voltage of the MISO pin of the master device becomes higher than its supply voltage, possibly causing damage to it. In Example 1, level-shifting can be easily accomplished by inserting level shifters between these master and slave devices.

Example 2: Suppose, for example, that you want to reduce the supply voltage of the slave devices from 3.3 V to 1.8 V. However, when V_{CCB} = 1.8 V, the output voltage (V_{OUT}) of the MOSO pin of the slave devices becomes lower than the input threshold (V_{IH}) of the master device, causing it to malfunction. In addition, the output voltage of the SCL, MOSI, and SS1 to SS3 pins of the master device becomes higher than the supply voltage of the slave devices, possibly causing damage to them. In Example 2, level-shifting can be easily accomplished by inserting level shifters between the master and slave devices.

Visit the following URLs to view or download the datasheets for bus transceivers:

7UL1G34FU : Non-inverter, Package (USV)
7UL1T34FU : Non-Inverter with Level Shifting, Package (USV)

Conclusion

This application note has discussed how to select level shifters (voltage translation ICs).

In some cases, CMOS logic ICs with a TTL-level input or an open-drain output provide level-shifting without using costly level shifters. It is therefore important to select the optimum device, taking available board space and part costs into consideration.

We hope that you have found this application note useful in considering the use of Toshiba's level shifters.

To perform a parametric search of Toshiba's level shifter ICs → Click Here

Appendix Lists of products and packages

Lists of Toshiba's level shifters

List of level shifters #1 (unidirectional, up translation)
List of level shifters #2 (unidirectional, down translation)
List of level shifters #3 (bidirectional, up/down translation)

Toshiba's Level Shifters Line-up #1 (Unidirectional・Up translation)

Utilize TTL-Input Vcc=4.5 -5V)

Utilize Open-Drain +Output tolerant

Utilize LVTTL-input (VCC=2.3-3.6V)

Utilize TTL/LVTTL-input (VCC=1.65-5.5V)

Single supply

Dual Supply

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range(V)	t_{PLH}/t_{PHL} (ns) #1	$\lvert I_{OH}/I_{OL}\rvert$ (mA)
CMOS Logic IC	74HC	TC74HCTxxx	1~8	DIP/SOP/TSSOP	4.5~5.5	2	5.5	2→5.5	28	6 @V_{CC}=4.5V
		74HCTxxx		SOIC/TSSOP	4.5~5.5	2	5.5	2→5.5		
	74AC	TC74ACTxxx	4,6,8	DIP/SOP/TSSOP	4.5~5.5	2	5.5	2→5.5	9	24 @V_{CC}=4.5V
	74VHC	TC74VHCTxxx	1~8	DIP/SOP/TSSOP/US	4.5~5.5	2	5.5	2→5.5	9.5	8 @V_{CC}=4.5V
		74VHCTxxx	1~8	TSSOP	4.5~5.5	2	5.5	2→5.5		
Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range(V)	t_{PLH}/t_{PHL} (ns) #1	$\lvert I_{OH}/I_{OL}\rvert$ (mA)
One-gate Logic (L-MOS)	TTL-level input	TC7WTxxx	2	SM8	4.5~5.5	2	5.5	2→5.5	28	6 @V_{CC}=4.5V
		TC7SETxxx	1	SMV/USV	4.5~5.5	2	5.5	2→5.5	11.9	8 @V_{CC}=4.5V

#1: max value at V_{CC}(opr.) max, Ta=85 ℃, CL=50 pF, Function : CMOS logic IC(244)/L-MOS(125)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #2	$\lvert I_{OH}/I_{OL}\rvert$ (mA)
CMOS Logic IC	74VHC	74VHCV05/07	6	TSSOP	1.8~5.5	1.65	5.5	1.65→5.5	8.5	16 @V_{CC}=4.5V
		TC74VHCV05/07		US	1.8~5.5	1.65	5.5	1.65→5.5		
	74LCX	74LCX05/07		TSSOP	1.65~5.5	1.65*0.9	5.5	1.5→5.5	4	24 @V_{CC}=3.0V
		TC74LCX05/07		US	1.65~5.5	1.65*0.9	5.5	1.5→5.5		
Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(Max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #2	$\lvert I_{OH}/I_{OL}\rvert$ (mA)
One-gate Logic (L-MOS)	VHS	TC7SH09	1	SMV/USV	2.0~5.5	1.5	5.5	1.5→5.5	8	8 @V_{CC}=4.5V
	SHS	TC7SZ05/07	2	SMV/USV/ESV/fSV	1.65~5.5	1.65*0.75	5.5	1.3→5.5	4.5	24 @V_{CC}=3.0V
		TC7PZ05/07		US6	1.65~5.5	1.65*0.75	5.5	1.3→5.5	3.9	
		TC7WZ05/07	3	US8	1.65~5.5	1.65*0.75	5.5	1.3→5.5	3.9	
	LVP	7UL1G07	1	USV	0.9~3.6	0.9	3.6	0.9→3.6	12.8/4.1	8 @V_{CC}=3.0V

#2: max value at V_{CC}(opr.)max, Ta=85 ℃, CL=50 pF (7UL1G:30pF), Function : CMOS logic IC(05)/L-MOS(05,07,09)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #3	$\lvert I_{OH}/I_{OL}\rvert$ (mA)
One-gate Logic (L-MOS)	LVP	7UL1Txxx	1	USV	2.3~3.6	1.1	3.6	1.1→3.6	4.7/5.0	8 @V_{CC}=3.3V
		7UL2Txxx	2	US8	2.3~3.6	1.1	3.6	1.1→3.6	7.5/5.2	

#3: max value at V_{CC} (opr.)max, V_{IN}=1.65 V, Ta=85℃, CL=15 pF, Function : L-MOS(125)

Product Category	Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	V_{IH}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #4	$\lvert I_{OH}/I_{OL}\rvert$ (mA)
Level Shifter	74LV4Txxx	4	TSSOP/US	4.5~5.5	2	5.5	2→5.5	5.6	16 @V_{CC}=4.5V
				3.0~3.6	1.35	3.6	1.35→3.6	8.1	8 @V_{CC}=3.0V
				2.3~2.7	1.2	2.7	1.2→2.7	12.4	3 @V_{CC}=2.3V
				1.65~1.95	1	1.95	1→1.95	33.2	2 @V_{CC}=1.65V

#4:max value at V_{CC} (opr.)max, V_{IH}(min), Ta=85 ℃, CL=30 pF, Function : CMOS logic IC(125)

Product Category	Product Name	Number of circuits	Package	V_{CCA}(V)	V_{IA}(min)(V)	V_{OUT}(max)(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #5	$\lvert I_{OH}/I_{OL}\rvert$ (mA)
Level Shifter	TC7SP3125	1	UF6	1.1~2.7	1.65~3.6	3.6	0.72~3.6	22	12 @V_{CCA}=1.1V/V_{CCB}=3.0V
	TC7SPN3125							29	3 @V_{CCA}=1.1V/V_{CCB}=3.0V
	TC7SP334		MP6C		VccA~3.6			6.2	3 @V_{CCA}=1.1V/V_{CCB}=3.0V
	TC7WP3125	2	US8		1.65~3.6			22	12 @V_{CCA}=1.1V/V_{CCB}=3.0V
	TC7WPN3125							29	3 @V_{CCA}=1.1V/V_{CCB}=3.0V

VccA*0.65

#5: max value at V_{CC} (opr.)max, V_{IH}(min), Ta=85 ℃,CL=30 pF

Toshiba's Level Shifters Line-up #2 (Unidirectional· Down translation)

Single Supply

Utilize Input Tolerant

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #6	$\|I_{OH}\|/I_{OL}$ (mA)
CMOS Logic IC	74VHC	TC74VHCxxx	1~9	DIP/SOP/TSSOP/US	2~5.5	5.5	5.5→2	10 @V_{CC}=3.3V,CL=15pF	8 @V_{CC}=4.5V
		74VHCxxx		SOP/TSSOP/US	2~5.5	5.5	5.5→2		
		TC74VHCV***	4~8	TSSOP/US	1.8~5.5	5.5	5.5→1.8	10 @V_{CC}=3.3V,CL=15pF 15 @V_{CC}=2.3V,CL=15pF	16 @V_{CC}=4.5V
		74VHCV***		TSSOP/US	1.8~5.5	5.5	5.5→1.8		
	74LCX	TC74LCX***	1~16	SOP/TSSOP/US	1.65~3.6	3.6	3.6→1.65	8.5 @V_{CC}=2.3V,CL=30pF 25 @V_{CC}=1.65V,CL=30pF	24 @V_{CC}=3.0V
	74VCX	TC74VCX***	1~16	TSSOP/US	1.2~3.6	3.6	3.6→1.2	4.2 @V_{CC}=2.3V,CL=30pF 42 @V_{CC}=1.2V,CL=15pF	24 @V_{CC}=3.0V

#6: Ta=85 ℃, Function : CMOS logic IC (244)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant (V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #7	$\|I_{OH}\|/I_{OL}$ (mA)
One-Gate Logic (L-MOS)	VHS	TC7SHxxx	1	SMV/USV	2.0~5.5	5.5	5.5→ 2	9.5 @V_{CC}=3.3V,CL=15pF	8 @V_{CC}=4.5V
		TC7WHxxx	1,2,3	SM8/US8					
	SHS	TC7SZxxx	1	USV/ESV/fSV	1.65~5.5	5.5	5.5→1.65	11.5 @V_{CC}=1.65V,CL=15pF 8 @V_{CC}=2.3V,CL=15pF	24 @V_{CC}=3.0V
		TC7PZxxx	2	US6	1.65~5.5	5.5	5.5→1.65	10 @V_{CC}=1.65V,CL=15 p F 7 @V_{CC}=2.3V,CL=15pF	
		TC7WZxxx	3	SM8/US8	1.65~5.5	5.5	5.5→1.65	11.5 @Vcc=1.65V,CL=15pF 8 @Vcc=2.3V,CL=15pF	
	LVP	7UL1GxxxFU	1	USV	0.9~3.6	3.6	3.6→0.9	7.1 Vcc=1.65V,CL=15 p F 5 V_{CC}=2.3V,CL=15pF	8 @V_{CC}=3.0V

#7:Ta=85 ℃, Function: L-MOS TC7PZ(04), except TC7PZ (125)

Product Category	Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant (V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #8	$\|I_{OH}\|/I_{OL}$ (mA)
Level Shifter	74LV4Txxx	4	TSSOP/US	4.5~5.5	5.5	5.5→4.5	5.6	16 @V_{CC}=4.5V
				3.0~3.6		5.5→3.0	8.1	8 @V_{CC}=4.5V
				2.3~2.7		5.5→2.3	12.4	3 @V_{CC}=2.3V
				1.65~1.95		5.5→1.65	33.2	2 @V_{CC}=1.65V

#8: max value at Ta=85 ℃, CL=30 pF, Function : Level Shifter (125)

Toshiba's Level Shifters Line-up #2 (Unidirectional・Down translation)

Single Supply

Utilize Input tolerant (Open−drain)

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant(V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #9	$\|I_{OH}\|/I_{OL}$ (mA)
CMOS Logic IC	74VHC	74VHC03	4	TSSOP	2~5.5	5.5	5.5→2	13 @V_{CC}=3.3V,CL=50pF	8 @VCC=4.5V
		TC74VHC03		SOP/US					
		74VHC05/07	6	TSSOP				12 @Vcc=3.3V,CL=50pF	
		TC74VHC05/07		SOP/US					
		74VHCV05/07		TSSOP	1.8~5.5		5.5→1.8	18/15 @Vcc=2.3V,CL=30pF	16 @V_{CC}=4.5V
		TC74VHCV05/07		US					
	74LCX	74LCX05/07		TSSOP	1.65~5.5		5.5→1.65	13 @Vcc=2.3V,CL=30pF	24 @V_{CC}=4.5V
		TC74LCX05/07		US				26 @Vcc=1.65V,CL=30pF	

Product Category		Product Name	Number of circuits	Package	V_{CC}(opr.)(V)	Input tolerant (V)	Voltage translation range (V)	t_{PLH}/t_{PHL} (ns) #10	$\|I_{OH}\|/I_{OL}$ (mA)
One-Gate Logic (L-MOS)	VHS	TC7SH09	1	SMV/USV	2.0~5.5	5.5	5.5→2	8.5 @Vcc=3.3V,CL=15pF	8 @V_{CC}=4.5V
	SHS	TC7SZ05/07		SMV/USV/ESV/fSV	1.65~5.5	5.5	5.5→1.65	11 @Vcc=1.65V,CL=50pF	24 @V_{CC}=4.5V
		TC7PZ05/07	2	US6	1.65~5.5	5.5		10.5 @Vcc=1.65V,CL=50pF	
		TC7WZ05/07	3	US8	1.65~5.5	5.5			
	LVP	7UL1G07	1	USV	0.9~3.6	3.6	3.6→0.9	10.5/7.9 @Vcc=1.65V,CL=15pF	8 @V_{CC}=3.0V

#9、#10:Ta=85 ℃

Toshiba's Level Shifters Line-up #3 (Bidirectional, Up/Down translation)

Dual Supply

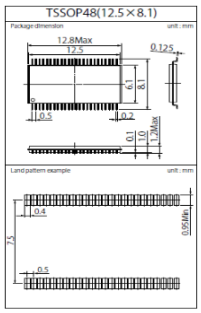
Buffer Type

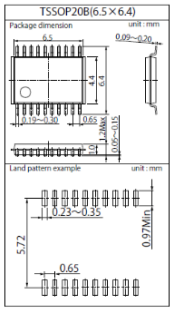
Product Category		Product Name	Number of circuits	Package	V_{IHA}(min)(V)	V_{CCB}(V)	V_{IHB}(min)(V)	Input tolerant (V)	Voltage translation range (V)	Supply Voltage Condition	t_{PLH}/t_{PHL} (ns) @Ta=85℃	$\|I_{OH}\|/I_{OL}$ (mA)
74LCX	TC74LCX163245FT	16	TSSOP	4.5~5.5	2	2.3~3.6	1.7	5.5	5.5→2.3 (A→B) 1.7→5.5 (B→A)	$V_{CCA}>V_{CCB}$	V_{CCA}=5.0±0.5, V_{CCB}=2.5±0.2 A→B (9.0) 30pF, B→A (8.0) 50pF	24 (A port/B port) V_{CCA}=4.5V, V_{CCB}=3.0V
	TC74LCXR163245FT										V_{CCA}=5±0.5, V_{CCB}=2.5±0.2 A→B (9.5) 30pF, B→A (9.0) 50pF	12 (A port/B port) V_{CCA}=4.5V, V_{CCB}=3.0V
	TC74LCX164245FT			2.3~3.6	1.7	4.5~5.5	2		1.7→5.5 (A→B) 5.5→2.3 (B→A)	$V_{CCA}<V_{CCB}$	V_{CCA}=2.5±0.2, V_{CCB}=5±0.5 A→B (9.0) 50pF, B→A (8.4) 30pF	24 (A port/B port) V_{CCA}=4.5V, V_{CCB}=3.0V
	TC74LCXR164245FT										V_{CCA}=2.5±0.2, V_{CCB}=5±0.5 A→B (10) 50pF, B→A (9.0) 30pF	12 (A port/B port) V_{CCA}=4.5V, V_{CCB}=3.0V
74VCX	TC74VCX163245FT	16	TSSOP	2.3~3.6	1.6	1.65~2.7	V_{CCB}*0.65	3.6	3.6→1.65 (A→B) 1.1→3.6 (B→A)	$V_{CCA}>V_{CCB}$	V_{CCA}=3.3±0.3, V_{CCB}=1.8±0.15 A→B (7.1) 30pF, B→A (5.5) 30pF	24 (A port/B port) V_{CCA}=3.0V, V_{CCB}=2.5V
	TC74VCX164245FT			1.65~2.7	V_{CCA}*0.65	2.3~3.6	1.6		1.1→3.6 (A→B) 3.6→1.65 (B→A)	$V_{CCA}<V_{CCB}$	V_{CCA}=1.8±0.15, V_{CCB}=3.3±0.3 A→B (5.5) 30pF, B→A (7.1) 30pF	18 (A port) /24 (B port) V_{CC}A=2.3V, V_{CCB}=3.0V
Level Shifter	TC7MP3125	4	TSSOP/US	1.1~2.7	1.1*0.65	1.65~3.6	1.65*0.65	3.6	1.1*0.65→3.6 (A→B) 3.6→1.1 (B→A)	$V_{CCA}<V_{CCB}$	V_{CCA}=1.8±0.15, V_{CCB}=3.3±0.3 A→B (7.8) 30pF, B→A(8.9) 15pF	3 (A port) /12 (B port) V_{CCA}= 1.65V, V_{CCB}=3.0V
	TC7MPN3125										V_{CCA}=1.8±0.15, V_{CCB}=3.3±0.3 A→B (14.8) 30pF, B→A(8.9) 15pF	3 (A port) /3 (B port) V_{CCA}=1.65V, V_{CCB}=3.0V

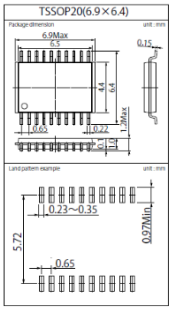
Level Shift Bus Switch

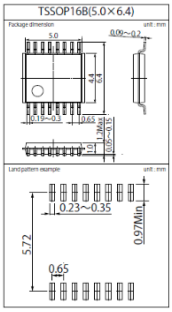
Product Category		Product Name	Number of circuits	Package	V_{CCA} (V)	V_{CCB} (V)	Input/Output Characteristics (translating up) (V_{OHU})	Voltage translation range (V)	Supply voltage condition	t_{PHZ}/t_{PZL} (ns) @Ta=85℃
Dual supply Level shift Bus Switch	TC7MPB9307	SPST	8	TSSOP/US	1.65~5.0	2.3~5.5	1.4@V_{CCA}=1.65 2.05@V_{CCA}=2.3 2.7@V_{CCA}=3.0	1.4→5.5 (A→B) 5.5→1.65 (B→A)	$V_{CCA}<V_{CCB}$	V_{CCA}=3.3±0.3, V_{CCB}=5±0.5 11/9 @RL=1 kΩ,CL=30pF V_{CCA}=2.5±0.2, V_{CCB}=5±0.5 15/13 @RL=1kΩ,CL=30pF
	TC7MPB9326	SPDT								
	TC7MPB9327									
	TC7QPB9306		4							
	TC7QPB9307									
	TC7WPB9306	SPST	2	US8						
	TC7WPB9307		2							
	TC7SPB9306		1	UF6						
	TC7SPB9307		1							

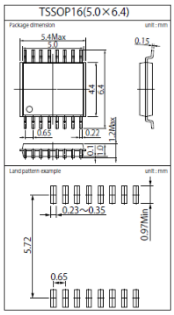
Lists of packages for Toshiba's level shifters

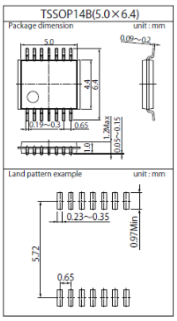


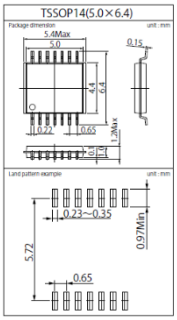


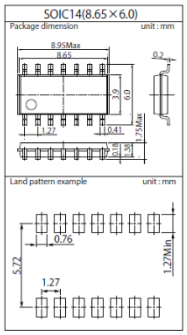


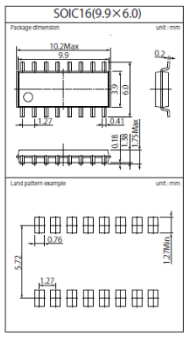


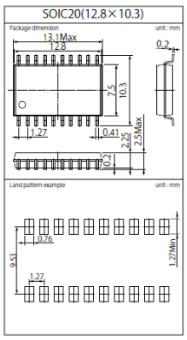


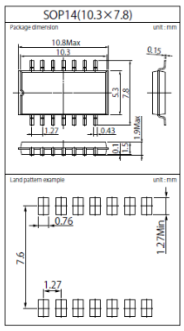


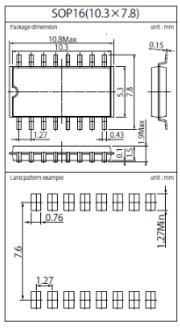


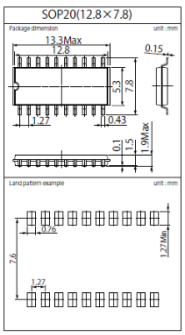


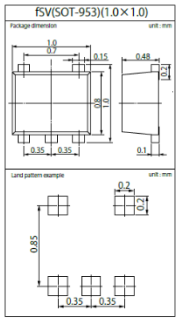


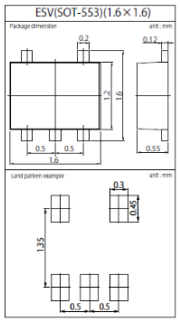


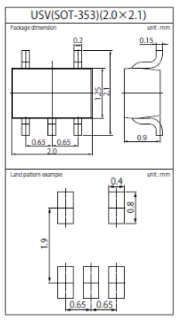


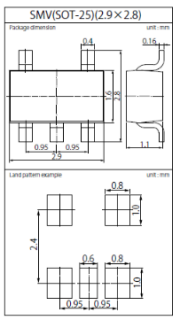


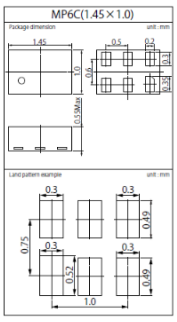


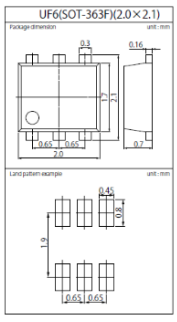


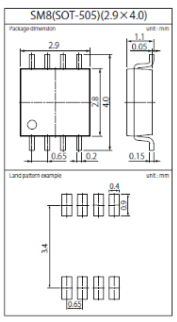


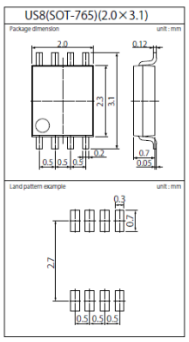


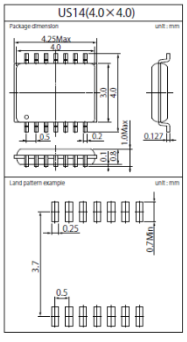


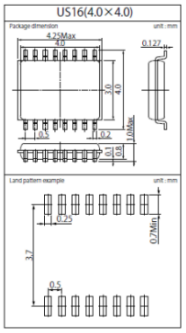


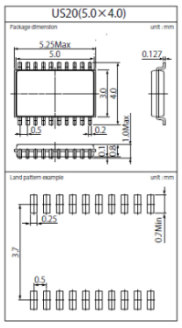












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