TCK321G, TCK322G, and TCK323 Load Switch ICs for 2-to-1 Power Multiplexing Application Note

Outline:

This application note describes the TCK321G, TCK322G, and TCK323 two-input, one-output load switch ICs incorporating a multiplexer for selecting between two input power lines.
The power multiplexing function of load switch ICs is ideal for the power management of battery chargers for mobile devices (e.g., smartphones and tablets) having two charging ports.

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1. Introduction

A load switch IC for 2-to-1 power multiplexing (power multiplexer IC) selects between two input power lines and forwards the selected input to the subsequent IC or circuitry. The TCK321G, TCK322G, and TCK323G (hereinafter collectively referred to as the TCK32*G) are ideal for the power management of high-current, high-voltage battery charging applications for smartphones, tablets, and other mobile devices having two charging ports. The TCK32*G series incorporates inrush current limiting (slew rate control), thermal shutdown, overvoltage lockout, undervoltage lockout, reverse current blocking, and flag output functions. Fabricated with a high-voltage CMOS process, the TCK32*G 2-to-1 power multiplexer ICs support an input voltage up to 36 V. In addition, the TCK32*G series provides not only Manual Selection mode in which an input power line is selected via an external control signal but also Auto Selection mode in which an input power line is automatically selected according to input voltages. The Auto Selection mode eliminates the need for an external control signal, enabling the TCK32*G series to operate on its own.

This application note describes the functions and operations of the TCK32*G. For details of the protection functions and other features available with the TCK32*G, see their datasheets.

To download the datasheet for the TCK321G → Click Here

To download the datasheet for the TCK322G → Click Here

To download the datasheet for the TCK323G → Click Here

2. Application examples for the TCK32*G

Figure 2.1 shows an example of a multiplexer circuit using the TCK32*G, which selects between two input power lines and forwards the selected input to the output. This circuit supplies either V_{INA} from a USB connector or V_{INB} from a wireless charger to a mobile device.

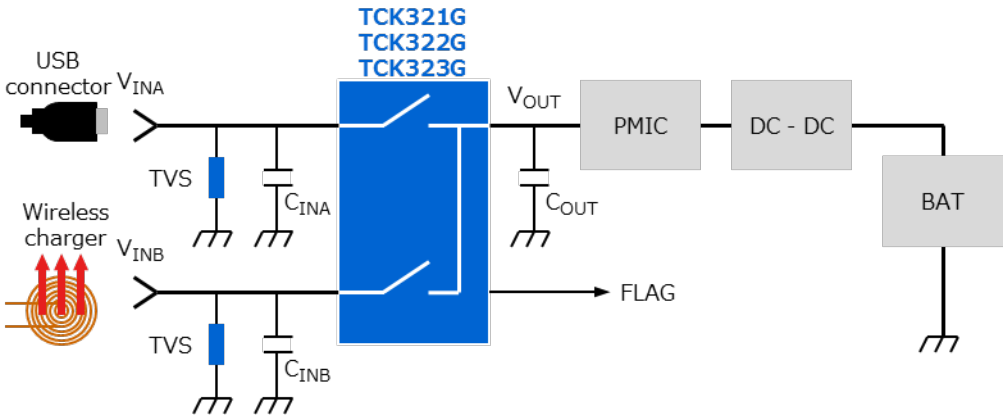

Figure 2.1 Example of a multiplexer circuit using the TCK321G, TCK322G and TCK323G

Figure 2.2 and Figure 2.3 show equivalent multiplexer circuits using discrete devices and non-multiplexing load switch ICs, respectively. The use of the TCK32*G, a dedicated power multiplexer IC, helps reduce parts counts and therefore the system size.

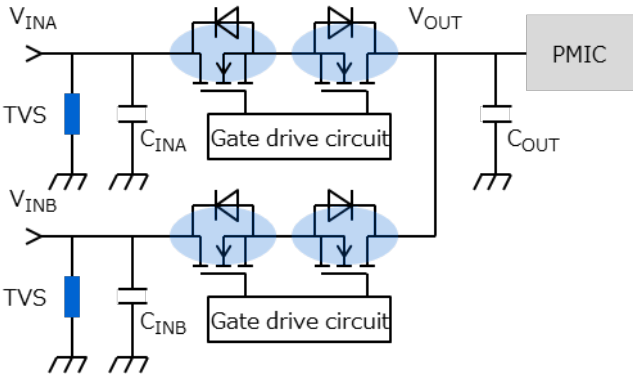

Figure 2.2 Example of a multiplexer circuit composed of discrete devices

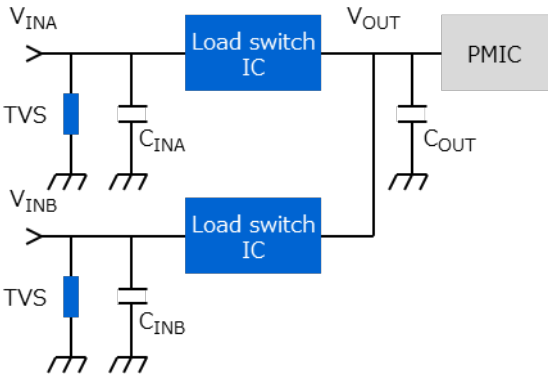

Figure 2.3 Example of a multiplexer circuit composed of non-multiplexing load switch ICs

3. Differences among the TCK321G, TCK322G, and TCK323G

The TCK321G, TCK322G, and TCK323G differ in the input power line whose state is indicated by the FLAG output in Auto Selection mode (V_{INA} state in the case of the TCK321G and TCK322G and V_{INB} state in the case of the TCK323G) as well as in overvoltage lockout threshold.

Table 3.1 Functions available with and differences among the TCK321G, TCK322G, and TCK323G

Part number	Overvoltage lockout (OVLO)		Undervoltage lockout (UVLO)		Inrush current limiting	Thermal shutdown (TSD)	Overcurrent protection	Break-before-make	Reverse current blocking (at switch-off)	FLAG output (in Auto Selection mode)
	V_{INA}	V_{INB}	V_{INA}	V_{INB}						
TCK321G	✓ 12.0 V (typ.)	✓ 12.0 V (typ.)	✓ 2.6 V (typ.)	✓ 2.6 V (typ.)	✓	✓	–	✓	✓	✓ Q_1 (V_{INA}) state
TCK322G	✓ 15.0 V (typ.)	✓ 15.0 V (typ.)	✓ 2.6 V (typ.)	✓ 2.6 V (typ.)	✓	✓	–	✓	✓	✓ Q_1 (V_{INA}) state
TCK323G	✓ 15.0 V (typ.)	✓ 15.0 V (typ.)	✓ 2.6 V (typ.)	✓ 2.6 V (typ.)	✓	✓	–	✓	✓	✓ Q_2 (V_{INB}) state

4. Block diagram of the TCK32*G and descriptions of internal blocks

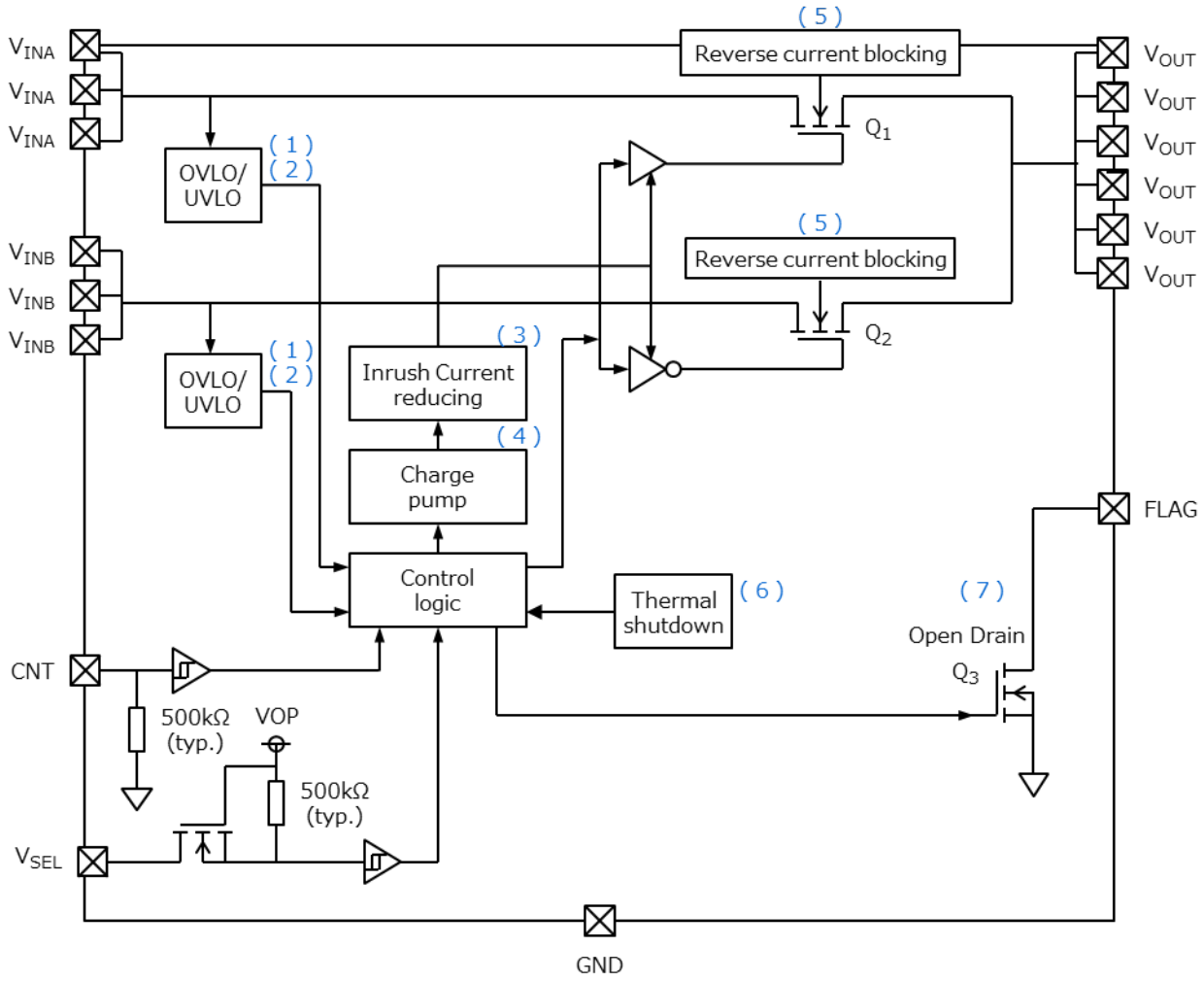

Figure 4.1 Block diagram of the TCK32*G

4.1. Overvoltage lockout (OVLO) circuit [Figure 4.1(1)]

When either V_{INA} or V_{INB} exceeds a threshold, the overvoltage lockout (OVLO) circuit turns off the V_{OUT} outputs to protect the ICs and circuits connected to them. The OVLO circuit is tripped when V_{INA} or V_{INB} exceeds the overvoltage lockout rising threshold (V_{OVL_RI}). Then, when V_{INA} or V_{INB} drops below the overvoltage lockout falling threshold (V_{OLV_FA}), the V_{OUT} output turns back on automatically. The OVLO circuit compares V_{INA} or V_{INB} with a voltage derived by dividing the reference voltage (V_{REF}) as shown in Figure 4.2. When V_{INA} or V_{INB} exceeds the divided reference voltage (V_{OVDET}), the comparator output is toggled, then turning off the V_{OUT} outputs. At the same time, the N-channel MOSFET for reference voltage (comparator input) selection turns on, then the reference voltage switches to V_{OVDET_r}. When V_{INA} or V_{INB} drops below V_{OVDET_r} again, the comparator output is toggled again, turning the V_{OUT} outputs back on.

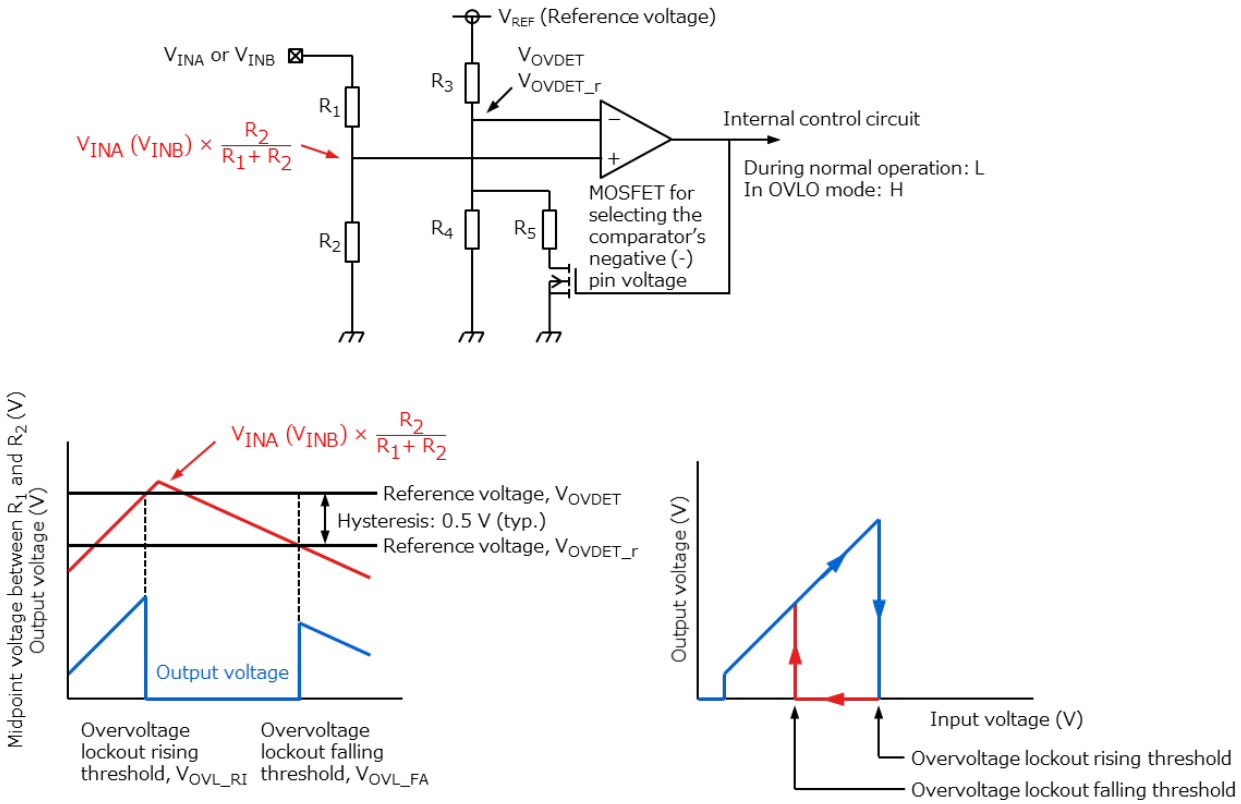

Figure 4.2 Overvoltage lockout operation

When recovering from overvoltage lockout, the OVLO circuit allows a hold time of 15 ms typical to prevent a false output due to input chattering as shown in 4.3.

Test conditions: C_{IN} = 1 µF, C_{OUT} = 1 µF, R_L = 50 Ω

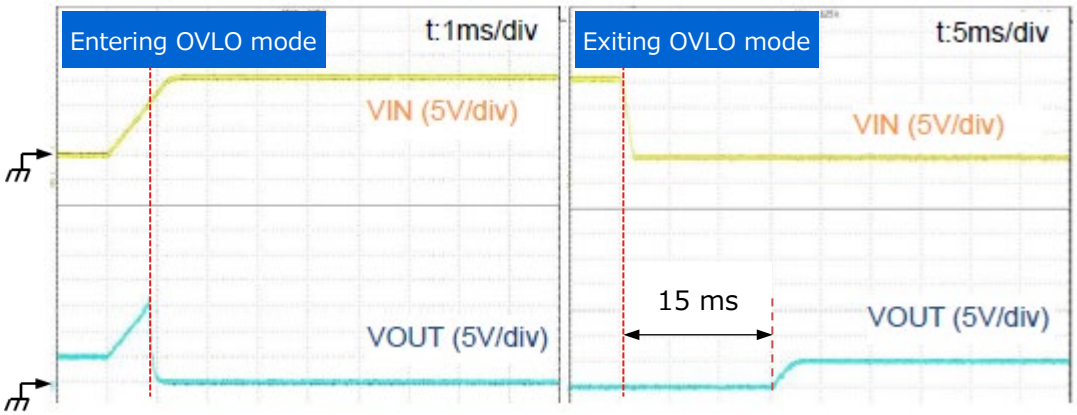

Figure 4.3 Example of operations when entering and exiting OVLO mode

Table 4.1 Comparison of overvoltage lockout thresholds among the TCK32*G

Part number	Characteristics	Symbol	Test Condition	T_a = 25°C			T_a = 40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
TCK321G	Overvoltage lockout (OVLO) rising threshold	V_{OVL_RI}	–	–	12.0	–	10.5	13.5	V
	Overvoltage lockout (OVLO) falling threshold	V_{OVL_FA}	–	–	V_{OVL_RI} - 0.5	–	–	–	V
TCK322G	Overvoltage lockout (OVLO) rising threshold	V_{OVL_RI}	–	–	15.0	–	13.4	16.6	V
	Overvoltage lockout (OVLO) falling threshold	V_{OVL_FA}	–	–	V_{OVL_RI} - 0.5	–	–	–	V
TCK323G	Overvoltage lockout (OVLO) rising threshold	V_{OVL_RI}	–	–	15.0	–	13.4	16.6	V
	Overvoltage lockout (OVLO) falling threshold	V_{OVL_FA}	–	–	V_{OVL_RI} - 0.5	–	–	–	V

4.2. Undervoltage lockout (UVLO) circuit [Figure 4.1(2)]

When either V_{INA} or V_{INB} drops below the minimum operating voltage of the ICs or circuits connected to the V_{OUT} outputs, the undervoltage lockout (UVLO) circuit turns off the V_{OUT} outputs to prevent system malfunction. The UVLO circuit is tripped when either V_{INA} or V_{INB} drops below the undervoltage lockout falling threshold voltage (V_{UVL_FA}). The UVLO circuit has hysteresis. When V_{INA} or V_{INB} rises back above V_{UVL_RI}, the V_{OUT} outputs turn back on automatically. The UVLO circuit compares V_{INA} or V_{INB} with a voltage derived by dividing the reference voltage (V_{REF}) as shown in Figure 4.4. When V_{INA} or V_{INB} drops below the divided reference voltage (V_{UVDET}), the comparator output is toggled, then the V_{OUT} outputs turn off. At the same time, the N-channel MOSFET for reference voltage selection turns off, then the reference voltage switches to V_{UVDET_r}. When V_{INA} or V_{INB} rises back above V_{UVDET_r}, the comparator is toggled again, turning the V_{OUT} outputs back on.

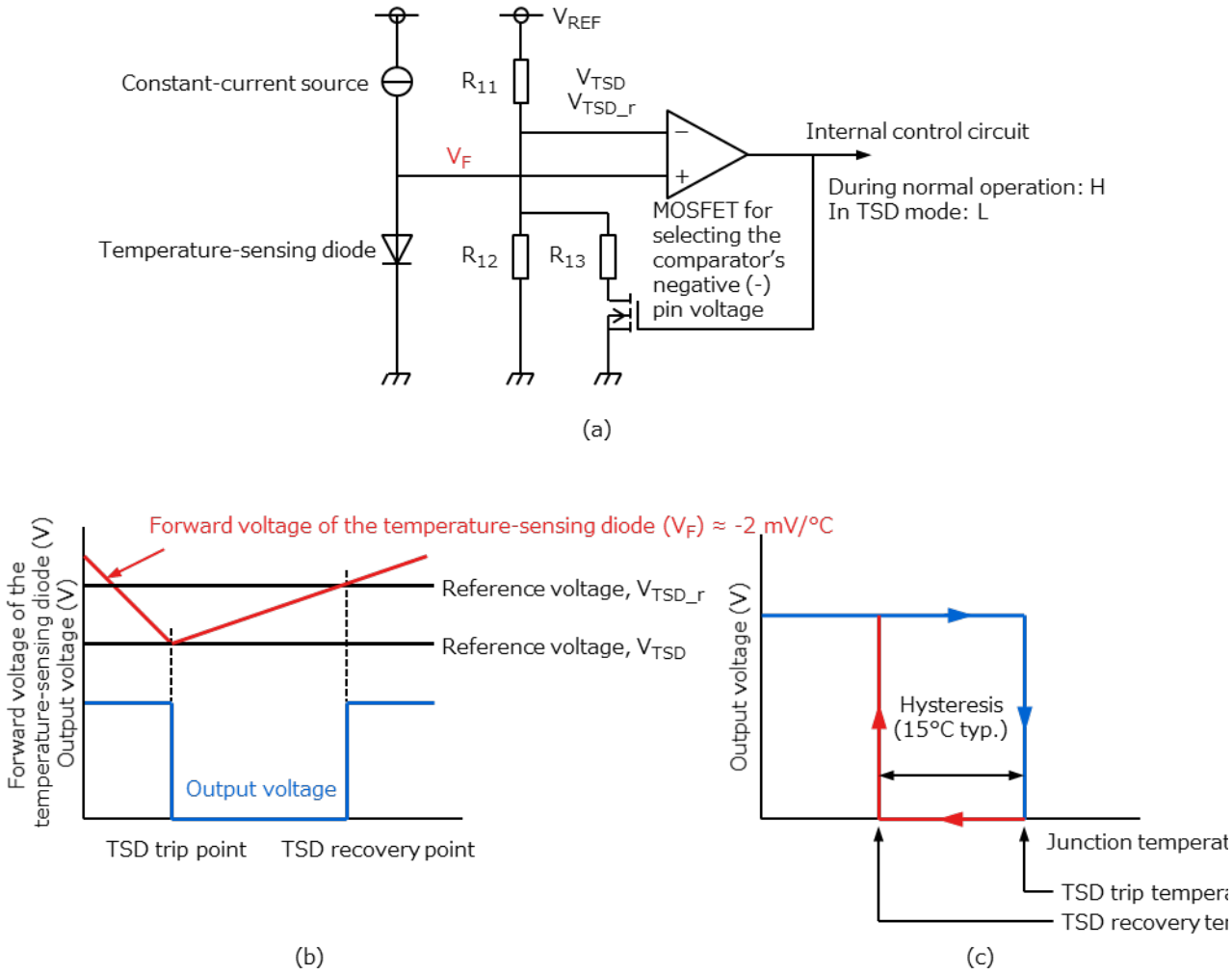

Figure 4.4 Undervoltage lockout operation

Table 4.2 Undervoltage lockout thresholds of the TCK32*G

Part number	Characteristics	Symbol	Test Condition	T_a = 25°C			T_a = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
TCK321G TCK322G TCK323G	Undervoltage lockout (UVLO) rising threshold	V_{UVL_RI}	–	–	2.9	–	2.3	3.5	V
	Undervoltage lockout (UVLO) falling threshold	V_{UVL_FA}	–	–	V_{UVL_RI} - 0.3	–	–	–	V

4.3. Inrush current limiting (slew rate control) circuit [Figure 4.1(3)]

Inrush current is limited by a slew rate control circuit. When a large capacitive load is connected to the output MOSFET, its turning on at high speed causes a large current to flow to charge the load. At this time, V_{IN} drops instantaneously because of the impedance of board traces on the V_{DD} side of a load switch IC, it may cause system instability or malfunction. To prevent this situation, the inrush current limiting circuit turns on the output MOSFET at a low slew rate, and charging slowly the capacitive load. Thereby it ensures a stable system start-up.

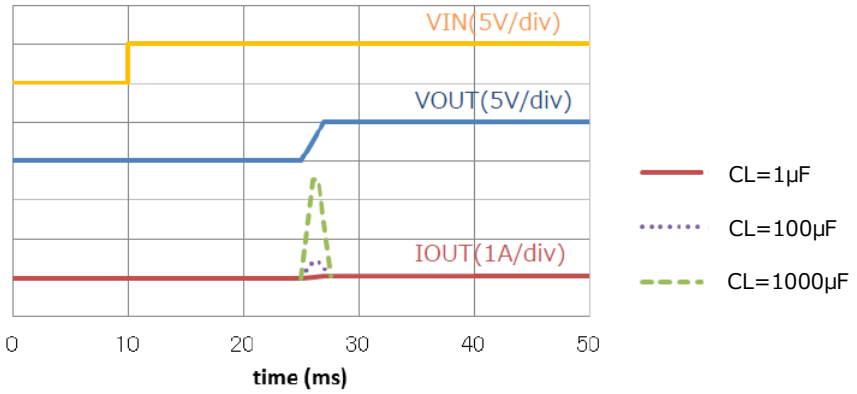

Figure 4.5 Output current waveform when inrush current is limited

4.4. Charge pump circuit [Figure 4.1(4)]

The charge pump circuit is a voltage booster that generates a voltage for driving the gate of the N-channel MOSFET.

4.5. Reverse current blocking circuit [Figure 4.1(5)]

While the internal MOSFET switch is off, the reverse current blocking circuit prevents current from flowing in the reverse direction from V_{OUT} to V_{INA} or V_{INB} when V_{INA} or $V_{INB} < V_{OUT}$. This circuit is disabled while the MOSFET is on.

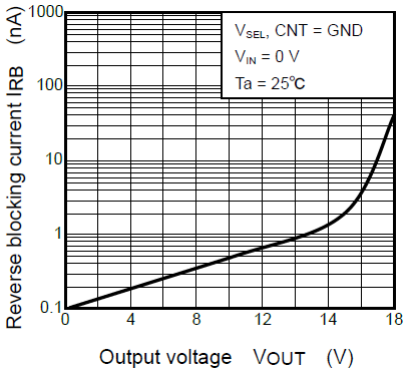

Figure 4.6 Reverse blocking current (I_{RB})-vs-output voltage (V_{OUT}) curve of the TCK32*G

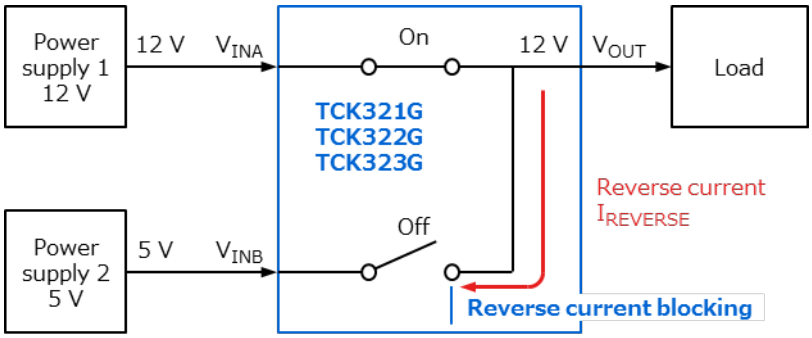

Figure 4.7 Reverse current blocking operation during switching between two power supplies

4.6. Thermal shutdown (TSD) circuit [Figure 4.1(6)]

The thermal shutdown (TSD) circuit monitors the junction temperature to protect the TCK32*G. When the junction temperature exceeds a threshold, the TSD circuit turns off the V_{OUT} outputs to prevent the TCK32*G from degrading or being damaged permanently. The TSD circuit detects the junction temperature by comparing a diode's forward voltage (V_F) with a reference voltage (V_{TSD}) that is hardly affected by temperature as shown in Figure 4.8(a). When the TCK32*G is operating properly, V_F is higher than V_{TSD}. The diode's forward voltage has a temperature coefficient of roughly -2 mV/°C. When the junction temperature reaches 158°C typical, V_F drops below V_{TSD}. This causes the comparator output to toggle, and the IC turned off. At this point, the TSD circuit switches the reference voltage from V_{TSD} to V_{TSD_r} via the comparator's output signal. Once the TCK32*G turns off, its power consumption decreases considerably, it causes the junction temperature to decrease. When a decrease of junction temperature causes V_F to rise above V_{TSD_r}, the V_{OUT} outputs turn back on automatically. The TSD circuit has a hysteresis of 15°C typical, i.e., there is a temperature difference of 15°C between the junction temperature at which TSD is tripped to turn off the V_{OUT} outputs and the junction temperature at which TSD is recovered.

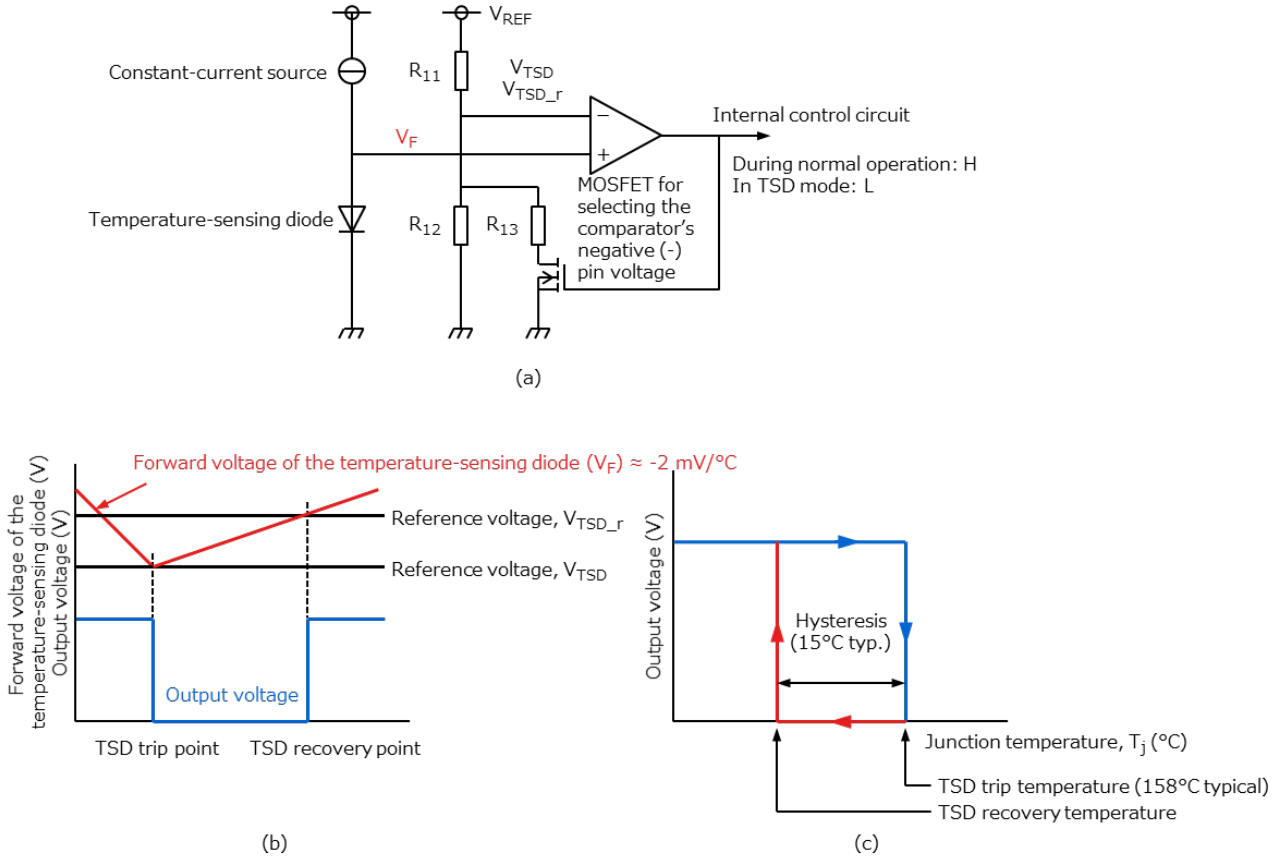

Figure 4.8 Thermal shutdown operation

4.7. FLAG output circuit [Figure 4.1(7)]

When the overvoltage or undervoltage lockout circuit is tripped, the FLAG output pin transitions from Low to High to warn a power management IC (PMIC) and other external IC of a system fault. Since the FLAG output has an open drain configuration, an external pull up resistor should be connected to the FLAG output. Select a pull up resistor, the resistance value should be determined in consideration of the sink current of the FLAG output and fully evaluate it with an actual board. (In the datasheet, V_{OL} is specified as 0.4 V maximum when I_{SINK} = 1 mA.)

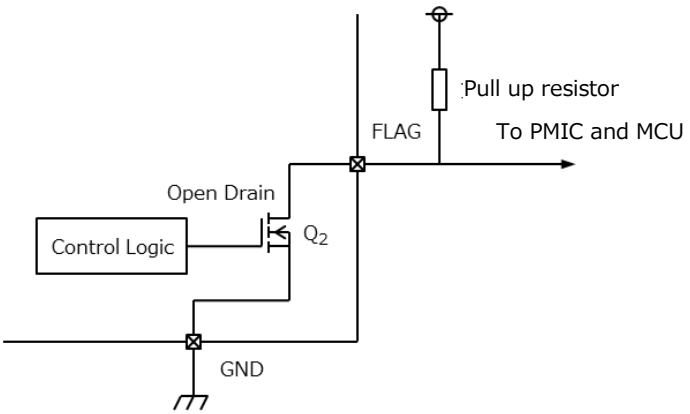

Figure 4.9 Equivalent circuit for the FLAG output

4.8. Other circuit in the TCK32*G

4.8.1. Break-before-make circuit

The TCK32*G incorporates two switches. After the TCK32*G "breaks" one switch, the break-before-make circuit keeps two switches off until it "makes" the other switch. This prevents two voltage domains from being short-circuited during the changeover between two switches.

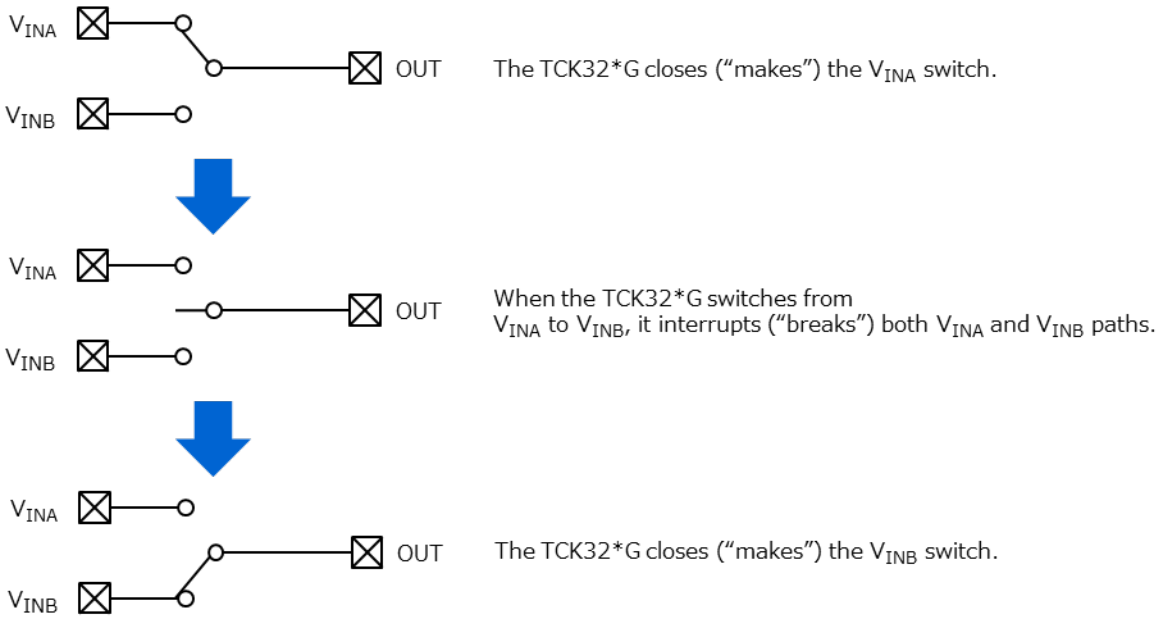

Figure 4.10 Break-before-make operation

5. Internal circuits at the control input pins

5.1. Internal circuit at the CNT pin

A pull-down resistor with a typical value of 500 kΩ is internally connected between the CNT and GND pins.

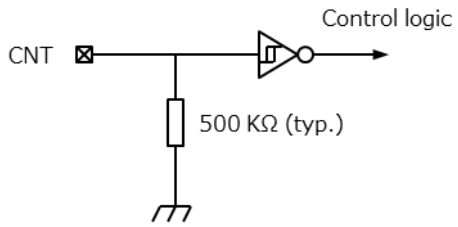

Figure 5.1 Internal circuit at the CNT pin

5.2. Internal circuit at the V_{SEL} pin

A resistor with a typical value of 500 kΩ and a MOSFET for voltage conversion are internally connected to the V_{SEL} pin. This resistor is pulled up to an internal 3-V power supply(VOP).

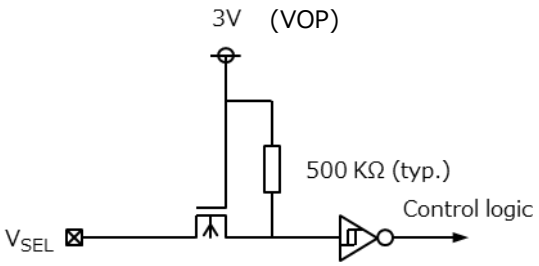

Figure 5.2 Internal circuit at the V_{SEL} pin

6. Control modes of the TCK32*G

The TCK32*G can be configured into Off, Auto Selection or Manual Selection mode via the Mode Control (CNT) and Input Selector (V_{SEL}) inputs while taking advantage of the break-before-make characteristics. The following subsections describe the operation in each mode.

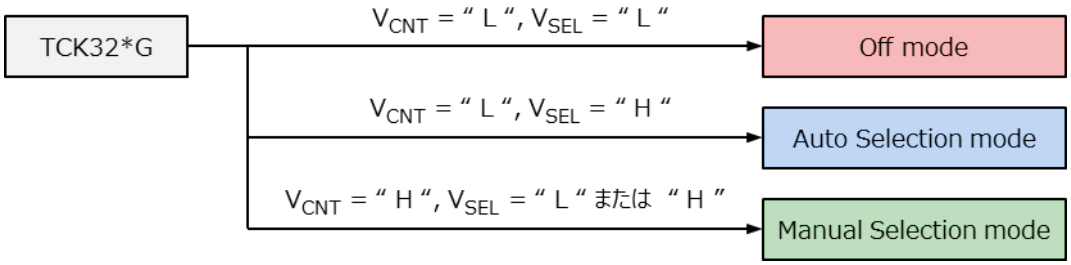

Figure 6.1 Control modes of the TCK32*G

6.1. Off Mode

Table 6.1 Operations of the TCK321G, TCK322G, and TCK323G in Off mode

When V_{CNT}= Low and V_{SEL} = Low

Input voltage	Independent of the voltages at V_{INA} and V_{INB}
Output voltage	Off (Disabled)
FLAG output	Off (High-Z)
Reverse current blocking	V_{INA}: Valid V_{INB}: Valid

6.2. Auto Selection mode

The TCK32*G is configured into Auto Selection mode when V_{CNT} is Low and V_{SEL} is High. In this mode, the TCK32*G transfers the voltage at the V_{INA} inputs to the V_{OUT} outputs if both V_{INA} and V_{INB} are within the normal voltage range. However, the TCK32*G transfers the voltage at the V_{INB} inputs to the V_{OUT} outputs if V_{INA} is in the overvoltage or undervoltage lockout range. The FLAG output differs among the TCK321G, TCK322G, and TCK323G as shown below.

Table 6.2 Operations of the TCK321G, TCK322G, and TCK323G in Auto Selection mode

When V_{CNT} = Low and V_{SEL} is High

Input voltage		V_{INA}: In the operating voltage range V_{INB}: In the operating voltage range	V_{INA}: In the operating voltage range V_{INB}: Outside the operating voltage range	V_{INA}: Outside the operating voltage range V_{INB}: In the operating voltage range	V_{INA}: Outside the operating voltage range V_{INB}: Outside the operating voltage range
Output voltage		On (V_{OUT}=V_{INA})	On (V_{OUT}=V_{INA})	On (V_{OUT}=V_{INB})	Off (Disabled)
FLAG output	TCK321G: Indicates the V_{INA} state	On (Low)	On (Low)	Off (High-Z)	Off (High-Z)
	TCK322G: Indicates the V_{INA} state	On (Low)	On (Low)	Off (High-Z)	Off (High-Z)
	TCK323G: Indicates the V_{INB} state	Off (High-Z)	Off (High-Z)	On (Low)	Off (High-Z)
Reverse current blocking		V_{INA}: Invalid V_{INB}: Valid	V_{INA}: Invalid V_{INB}: Valid	V_{INA}: Valid V_{INB}: Invalid	V_{INA}: Valid V_{INB}: Valid

In the operating voltage range: $V_{ULV\_RI}<V_{IN*}<V_{OVL\_RI}$

Outside the operating voltage range: $V_{UVL\_FA}>V_{IN*}$ or $V_{IN*}>V_{OVL\_RI}$

6.2.1. Timing diagram of the TCK321G and TCK322G in Auto Selection mode

In the case of the TCK312G and TCK322G, the FLAG output indicates the V_{INA} state in Auto Selection mode regardless of the V_{INB} state. The FLAG output remains Low while V_{INA} is in the normal voltage range, and is driven High when the overvoltage or undervoltage lockout circuit is tripped. See Section 7.1 for a description of its hold time (t_{HD}).

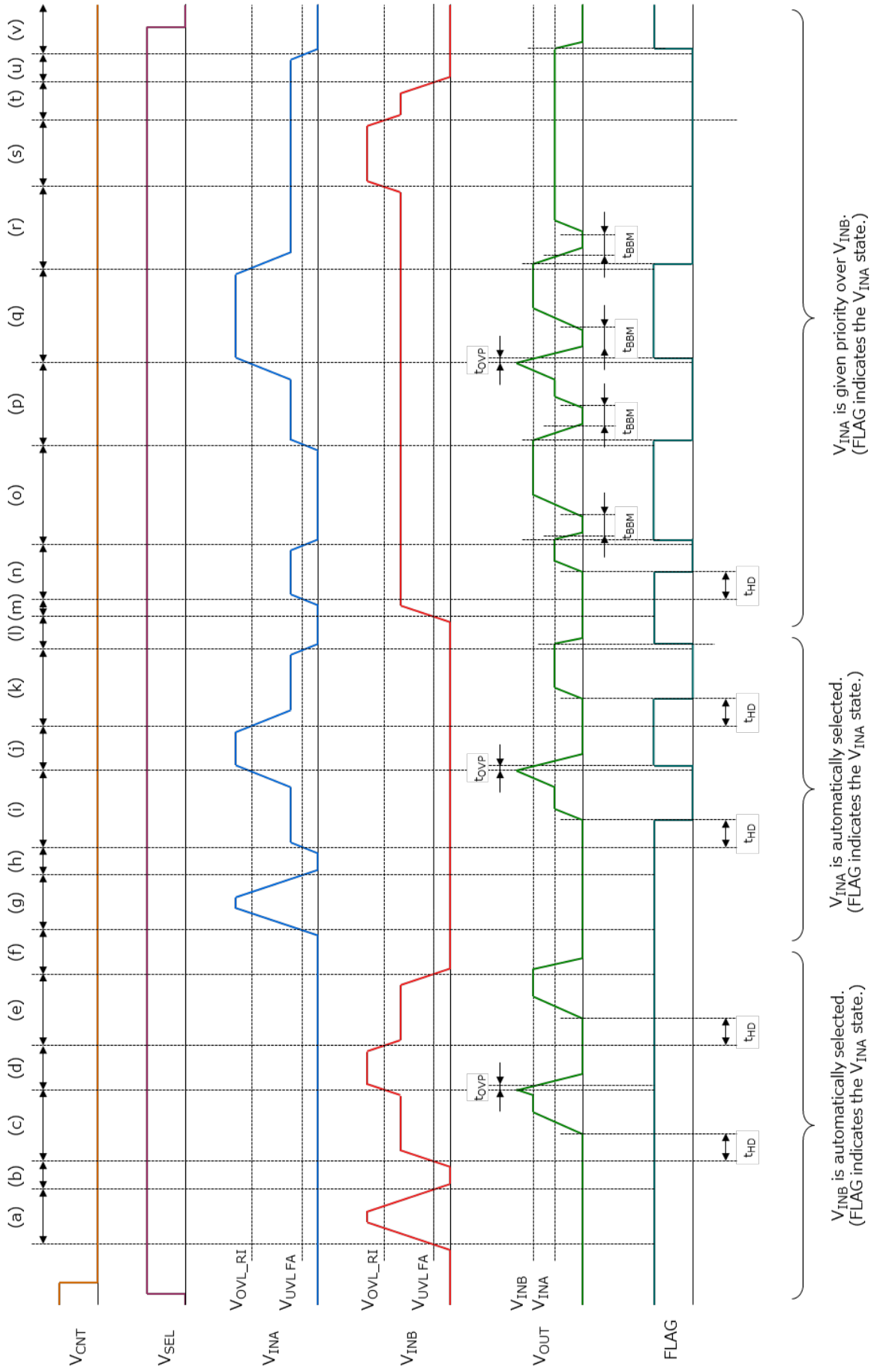

Figure 6.2 Timing diagram of the TCK321G and TCK322G in Auto Selection mode

Table 6.3 Operations of the TCK321G and TCK322G in Auto Selection mode

* V_{OUT} turns on after hold time (t_{HD}).
** V_{OUT} turns on after break-before-make time (t_{BBM}).

Period	V_{CNT}	V_{SEL}	V_{INA}	V_{INB}	V_{OUT}		FLAG	
					V_{OUT} output	Input voltage selected	FLAG output	Input state indicated
(a)	L	H	L	H	Off	–	Hz	–
(b)	L	H	L	L	Off	–	Hz	–
(c)	L	H	L	M	On(*)	V_{INB}	Hz	–
(d)	L	H	L	H	Off	–	Hz	–
(e)	L	H	L	M	On(*)	V_{INB}	Hz	–
(f)	L	H	L	L	Off	–	Hz	–
(g)	L	H	H	L	Off	–	Hz	–
(h)	L	H	L	L	Off	–	Hz	–
(i)	L	H	M	L	On(*)	V_{INA}	Hz → Low	V_{INA}
(j)	L	H	H	L	Off	–	Low → Hz	V_{INA}
(k)	L	H	M	L	On(*)	V_{INA}	Hz → Low	V_{INA}
(l)	L	H	L	L	Off	–	Low → Hz	V_{INA}
(m)	L	H	L	M	Off	–	Hz	–
(n)	L	H	M	M	On(*)	V_{INA}	Hz→ Low	V_{INA}
(o)	L	H	L	M	On(**)	V_{INB}	Low → Hz	V_{INA}
(p)	L	H	M	M	On(**)	V_{INA}	Hz → Low	V_{INA}
(q)	L	H	H	M	On(**)	V_{INB}	Low → Hz	V_{INA}
(r)	L	H	M	M	On(**)	V_{INA}	Hz → Low	V_{INA}
(s)	L	H	M	H	On	V_{INA}	Low	V_{INA}
(t)	L	H	M	M	On	V_{INA}	Low	V_{INA}
(u)	L	H	M	L	On	V_{INA}	Low	V_{INA}
(v)	L	H → L	L	L	Off	–	Low → Hz	V_{INA}

M: In the normal voltage range
Hz: High impedance
H: In the overvoltage lockout range
L: In the undervoltage lockout range

6.2.2. Timing chart of the TCK323G in Auto Selection mode

In the case of the TCK323G, the FLAG output indicates the V_{INB} state in Auto Selection mode regardless of the V_{INA} state. The FLAG output remains Low while V_{INB} is in the normal voltage range, and is driven High when the overvoltage or undervoltage lockout circuit is tripped. See Section 7.1 for a description of its hold time (t_{HD}).

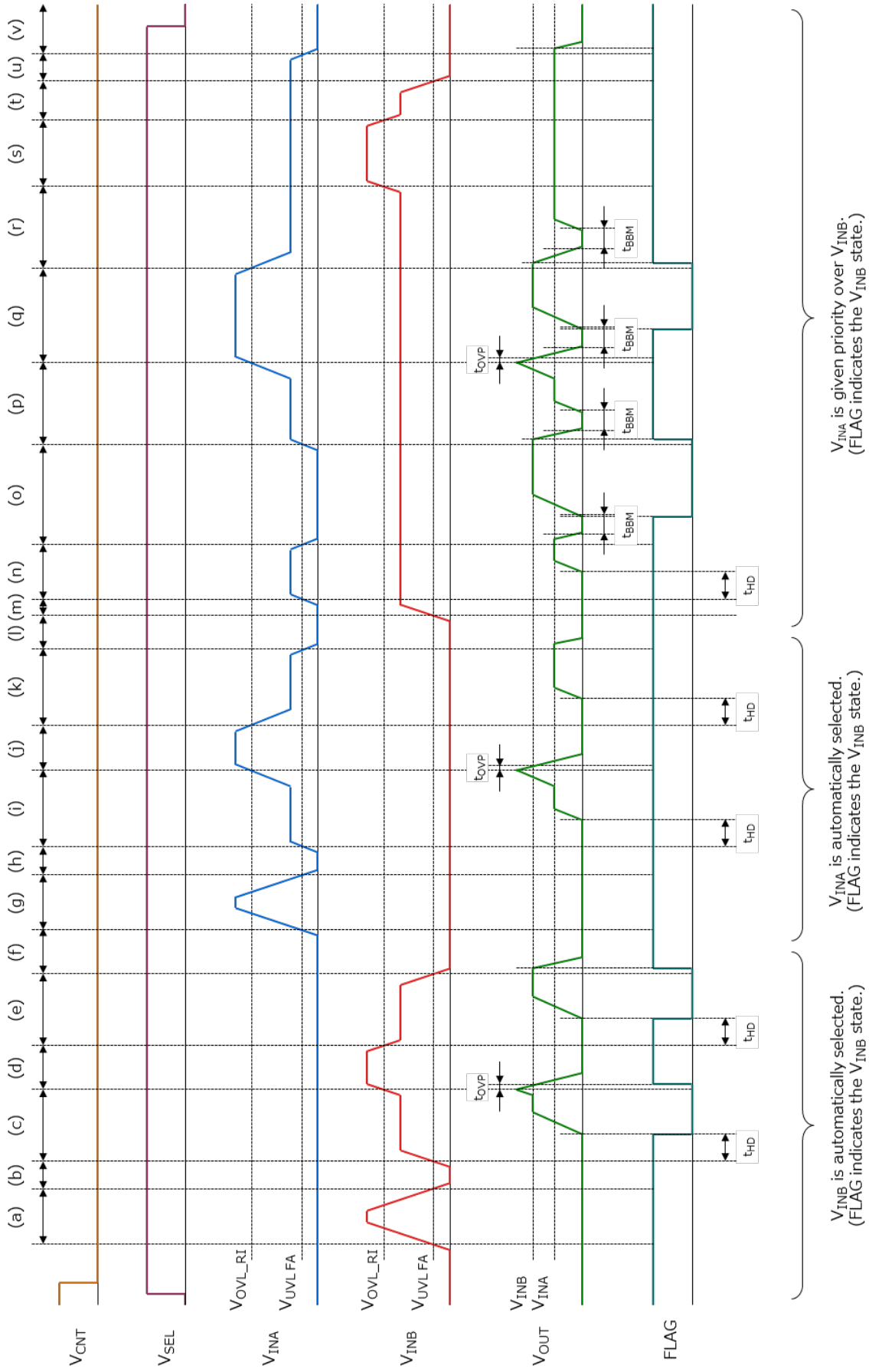

Figure 6.3 Timing diagram of the TCK323G in Auto Selection mode

Table 6.4 Operations of the TCK323G in Auto Selection mode

* V_{OUT} turns on after hold time (t_{HD}).
** V_{OUT} turns on after break-before-make time (t_{BBM}).

Period	V_{CNT}	V_{SEL}	V_{INA}	V_{INB}	V_{OUT}		FLAG	
					V_{OUT} output	Input voltage selected	FLAG output	Input state indicated
(a)	L	H	L	H	Off	–	Hz	–
(b)	L	H	L	L	Off	–	Hz	–
(c)	L	H	L	M	On(*)	V_{INB}	Hz → Low	V_{INB}
(d)	L	H	L	H	Off	–	Hz	–
(e)	L	H	L	M	On(*)	V_{INB}	Hz → Low	V_{INB}
(f)	L	H	L	L	Off	–	Hz	–
(g)	L	H	H	L	Off	–	Hz	–
(h)	L	H	L	L	Off	–	Hz	–
(i)	L	H	M	L	On(*)	V_{INA}	Hz	–
(j)	L	H	H	L	Off	–	Hz	–
(k)	L	H	M	L	On(*)	V_{INA}	Hz	–
(l)	L	H	L	L	Off	–	Hz	–
(m)	L	H	L	M	Off	–	Hz	–
(n)	L	H	M	M	On(*)	V_{INA}	Hz	–
(o)	L	H	L	M	On(**)	V_{INB}	Hz → Low	V_{INB}
(p)	L	H	M	M	On(**)	V_{INA}	Hz	–
(q)	L	H	H	M	On(**)	V_{INB}	Hz → Low	
(r)	L	H	M	M	On(**)	V_{INA}	Low → Hz	V_{INB}
(s)	L	H	M	H	On	V_{INA}	Hz	–
(t)	L	H	M	M	On	V_{INA}	Hz	–
(u)	L	H	M	L	On	V_{INA}	Hz	–
(v)	L	H → L	L	L	Off	–	Hz	–

M: In the normal voltage range
Hz: High impedance
H: In the overvoltage lockout range
L: In the undervoltage lockout range

6.3. Manual Selection mode

The TCK321G, TCK322G, and TCK323G operate identically in Manual Selection mode. In this mode, either V_{INA} or V_{INB} can be selectively forwarded to the V_{OUT} outputs via a control signal applied to the V_{SEL} pin. V_{INA} is selected when the Mode Control signal (V_{CNT}) is High, the Input Selector signal (V_{SEL}) is High, and both V_{INA} and V_{INB} are in the normal range. V_{INB} is selected when the Mode Control signal (V_{CNT}) is High and the Input Selector signal (V_{SEL}) is Low. When both V_{CNT} and V_{SEL} are Low, the TCK321G, TCK322G, and TCK323G are disabled, turning off the V_{OUT} outputs. When overvoltage or undervoltage lockout protection is tripped because of an abnormal V_{INA} or V_{INB} condition, the FLAG output is driven Low to indicate it externally. See Section 7.1 for a description of its hold time (t_{HD}).

Table 6.5 Operations of the TCK321G, TCK322G, and TCK323G in Manual Selection mode

When V_{CNT} is High, V_{SEL} is High, and V_{INA} is active

Input voltage		V_{INA}: In the operating voltage range V_{INB}: In the operating voltage range	V_{INA}: In the operating voltage range V_{INB}: Outside the operating voltage range	V_{INA}: Outside the operating voltage range V_{INB}: In the operating voltage range	V_{INA}: Outside the operating voltage range V_{INB}: Outside the operating voltage range
Output voltage		On (V_{OUT}=V_{INA})	On (V_{OUT}=V_{INA})	Off (Disabled)	Off (Disabled)
FLAG output	TCK321G	Off (High-Z)	On (Low)	On (Low)	On (Low)
	TCK322G	Off (High-Z)	On (Low)	On (Low)	On (Low)
	TCK323G	Off (High-Z)	On (Low)	On (Low)	On (Low)
Reverse current blocking		V_{INA}: Invalid V_{INB}: Valid	V_{INA}: Invalid V_{INB}: Valid	V_{INA}: Valid V_{INB}: Valid	V_{INA}: Valid V_{INB}: Valid

In the operating voltage range: $V_{ULV\_RI}<V_{IN*}<V_{OVL\_RI}$

Outside the operating voltage range: $V_{UVL\_FA}>V_{IN*}$ or $V_{IN*}>V_{OVL\_RI}$

When V_{CNT} is High, V_{SEL} is Low, and V_{INB} is active

Input voltage		V_{INA}: In the operating voltage range V_{INB}: In the operating voltage range	V_{INA}: In the operating voltage range V_{INB}: Outside the operating voltage range	V_{INA}: Outside the operating voltage range V_{INB}: In the operating voltage range	V_{INA}: Outside the operating voltage range V_{INB}: Outside the operating voltage range
Output voltage		On (V_{OUT}=V_{INB})	Off (Disabled)	On (V_{OUT}=V_{INB})	Off (Disabled)
FLAG output	TCK321G	Off (High-Z)	On (Low)	On (Low)	On (Low)
	TCK322G	Off (High-Z)	On (Low)	On (Low)	On (Low)
	TCK323G	Off (High-Z)	On (Low)	On (Low)	On (Low)
Reverse current blocking		V_{INA}: Valid V_{INB}: Invalid	V_{INA}: Valid V_{INB}: Valid	V_{INA}: Valid V_{INB}: Invalid	V_{INA}: Valid V_{INB}: Valid

In the operating voltage range: $V_{ULV\_RI}<V_{IN*}<V_{OVL\_RI}$

Outside the operating voltage range: $V_{UVL\_FA}>V_{IN*}$ or $V_{IN*}>V_{OVL\_RI}$

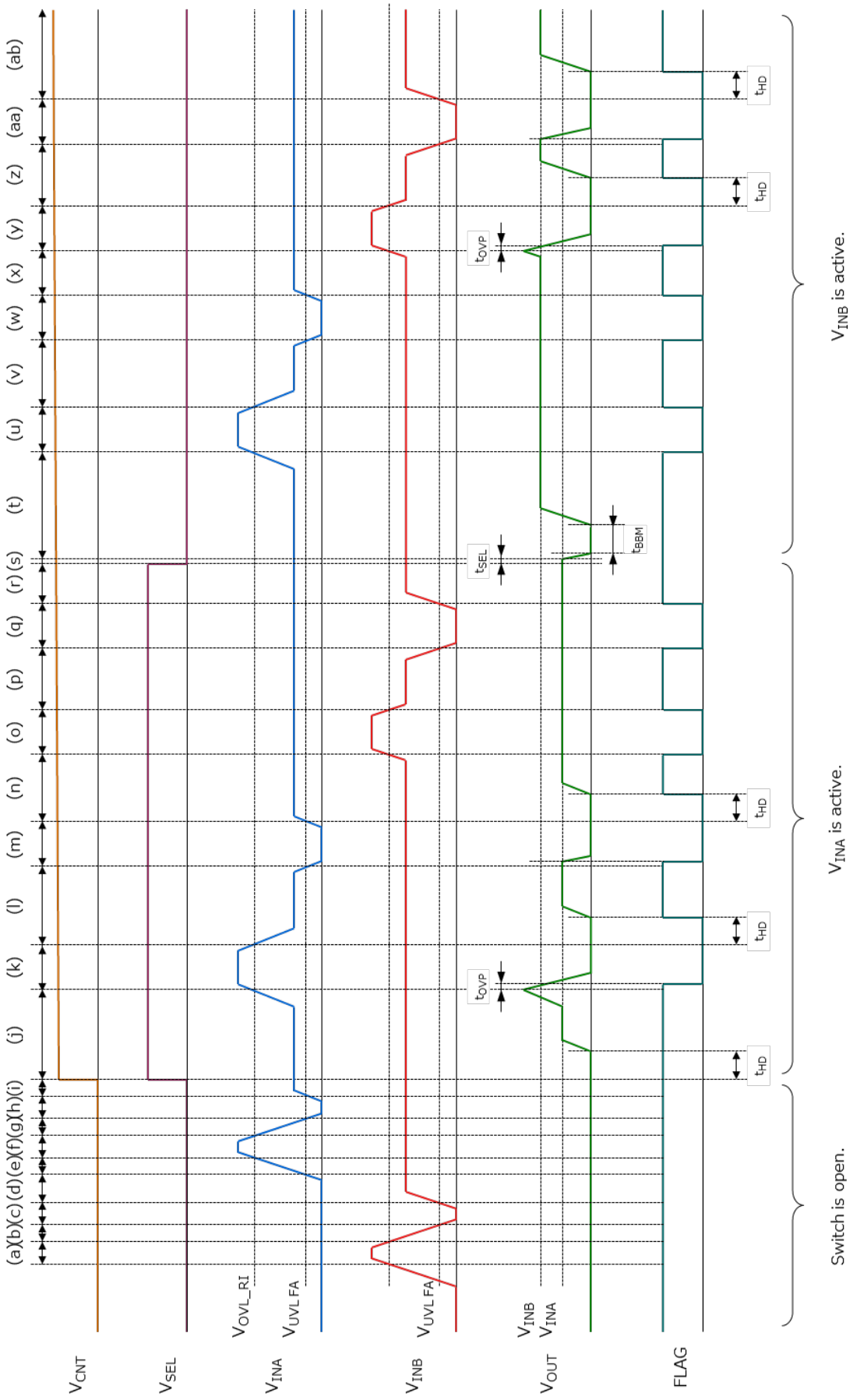

Figure 6.4 Timing diagram of the TCK321G, TCK322G, and TCK323G in Manual Selection mode

Table 6.6 Operations of the TCK321G, TCK322G, and TCK323G in Manual Selection mode

* V_{OUT} turns on after hold time (t_{HD}).
** V_{OUT} turns off after V_{IN} selection delay time (t_{SEL}).
*** V_{OUT} turns on after break-before-make time (t_{BBM}).

Period	V_{CNT}	V_{SEL}	V_{INA}	V_{INB}	V_{OUT}		FLAG	
					V_{OUT} output	Input voltage selected	FLAG output	Input state indicated
(a)	L	L	L	H	Off	–	Hz	–
(b)	L	L	L	M	Off	–	Hz	–
(c)	L	L	L	L	Off	–	Hz	–
(d)	L	L	L	M	Off	–	Hz	–
(e)	L	L	M	M	Off	–	Hz	–
(f)	L	L	H	M	Off	–	Hz	–
(g)	L	L	M	M	Off	–	Hz	–
(h)	L	L	L	M	Off	–	Hz	–
(i)	L	L	M	M	Off	–	Hz	–
(j)	H	H	M	M	On(*)	V_{INA}	Hz	–
(k)	H	H	H	M	Off	–	Hz → Low	–
(l)	H	H	M	M	On(*)	V_{INA}	Low → Hz	–
(m)	H	H	L	M	Off	–	Hz → Low	–
(n)	H	H	M	M	On(*)	V_{INA}	Low → Hz	–
(o)	H	H	M	H	On	V_{INA}	Low	–
(p)	H	H	M	M	On	V_{INA}	Hz	–
(q)	H	H	M	L	On	V_{INA}	Low	–
(r)	H	H	M	M	On	V_{INA}	Hz	–
(s)	H	L	M	M	Off(**)	–	Hz	–
(t)	H	L	M	M	On(***)	V_{INB}	Hz	–
(u)	H	L	H	M	On	V_{INB}	Low	–
(v)	H	L	M	M	On	V_{INB}	Hz	–
(w)	H	L	L	M	On	V_{INB}	Low	–
(x)	H	L	M	M	On	V_{INB}	Hz	–
(y)	H	L	M	H	Off	–	Low	–
(z)	H	L	M	M	On(*)	V_{INB}	Low → Hz	–
(aa)	H	L	M	L	Off	–	Hz → Low	–
(ab)	H	L	M	M	On(*)	V_{INB}	Low → Hz	–

M : In the normal voltage range
Hz : High impedance
H : In the overvoltage lockout range
L : In the undervoltage lockout range

7. Definitions of the AC characteristics of the TCK32*G

7.1. Hold time (t_{HD})

The hold time (t_{HD}) is a delay time that is inserted to prevent a malfunction due to chatter caused by the application of input voltage until the output is enabled. When the TCK32*G detects a voltage between the undervoltage and overvoltage lockout thresholds, the V_{OUT} outputs are enabled after a predefined delay time (15 ms typical). This function makes it possible to set the output rise time independent of the input voltage.

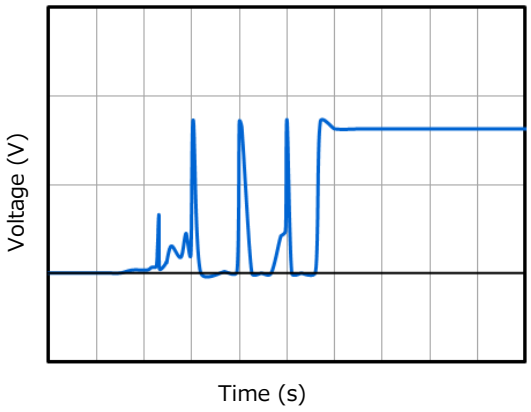

Figure 7.1 Example of a chattering waveform

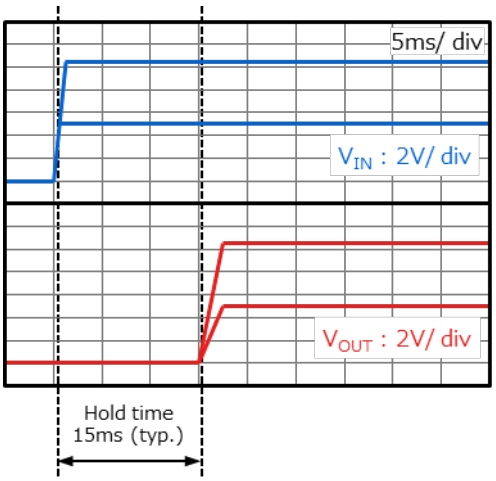

Figure 7.2 Hold time

7.2. V_{IN} selection delay time (t_{SEL})

The V_{IN} selection delay time is defined between the time from a time V_{SEL} input pin toggles to a time the output voltage drops to 90% of V_{OUT} in Manual Selection mode as shown in Figure 7.3.

7.3. Break-before-make time (t_{BBM})

The break-before-make time is a period during the break-before-make function keeps off both the MOSFETs connected to the V_{INA} and V_{INB} inputs when the TCK32*G switches between these inputs. The break-before-make time is defined as the time from 10% of V_{OUT} of the falling output to 10% of V_{OUT} of the rising output.

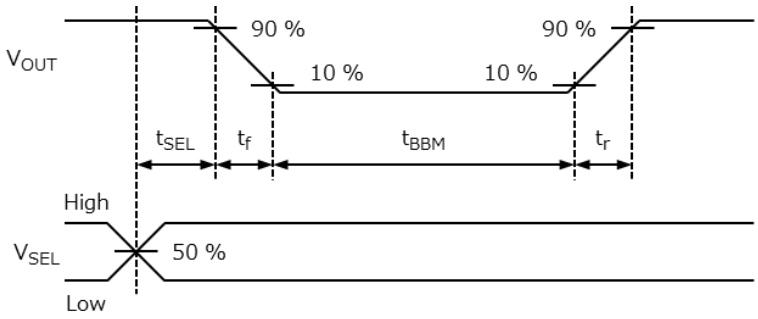

Figure 7.3 Definitions of V_{IN} selection time (t_{SEL}) and break-before-make time (t_{BBM})

7.4. V_{OUT} OVP off-time (t_{OVP})

The V_{OUT} OVP off-time (t_{OVP}) is defined as a delay time from when the input voltage (V_{IN*}) exceeds the overvoltage lockout (V_{OVLO_RI}) rising threshold to when the output voltage drops to 80% of V_{OVLO_RI}.

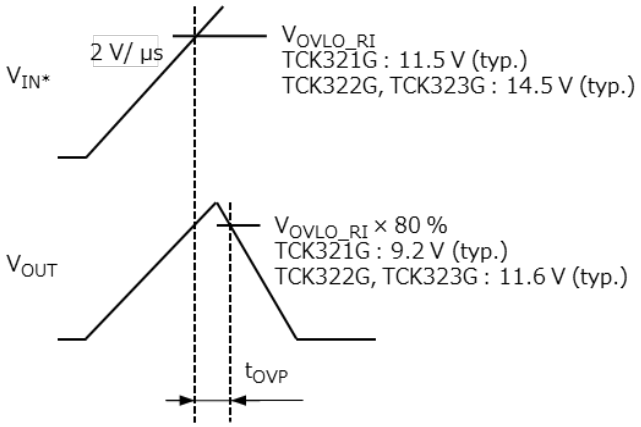

Figure 7.4 Definition of V_{OUT} OVP off-time (t_{OVP})

7.5. V_{OUT} off-time (CNT) (t_{OFF})

The V_{OUT} off-time (t_{OFF}) is defined as the time required from when the control voltage is 50% of V_{CNT} to when the output voltage drops to 80% of V_{OUT}.

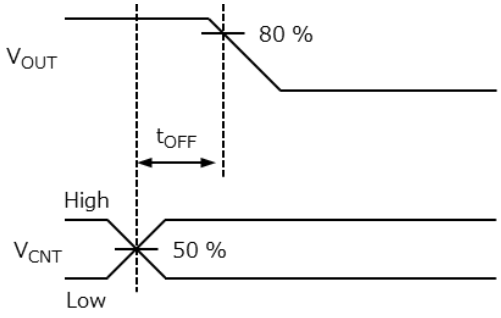

Figure 7.5 Definition of V_{OUT} off-time (t_{OFF})

7.6. V_{OUT} rise time (t_r) and V_{OUT} fall time (t_f)

The V_{OUT} rise time (t_r) is the time required for the output voltage to change from 10% to 90% of V_{OUT}. The V_{OUT} fall time (t_f) is the time required for the output voltage to change from 90% to 10% of V_{OUT}.

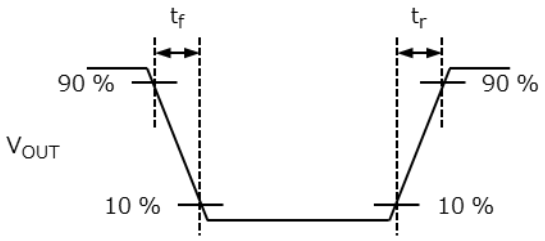

Figure 7.6 Definitions of V_{OUT} rise time (t_r) and V_{OUT} fall time (t_f)

8. Calculating the power dissipation and junction temperature of an IC

The power dissipation (P_D) of an IC can be calculated by Equation 8-1. The term $V_{IN} \times I_Q$ is negligible when it is much smaller than the term $I_{OUT}^2 \times R_{on}$.

1) When $V_{INA} = V_{INB}$ in Manual Selection mode:

$$P = {I_{OUT}}^2 \times R_{ON} + (V_{INA} + V_{INB}) \times I_{Q(ON)} \quad (\mathrm{W}) \qquad (8\text{-}1)$$

I_{OUT}:	Output current	(A)
R_{ON}:	On-resistance	(Ω)
V_{INA}, V_{INB}:	Input voltage	(V)
$I_{ON:}$	On-state quiescent current	(A)

2) When $V_{INA} \neq V_{INB}$ in Auto Selection mode

$$P = {I_{OUT}}^2 \times R_{ON} + I_{Q(ON\_VINA)} \times V_{INA} + I_{Q(ON\_VINB)} \times V_{INB} \quad (\mathrm{W}) \qquad (8\text{-}2)$$

I_{OUT}:	Output current	(A)
R_{ON}:	On-resistance	(Ω)
V_{INA}, V_{INB}:	Input voltage	(V)
$I_{Q(ON\_VINA)}$:	Quiescent current of V_{INA} in the on state	(A)
$I_{Q(ON\_VINB)}$:	Quiescent current of V_{INB} in the on state	(A)

The junction temperature (T_j) can be calculated by Equation 8-3.

$$T_j = P \times R_{th(j-a)} + Ta$$
$$= P \times \frac{T_{j(\max)} - 25\ °C}{P_D} + Ta$$
$$= P \times \frac{150\ °C - 25\ °C}{P_D} + Ta \quad (°C) \qquad (8\text{-}3)$$

P:	IC power dissipation	(W)
P_D:	Power dissipation of the TCK32*G when it is mounted on a board of the size specified in a datasheet	(W)
R_{th}:	Thermal resistance	(°C/W)
T_j:	Junction temperature	(°C)
T_a:	Ambient temperature	(°C)

The permissible power dissipation of the TCK32*G is specified as an absolute maximum rating when it is mounted on a board. Design PCB traces in such a manner as to allow a sufficient margin relative to the expected maximum power dissipation during operation. The maximum power dissipation should be adequately derated according to the ambient temperature, input voltage, output current, and other conditions of an actual application.

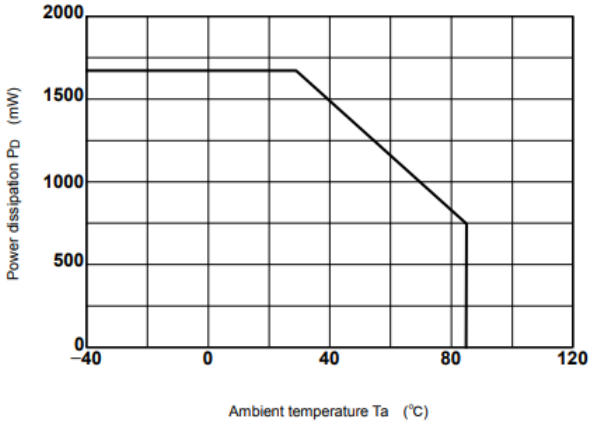

Figure 8.1 Power dissipation (P_D) vs. ambient temperature (T_a)

Board conditions

Material:	Glass epoxy (FR4)
Size:	40 mm × 40 mm (four Cu layers)

9. Usage considerations

9.1. External capacitors

Connect external input and output capacitors to achieve the guaranteed performance and improve the stability of a power supply. Connect capacitors of at least 1.0 μF as close as possible to the input and output pins. The withstand voltage of these capacitors should be sufficiently higher than their operating voltage.

9.2. Board assembly

In order to further stabilize output voltage, add an output capacitor as close as possible to the TCK32*G and provide V_{IN} and GND traces as large as possible to reduce trace impedance.

9.3. Protection circuits

The reverse current blocking, thermal shutdown, overvoltage lockout, and undervoltage lockout circuits incorporated in the TCK321G, TCK322G, and TCK323G are not intended to guarantee that they always remain below their absolute maximum ratings. Apply the above design considerations and derate the absolute maximum rated values as described in the Toshiba Semiconductor Reliability Handbook to ensure that none of the absolute maximum ratings will be exceeded under any circumstances. It is recommended to add fail-safe and other safety features to an application system.

9.4. Power dissipation

Design PCB traces in such a manner that the IC temperature remains well below the maximum rated temperature during operation even at the maximum power dissipation point. For PCB trace design, input voltage, output current, ambient temperature, and other environmental conditions should also be considered.

10. Conclusion

This application note has discussed the basics of 2-to-1 power multiplexer ICs such as electrical characteristics and protection features shown in the datasheet. The 2-to-1 power multiplexer ICs are very effective for the power management of smartphones, tablets, wearable devices, and other mobile devices having two charging ports. Toshiba provides a wide range of 2-to-1 power multiplexer ICs, including low-on-resistance power multiplexer ICs that help reduce power loss and incorporate various protection features. We hope that you have found this application note useful in considering the use of Toshiba's 2-to-1 power multiplexer ICs.

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