

TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S103F

Single Operational Amplifier

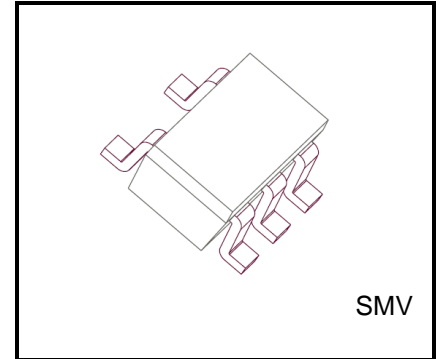
Low supply current

Features

- Input, Output Full Range type (Rail to Rail)
- Low supply current 100 μ A (Typ.) @ $V_{DD}=1.8V$
- Low Input offset voltage 1.5mV (Max) @ $V_{DD}=1.8V$
- Wide Operating Voltage Range 1.8V to 5.5V

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{DD} - V_{SS}$	6	V
Differential input voltage	DV_{IN}	± 6	V
Input voltage	V_{IN}	V_{DD} to V_{SS}	V
Output voltage	V_{OUT}	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V \leq V_{SS} + 6V$	V
Output current	I_{OUT}	± 25	mA
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	-40 to 105	°C
Storage temperature	T_{stg}	-55 to 150	°C



Weight:
SMV (SOT-25)(SC-74A) :14 mg (typ.)

Note1: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ratings (Ta = -40 to 105°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{DD} - V_{SS}$	1.8 to 5.5	V

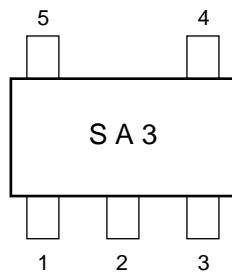
Note2: A higher load capacitance will increase the risk of voltage oscillation. Allow sufficient capacitance value when designing your circuit and using this product to prevent voltage oscillation.

Note3: This device is sensitive to electrostatic discharge.

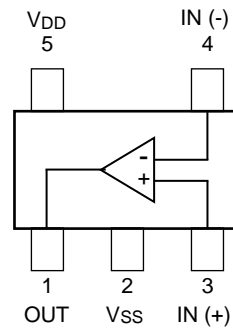
Please ensure equipment, operator and tools are adequately earthed when handling.

Start of commercial production
2020-09

Marking (top view)



Pin Assignment (top view)



Electrical Characteristics

DC Characteristics ($V_{DD} = 1.8V$, $V_{SS} = GND$, $T_a = 25^\circ C$, $V_{IN} = V_{DD}/2$, unless otherwise noted.)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$ $T_a = -40\text{ to }105^\circ C$	-1.85	0.3	1.85	mV
			$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$ $T_a = 25^\circ C$	-1.5	0.3	1.5	mV
Input offset voltage drift	$V_{IO\text{drift}}$	1	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	-	1	-	$\mu V/^\circ C$
Input offset current	I_{IO}	2	-	-	1	-	pA
Input bias current	I_I	2	-	-	1	-	pA
Common mode input voltage	CMV_{IN}	3	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	0	-	V_{DD}	V
Voltage gain (open loop)	G_V	-	-	85	100	-	dB
Maximum output voltage	V_{OH}	4	$R_L \geq 100\text{ k}\Omega$	1.7	-	-	V
	V_{OL}	5	$R_L \geq 100\text{ k}\Omega$	-	-	0.1	
Common mode input signal rejection ratio	$CMRR$	3	$V_{IN} = 0\text{ to }1.8V$	60	80	-	dB
Supply voltage rejection ratio	$SVRR$	1	$V_{DD} = 1.8\text{ to }5.0V$	70	85	-	dB
Supply current	I_{DD}	6	-	-	100	165	μA
Source current	I_{source}	7	-	1.2	2	-	mA
Sink current	I_{sink}	8	-	1	2	-	mA

AC Characteristics ($V_{DD} = 0.9\text{ V}$, $V_{SS} = -0.9\text{ V}$, $T_a = 25^\circ C$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Unity Gain Cross Frequency	f_T	-	-	-	0.3	-	MHz
Phase margin	Φ_m	-	-	-	40	-	degrees
Slew Rate	SR	-	-	-	0.52	-	$V/\mu s$

DC Characteristics ($V_{DD} = 3.3V$, $V_{SS} = GND$, $T_a = 25^\circ C$, $V_{IN} = V_{DD}/2$, unless otherwise noted.)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$ $T_a = -40\text{ to }105^\circ C$	-2.15	0.4	2.15	mV
			$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$ $T_a = 25^\circ C$	-1.85	0.4	1.85	mV
Input offset voltage drift	$V_{IO\text{drift}}$	1	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	-	2	-	$\mu V/^\circ C$
Input offset current	I_{IO}	2	-	-	1	-	pA
Input bias current	I_I	2	-	-	1	-	pA
Common mode input voltage	CMV_{IN}	3	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	0	-	V_{DD}	V
Voltage gain (open loop)	G_V	-	-	100	125	-	dB
Maximum output voltage	V_{OH}	4	$R_L \geq 100\text{ k}\Omega$	3.2	-	-	V
	V_{OL}	5	$R_L \geq 100\text{ k}\Omega$	-	-	0.1	
Common mode input signal rejection ratio	$CMRR$	3	$V_{IN} = 0\text{ to }3.3V$	65	90	-	dB
Supply current	I_{DD}	6	-	-	100	165	μA
Source current	I_{source}	7	-	6	10	-	mA
Sink current	I_{sink}	8	-	6	10	-	mA

AC Characteristics ($V_{DD} = 1.65\text{ V}$, $V_{SS} = -1.65\text{ V}$, $T_a = 25^\circ C$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Unity Gain Cross Frequency	f_T	-	-	-	0.36	-	MHz
Phase margin	Φ_m	-	-	-	60	-	degrees
Slew Rate	SR	-	-	-	0.4	-	$V/\mu s$

DC Characteristics ($V_{DD} = 5.0V$, $V_{SS} = GND$, $T_a = 25^\circ C$, $V_{IN} = V_{DD}/2$, unless otherwise noted.)

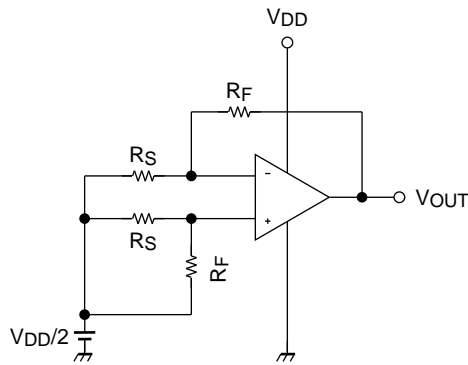
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$ $T_a = -40\text{ to }105^\circ C$	-2.15	0.4	2.15	mV
			$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$ $T_a = 25^\circ C$	-1.85	0.4	1.85	mV
Input offset voltage drift	$V_{IO\text{drift}}$	1	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	-	2	-	$\mu V/^\circ C$
Input offset current	I_{IO}	2	-	-	1	-	pA
Input bias current	I_I	2	-	-	1	-	pA
Common mode input voltage	CMV_{IN}	3	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	0	-	V_{DD}	V
Voltage gain (open loop)	G_V	-	-	100	125	-	dB
Maximum output voltage	V_{OH}	4	$R_L \geq 100\text{ k}\Omega$	4.9	-	-	V
	V_{OL}	5	$R_L \geq 100\text{ k}\Omega$	-	-	0.1	
Common mode input signal rejection ratio	$CMRR$	3	$V_{IN} = 0\text{ to }5.0V$	68	90	-	dB
Supply current	I_{DD}	6	-	-	115	190	μA
Source current	I_{source}	7	-	17	-	-	mA
Sink current	I_{sink}	8	-	17	-	-	mA

AC Characteristics ($V_{DD} = 2.5\text{ V}$, $V_{SS} = -2.5\text{ V}$, $T_a = 25^\circ C$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Unity Gain Cross Frequency	f_T	-	-	-	0.37	-	MHz
Phase margin	Φ_m	-	-	-	60	-	degrees
Slew Rate	SR	-	-	-	0.4	-	$V/\mu s$

Test Circuit

1. SVRR, V_{IO}



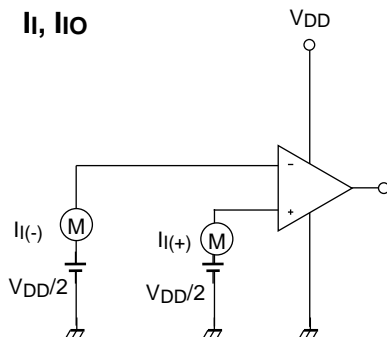
- SVRR
- For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.
When V_{DD} = 1.8 V, V_{DD} = V_{DD1} and V_{OUT} = V_{OUT1}
When V_{DD} = 5.0 V, V_{DD} = V_{DD2} and V_{OUT} = V_{OUT2}

$$SVRR = 20 \log \left[\left| \frac{V_{DD1} - V_{DD2}}{\left\{ V_{OUT1} - \left(\frac{V_{DD1}}{2} \right) \right\} - \left\{ V_{OUT2} - \left(\frac{V_{DD2}}{2} \right) \right\}} \right| \times \frac{R_F + R_S}{R_S} \right]$$

- V_{IO}
Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

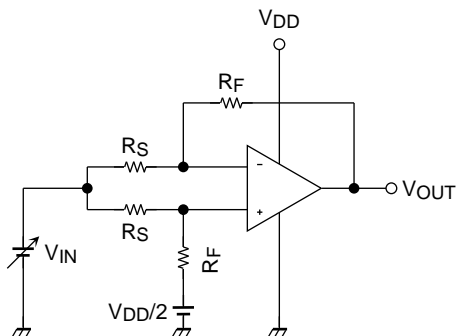
$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. I_I, I_{IO}



- I_I = (|I_{I(-)}| + |I_{I(+)}|) / 2
- I_{IO} = |I_{I(-)}| - |I_{I(+)}|

3. CMRR, CMV_{IN}

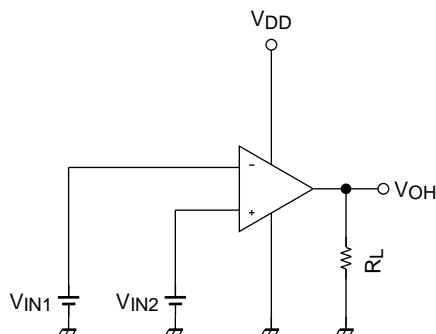


- CMRR
Measure the V_{OUT} value, as indicated below, and calculate the value of the CMRR using the equation shown.
When V_{IN} = 0 V, V_{IN} = V_{IN1} and V_{OUT} = V_{OUT1}
When V_{IN} = 3.3 V, V_{IN} = V_{IN2} and V_{OUT} = V_{OUT2}

$$CMRR = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

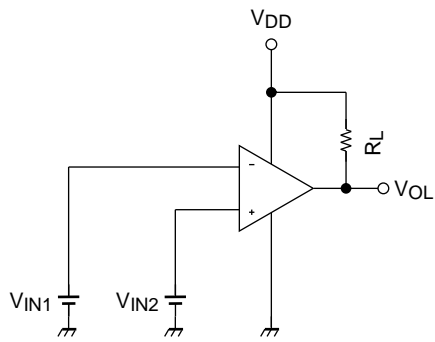
- CMV_{IN}
Input range within which the CMRR specification guarantees V_{OUT} value (as varied by the V_{IN} value).

4. V_{OH}



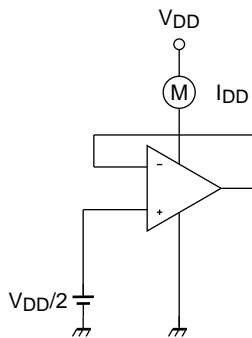
- V_{OH}
 $V_{IN1} = \frac{V_{DD}}{2} - 0.05V$
 $V_{IN2} = \frac{V_{DD}}{2} + 0.05V$

5. VOL

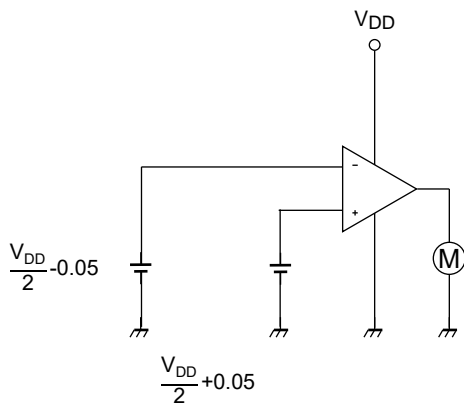


- VOL
- $V_{IN1} = \frac{V_{DD}}{2} + 0.05V$
- $V_{IN2} = \frac{V_{DD}}{2} - 0.05V$

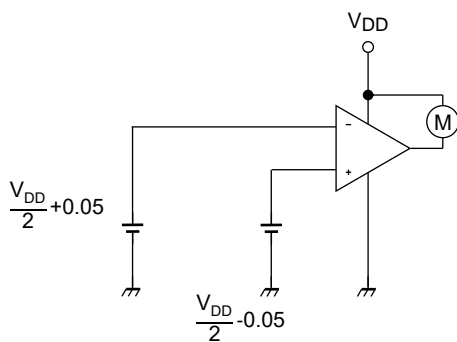
6. IDD



7. Isource



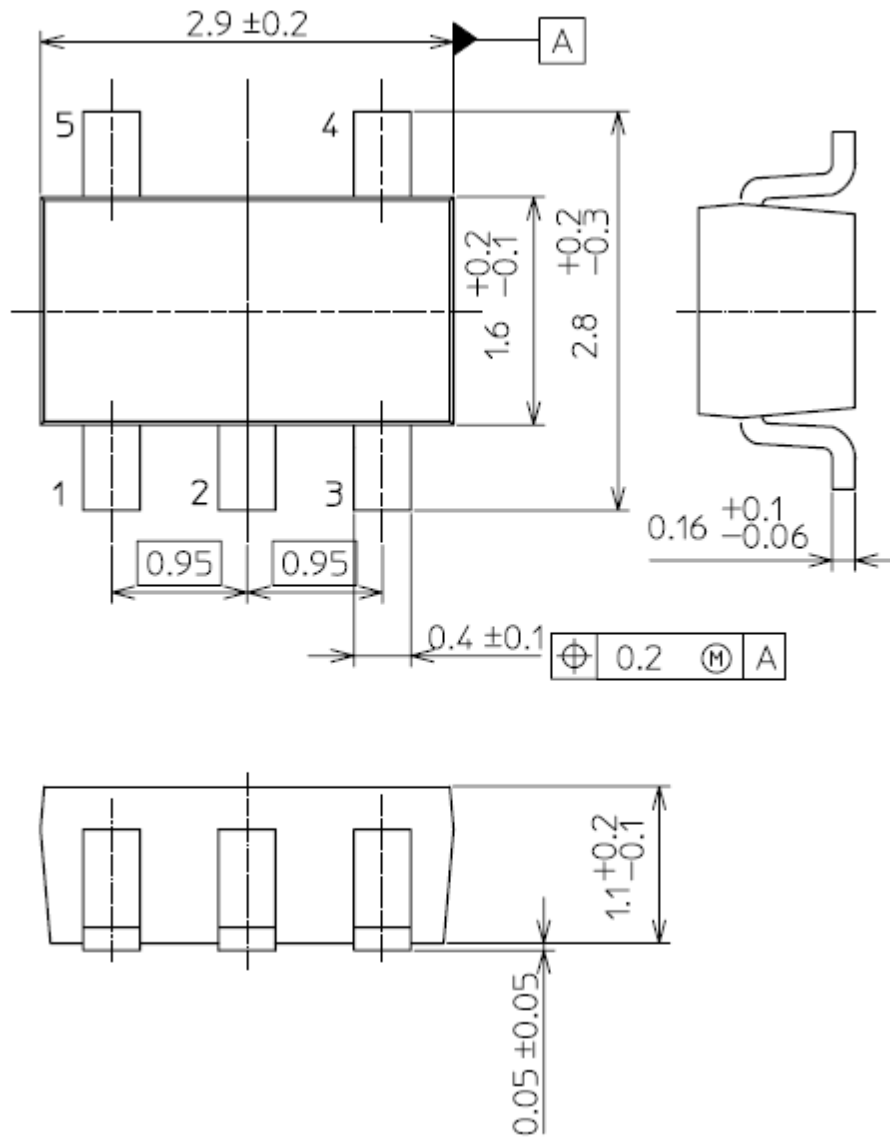
8. Isink



Package Dimensions

SMV (SOT-25)(SC-74A)

Unit: mm



Weight : 14 mg (typ.)

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