

MOSFETs Silicon Carbide N-Channel MOS

TW070J120B

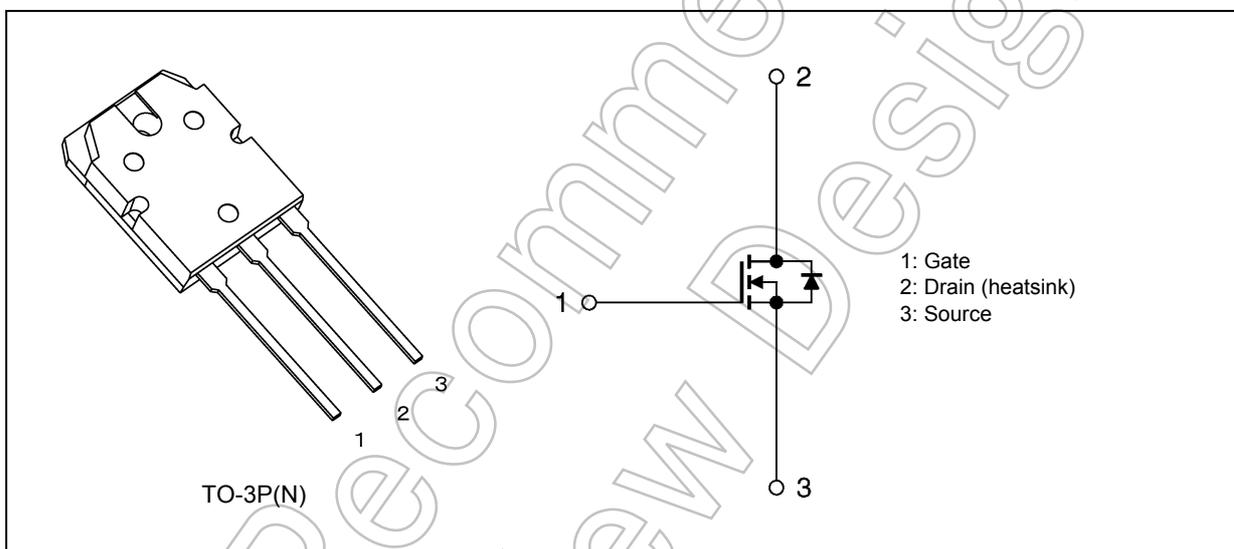
1. Applications

- Switching Voltage Regulators

2. Features

- (1) Chip design of 2nd generation (Built-in SiC schottky barrier diode)
- (2) Low diode forward voltage: $V_{DSF} = -1.35$ V (typ.)
- (3) High voltage: $V_{DSS} = 1200$ V
- (4) Low drain-source on-resistance: $R_{DS(ON)} = 70$ m Ω (typ.)
- (5) Less susceptible to malfunction due to high threshold voltage: $V_{th} = 4.2$ to 5.8 V ($V_{DS} = 10$ V, $I_D = 20$ mA)
- (6) Enhancement mode.

3. Packaging and Internal Circuit



Start of commercial production

2020-08

4. Absolute Maximum Ratings (Note) ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	1200	V
Gate-source voltage	V_{GSS}	+25/-10	
Drain current (DC) ($T_c = 25\text{ }^\circ\text{C}$) (Note 1)	I_D	36.0	A
Drain current (DC) ($T_c = 100\text{ }^\circ\text{C}$) (Note 1)	I_D	25.5	
Drain current (pulsed) (Note 1)	I_{DP}	72	
Power dissipation ($T_c = 25\text{ }^\circ\text{C}$)	P_D	272	W
Channel temperature	T_{ch}	175	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 175	
Mounting torque	TOR	0.8	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	0.55	$^\circ\text{C}/\text{W}$
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	50	

Note 1: Ensure that the channel temperature does not exceed $175\text{ }^\circ\text{C}$.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care. It should be used for switching applications.

Not Recommended for New Design

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = +25/-10\text{ V}$, $V_{DS} = 0\text{ V}$	—	—	± 0.5	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 1200\text{ V}$, $V_{GS} = 0\text{ V}$	—	0.2	10	
		$T_a = 175\text{ }^\circ\text{C}$, $V_{DS} = 1200\text{ V}$, $V_{GS} = 0\text{ V}$	—	3.0	—	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	1200	—	—	V
Gate threshold voltage (Note 2)	V_{th}	$V_{DS} = 10\text{ V}$, $I_D = 20\text{ mA}$	4.2	—	5.8	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 20\text{ V}$, $I_D = 18\text{ A}$	—	70	90	$\text{m}\Omega$
		$T_a = 150\text{ }^\circ\text{C}$, $V_{GS} = 20\text{ V}$, $I_D = 18\text{ A}$	—	87	—	

Note 2: Please be sure to I_{GSS} ($V_{GS} = 25\text{ V}$) test before the V_{th} test.

6.2. Dynamic Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{ISS}	$V_{DS} = 800\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 100\text{ kHz}$	—	1680	—	pF
Reverse transfer capacitance	C_{RSS}		—	8	—	
Output capacitance	C_{OSS}		—	109	—	
C_{OSS} stored energy	E_{OSS}		—	42	—	μJ
Gate resistance	r_g	$V_{DS} = \text{OPEN}$, $f = 100\text{ kHz}$	—	3.5	—	Ω
Turn-on delay time	$t_{d(on)}$	See Fig. 6.5.1	—	17	—	ns
Switching time (rise time)	t_r	See Fig. 6.5.2	—	7	—	
Turn-off delay time	$t_{d(off)}$		—	40	—	
Switching time (fall time)	t_f		—	35	—	
Turn-on switching loss	E_{on}		—	0.380	—	mJ
Turn-off switching loss	E_{off}		—	0.035	—	

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} = 800\text{ V}$, $V_{GS} = 20\text{ V}$, $I_D = 18\text{ A}$	—	67	—	nC
Gate-source charge 1	Q_{gs1}		—	13	—	
Gate-drain charge	Q_{gd}		—	25	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward current (DC) (Note 3)	I_F	$T_c = 25\text{ }^\circ\text{C}$	—	—	36	A
		$T_c = 100\text{ }^\circ\text{C}$	—	—	29.6	
Diode forward current (pulsed) (Note 3)	I_{FP}	$T_c = 25\text{ }^\circ\text{C}$	—	—	72	
		$T_c = 100\text{ }^\circ\text{C}$	—	—	32	
Diode forward voltage	V_{DSF}	$I_{DR} = 10\text{ A}$, $V_{GS} = -5\text{ V}$	—	-1.35	-1.80	V
		$T_a = 150\text{ }^\circ\text{C}$, $I_{DR} = 10\text{ A}$, $V_{GS} = -5\text{ V}$	—	-1.70	—	
Reverse recovery time	t_{rr}	$I_{DR} = 10\text{ A}$, $V_{GS} = 0\text{ V}$, $V_{DD} = 800\text{ V}$, $-di_{DR}/dt = 1000\text{ A}/\mu\text{s}$	—	22	—	ns
Reverse recovery charge	Q_{rr}		—	170	—	nC
Peak reverse recovery current	I_{rr}		—	15	—	A

Note 3: Ensure that the channel temperature does not exceed $175\text{ }^\circ\text{C}$.

6.5. Test Circuit and Timing Diagram

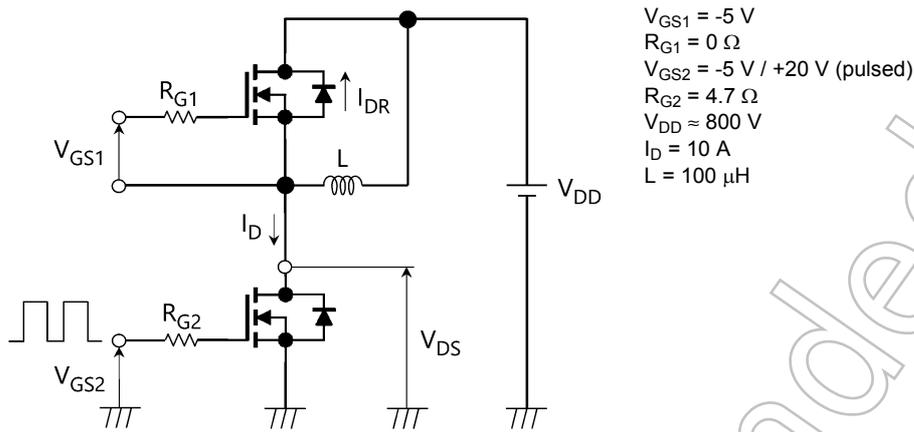


Fig. 6.5.1 Switching Time Test Circuit

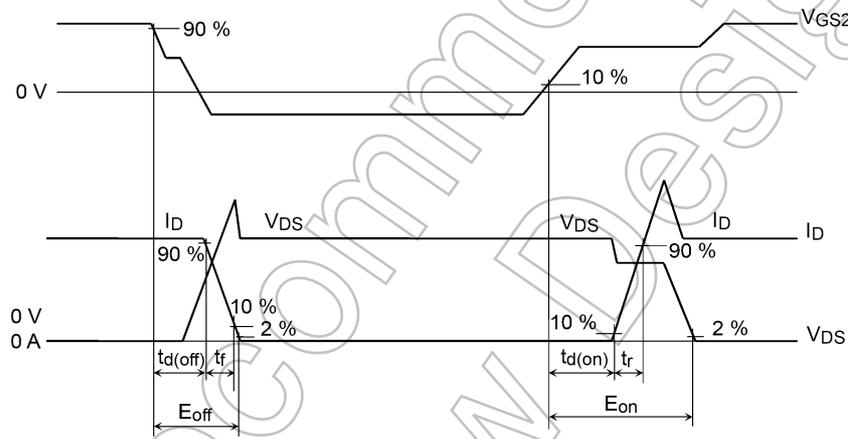


Fig. 6.5.2 Timing Diagram

7. Marking (Note)

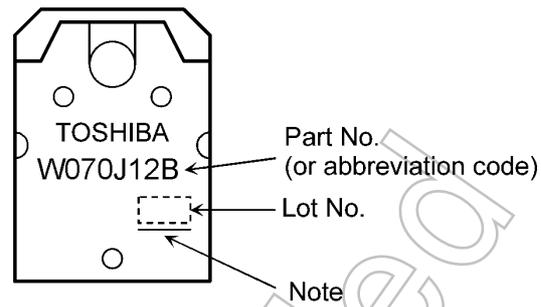


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Not Recommended for New Design

8. Characteristics Curves (Note)

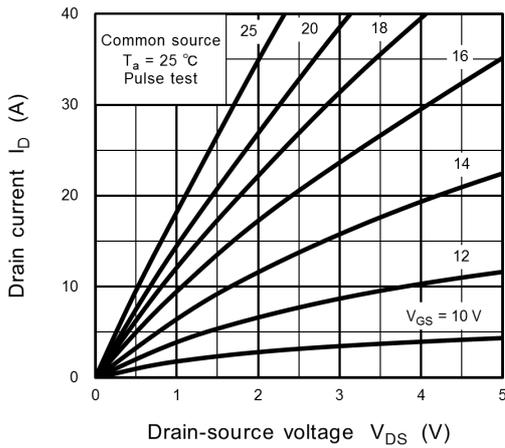


Fig. 8.1 $I_D - V_{DS}$

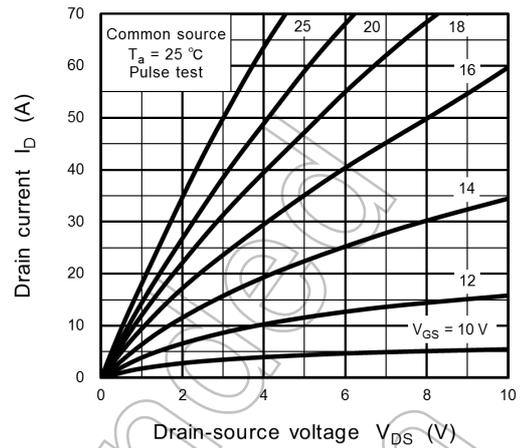


Fig. 8.2 $I_D - V_{DS}$

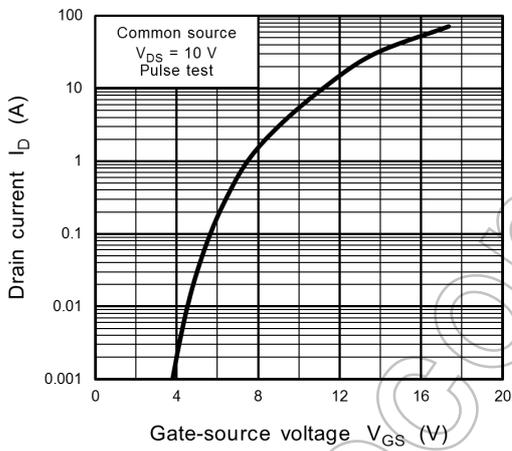


Fig. 8.3 $I_D - V_{GS}$

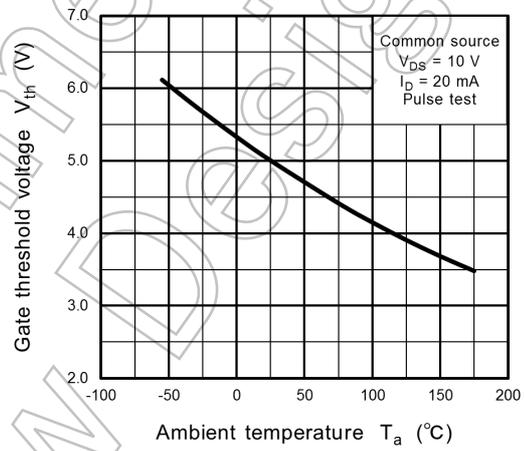


Fig. 8.4 $V_{th} - T_a$

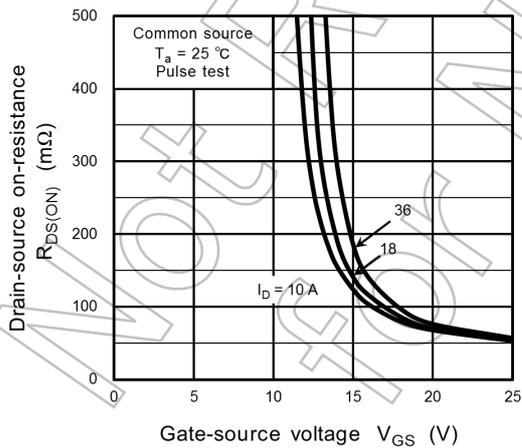


Fig. 8.5 $R_{DS(ON)} - V_{GS}$

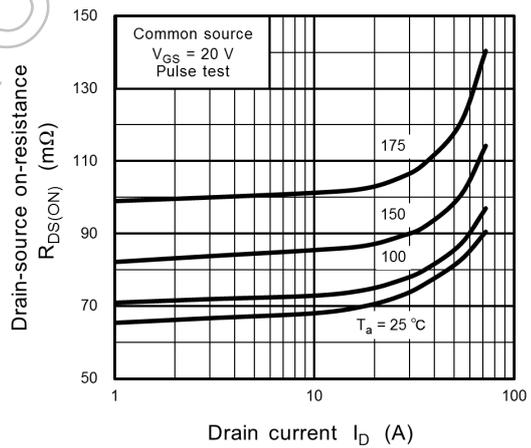


Fig. 8.6 $R_{DS(ON)} - I_D$

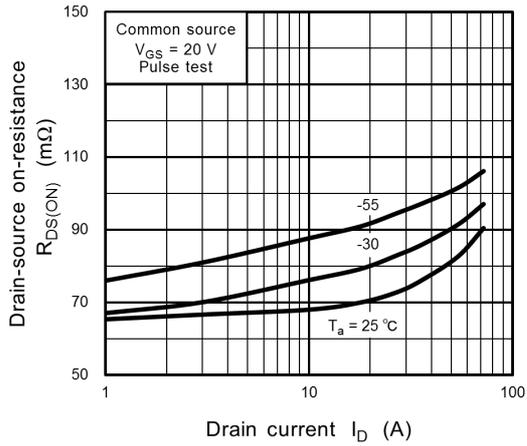


Fig. 8.7 $R_{DS(ON)} - I_D$

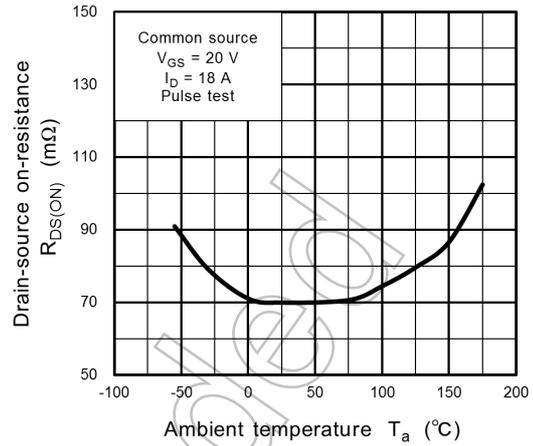


Fig. 8.8 $R_{DS(ON)} - T_a$

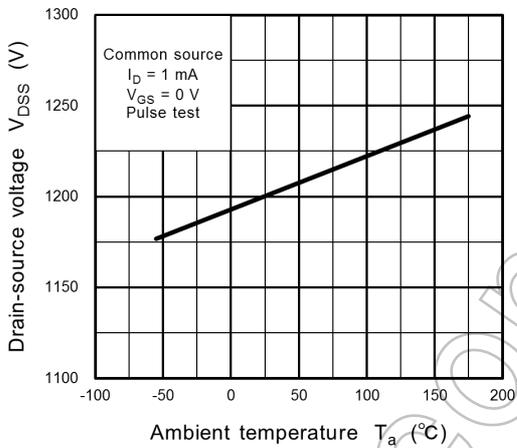


Fig. 8.9 $V_{DS} - T_a$

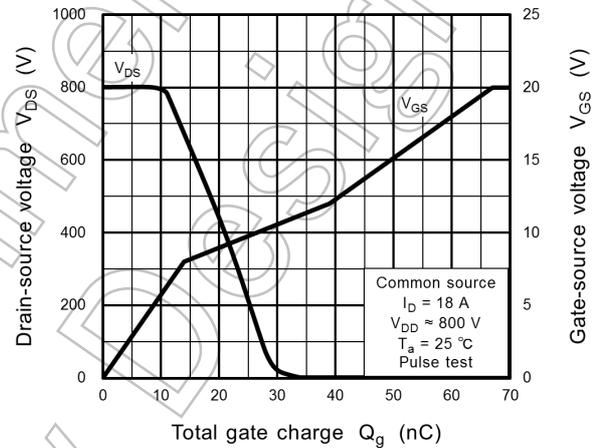


Fig. 8.10 Dynamic Input/Output Characteristics

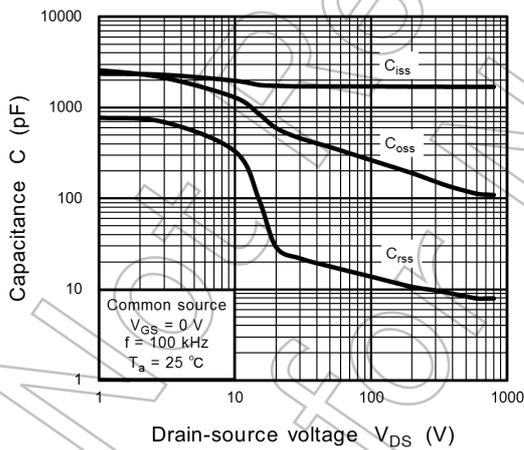


Fig. 8.11 $C - V_{DS}$

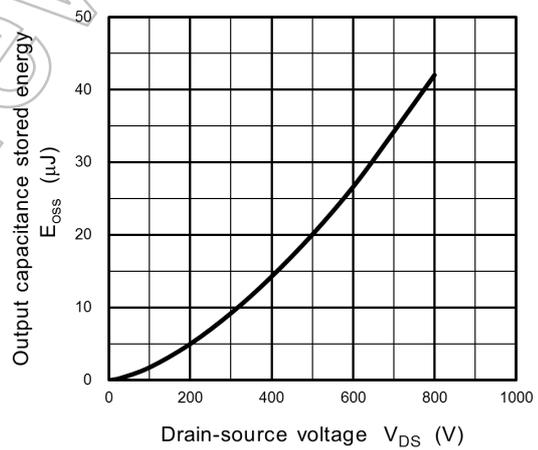
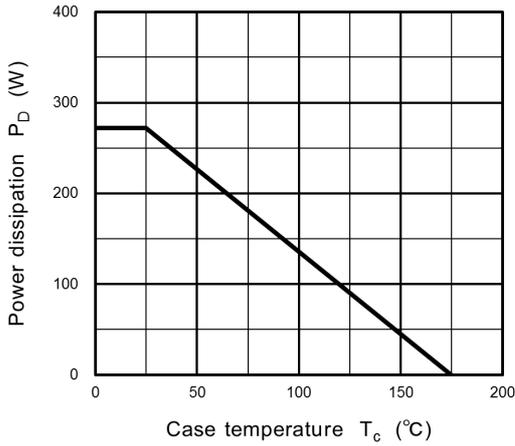


Fig. 8.12 $E_{oss} - V_{DS}$



**Fig. 8.13 $P_D - T_c$
(Guaranteed Maximum)**

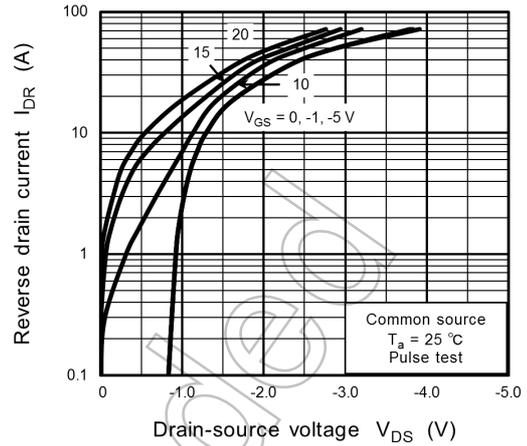
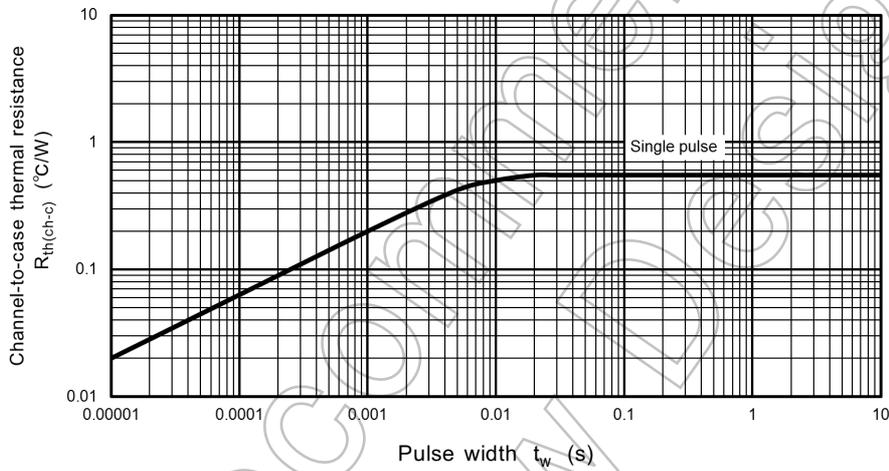
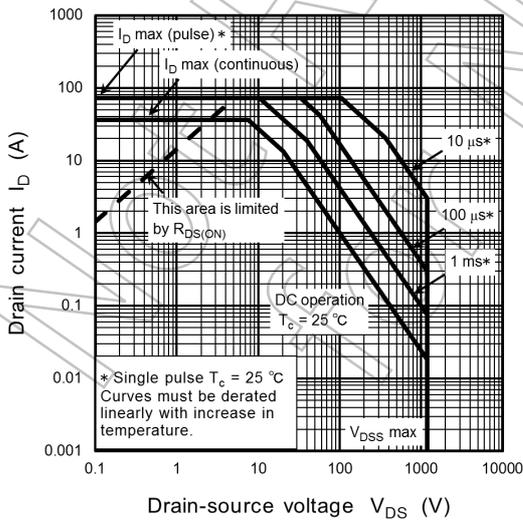


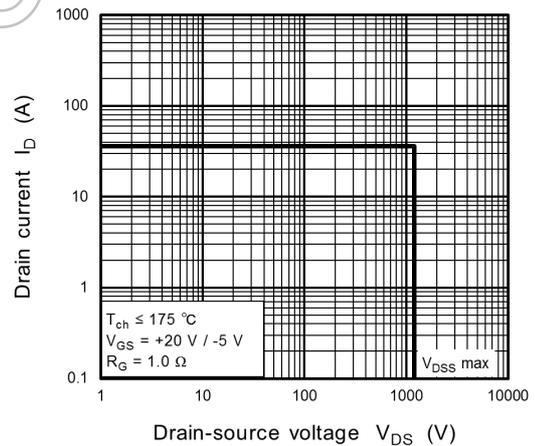
Fig. 8.14 $I_{DR} - V_{DS}$



**Fig. 8.15 $R_{th(ch-c)} - t_w$
(Guaranteed Maximum)**



**Fig. 8.16 Safe Operating Area
(Guaranteed Maximum)**



**Fig. 8.17 Reverse Safe Operating Area
(Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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