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Dear customers

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Toshiba Electronic Devices & Storage Corporation
Toshiba Electronic Device Solutions Corporation

Regarding a problem when Serial Periferal Interface (TSPI) utilize DMA Controler (DMAC)

Thank you for using Toshiba microcontrollers.
In the data transfer of DMAC + TSPI, a problem was found that some data was discarded. And we will inform you about the phenomenon and workaround.
We apologize for any inconvenience, but we ask that you review the content.
If you have any questions about this matter, please contact our sales representative.

1. Product

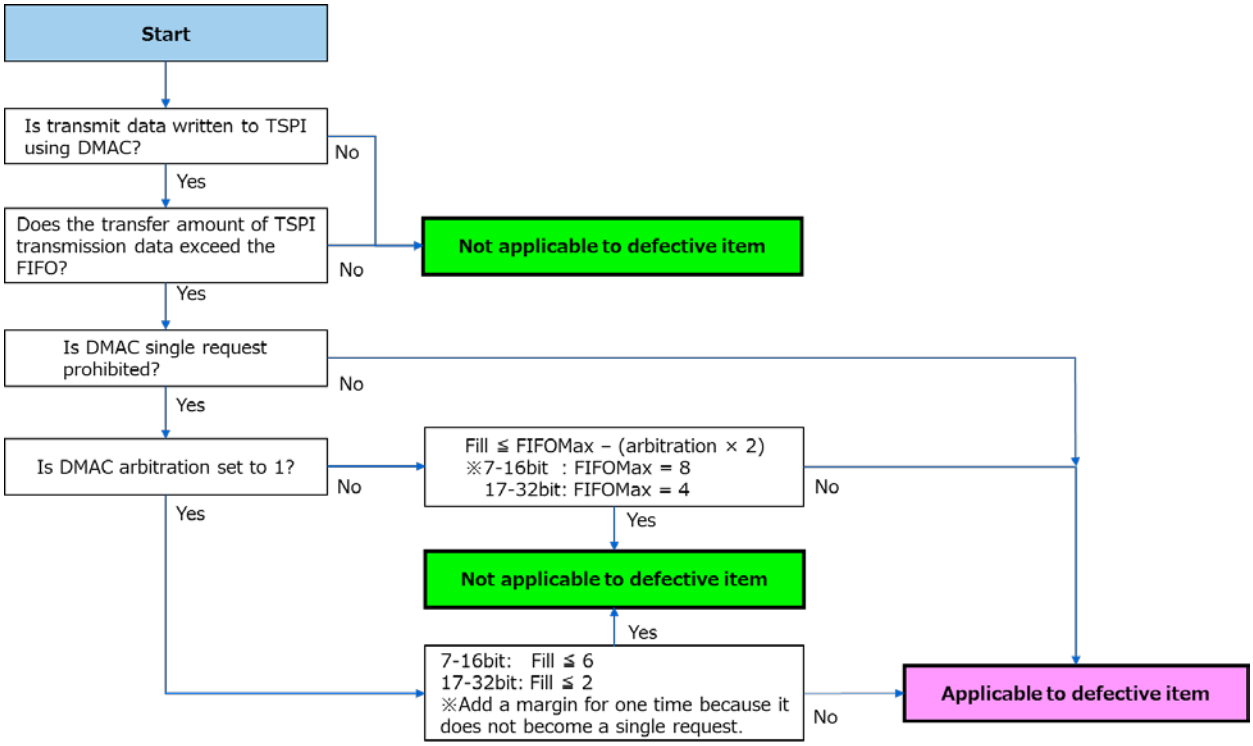
M3H group(1)、M3H group(2)、M4K group(1)、M4K group(2)

2. Occurrence phenomenon

When transmitting data to TSPI using the DMAC, FIFO control may not be performed correctly depens on the DMAC and TSPI setting conditions, and the data transferred by the DMAC to the TSPI may be discarded.

3. Occurrence condition

Please check the detailed conditions of the problem occurrence in the flowchart below.



4. How to avoid the problem

When performing TSPI transmission using the DMAC, set the DMAC and TSPI to (1) or (2) below.

(1) Set arbitration of DMAC to once

DMAC:

- Write "0000" to the Tansfer mode setup(**DMAChnlCfg**)<R_power> in the Channel control data to set arbitration to 1.
- Write "1" to the bit of the corresponding channel of the ***[DMAxChnlUseburstSet]*** to disable the single transfer request operation.

TSPI:

- Set <TIL[3:0]> of ***[TSPIxCR2]*** register to below

7-16bit: set the Fill Level less or equal 6
17-32bit: set the Fill Level less or equal 2

(2) Set arbitration of DMAC to more than once

DMAC:

- Write "0001"(twice) or "0010"(4 times) to the Tansfer mode setup(**DMAChnlCfg**)<R_power> in the Channel control data.
- Write "1" to the bit of the corresponding channel of the ***[DMAxChnlUseburstSet]*** to disable the single transfer request operation.

TSPI:

- Set <TIL[3:0]> of ***[TSPIxCR2]*** register to below

$$Fill \leqq FIFOMax - (arbitoration \times 2)$$

7-16bit: FIFOMax = 8
17-32bit: FIFOMax = 4

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5. List of the products

M3H group(1)

TMPM3H6FSFG, TMPM3H6FUFG, TMPM3H6FWFG, TMPM3H5FSFG, TMPM3H5FUFG, TMPM3H5FWFG, TMPM3H4FSUG, TMPM3H4FUUG, TMPM3H4FWUG, TMPM3H2FSDUG, TMPM3H2FUDUG, TMPM3H2FSQG, TMPM3H2FUQG, TMPM3H2FWDUG, TMPM3H2FWQG

M3Hgroup(2)

TMPM3HQFDFG, TMPM3HQFYFG, TMPM3HQFZFG, TMPM3HPFDFG, TMPM3HPFYFG, TMPM3HPFZFG, TMPM3HNFDDFG, TMPM3HNFDFG, TMPM3HNFYDFG, TMPM3HNFYFG, TMPM3HNFZDFG, TMPM3HNFZFG, TMPM3HMFDFG, TMPM3HMFYFG, TMPM3HMFZFG, TMPM3HLFDUG, TMPM3HLFYUG, TMPM3HLFZUG

M4Kgroup(1)

TMPM4K4FSAFG, TMPM4K4FSAUG, TMPM4K4FUAFG, TMPM4K4FUAUG, TMPM4K4FWAFG, TMPM4K4FWAUG, TMPM4K4FYAFG, TMPM4K4FYAUG, TMPM4K2FSADUG, TMPM4K2FUADUG, TMPM4K2FWADUG, TMPM4K2FYADUG, TMPM4K1FSAUG, TMPM4K1FUAUG, TMPM4K1FWAUG, TMPM4K1FYAUG, TMPM4K0FSADUG

M4Kgroup(2)

TMPM4KQFDFG, TMPM4KQFWFG, TMPM4KQFYFG, TMPM4KPFDDFG, TMPM4KPFWDFG, TMPM4KPFYDFG, TMPM4KNFDDFG, TMPM4KNFDFG, TMPM4KNFWDFG, TMPM4KNFWFG, TMPM4KNFYDFG, TMPM4KNFYFG, TMPM4KMFDDFG, TMPM4KMFDFG, TMPM4KMFWDFG, TMPM4KMFWFG, TMPM4KMFYDFG, TMPM4KMFYFG, TMPM4KLFDFG, TMPM4KLFDUG, TMPM4KLFWFG, TMPM4KLFWUG, TMPM4KLFYFG, TMPM4KLFYUG