Basics of CMOS Logic ICs

Outline:

This document describes applications, functions, operations, and structure of CMOS logic ICs.
Each functions (inverter, buffer, flip-flop, etc.) are explained using system diagrams, truth tables, timing charts, internal circuits, image diagrams, etc.

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1. Standard logic IC

1.1. Devices that use standard logic ICs

Standard logic ICs are used in various types of equipment.

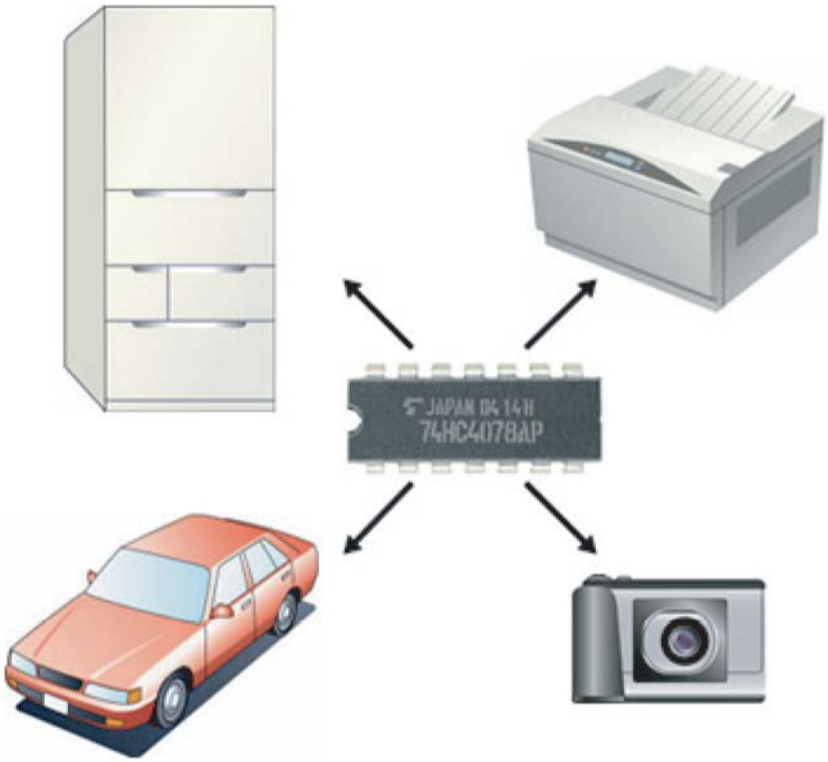


Figure 1.1 Examples of equipment using standard logic ICs

1.2. Where are standard logic ICs used?

Standard logic ICs are often used to interface LSIs such as CPUs and memories. These ICs are used to improve the driving capability (buffer), shape the waveform, and adjust the timing of the signal output. Standard logic ICs are also used to make minor modifications to the system, because it is easier to use logic ICs than to modify the LSI.

The following are examples of the use of standard logic ICs.

> Oscillation circuit: Inverter (unbuffer)
> Circuit modification of microcomputer peripheral circuits: NAND, OR, etc.
> Improvement of driving capability and reduction of output impedance when board trace is long: Buffer
> Waveform shaping of signals to CPU or memory: Buffer
> Adjusting the timing of the control signal from the microcomputer: Flip-flop, decoder, etc.

1.3. What is a standard logic IC?

Standard logic ICs are logic circuits standardized in the industry, and their functions and pin arrangements are compatible.

Although there are some exceptions in the case of small packages, compatible packages are available from various manufacturers.

Standard logic ICs have the same function and the same pin arrangement if their function number is the same.

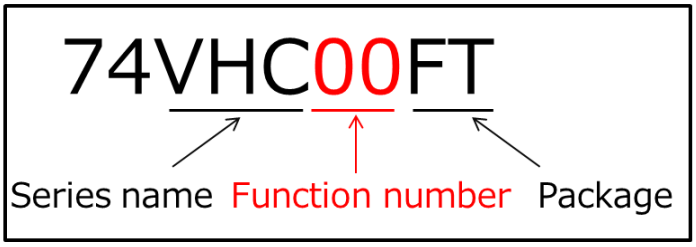


Figure 1.2 Example of product numbering method11

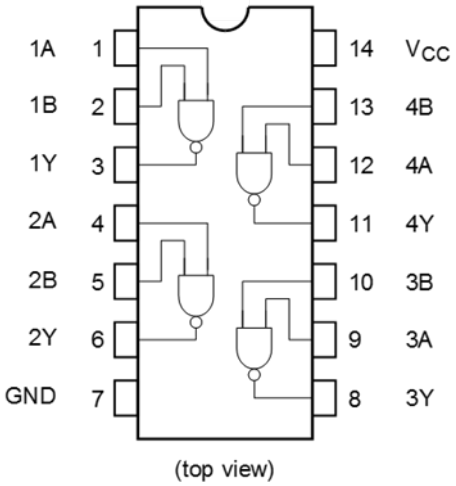


Figure 1.3 Example of pin assignment

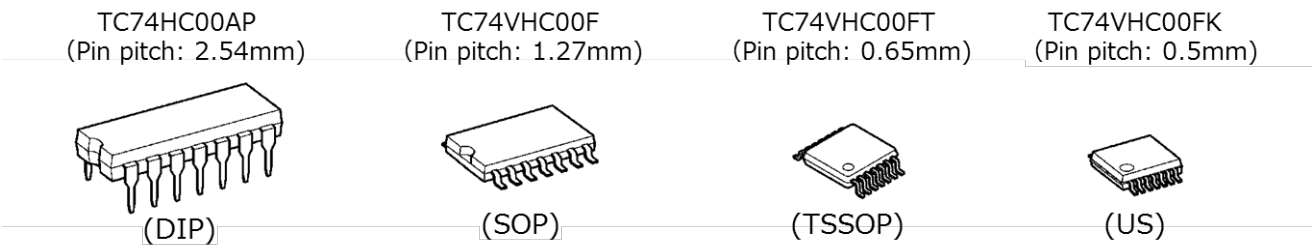


Figure 1.4 Package examples

1.4. Classification of standard logic ICs

Standard logic ICs are mainly classified as follows depending on the product structure (process), and their characteristics differ from one another.

■ TTL (Transistor-Transistor Logic)

TTL is a bipolar logic IC, a product introduced in the early days when standard logic ICs first became popular. TTLs are characterized by higher current drivability and higher operating speed than CMOS logic ICs, but consume more power. The low-level input voltage $V_{IL(Max)}$ of TTL is 0.8 V, and the high-level input voltage $V_{IH(Min)}$ of TTL is 2.0 V. This is called the TTL level.

■ CMOS logic

CMOS logic ICs consume less power than TTLs. Although the operation speed of CMOS logic in the early days was slower than that of TTL, CMOS logic, employing fine processes, now achieves higher speed than that of TTL. In typical CMOS logic ICs (V_{CC} = 5 V), the low-level input voltage $V_{IL(Max)}$ is 1.5 V and the high-level input voltage $V_{IH(Min)}$ is 3.5 V. Some CMOS logic ICs offer input levels that are compatible with TTL levels. (e.g., products with T at the end of the series name, such as VHCT)

■ BiCMOS logic

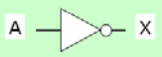
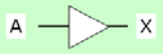
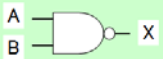
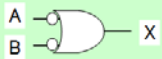
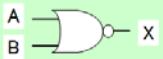
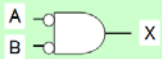
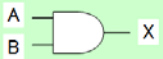
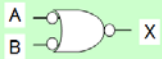
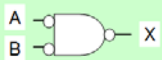
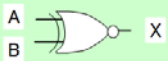
BiCMOS logic is a logic IC that uses CMOS processes in the input circuits and logic circuits to reduce power consumption and uses bipolar transistors in the output circuits to enable high-current driving. The need for both MOS and bipolar processes increases the number of manufacturing processes.

Currently, CMOS logic ICs are the mainstream standardized logic ICs. The following is a description of the CMOS logic IC.

1.5. List of basic circuits of CMOS logic ICs (combinational logic circuits)

Table 2.1 shows the logic symbols and logic equations of the combinational logic circuits that are the basis of logic circuits.

Table 1.1 Logic symbols and logic equations of combinatorial logic circuits

Circuit Function	Logic Symbols		Logic Equation
Inverter			$X=\overline{A}$
Buffer			$X=A$
NAND			$X=\overline{A\cdot B}=\overline{A}+\overline{B}$
NOR			$X=\overline{A+B}=\overline{A}\cdot\overline{B}$
AND			$X=A\cdot B=\overline{\overline{A}+\overline{B}}$
OR			$X=A+B=\overline{\overline{A}\cdot\overline{B}}$
Exclusive OR			$X=\overline{A}\cdot B+A\cdot\overline{B}$
Exclusive NOR			$X=(A\cdot B)+(\overline{A}\cdot\overline{B})$

2. CMOS logic ICs

2.1. What is CMOS?

CMOS (Complementary Metal-Oxide-Semiconductor) is a circuit composed of the P-ch MOSFET and N-ch MOSFET that operate complementarily. A logic IC using a CMOS circuit configuration is called a "CMOS logic IC."

In this circuit, the gate current flows only when the MOSFET is switched on and off, and the gate current hardly flows in the steady state. ICs that use CMOS circuits can form logic circuits that consume less current than in the case of TTLs. Figure 2.1 shows the basic circuits (inverters) of CMOS logic ICs.

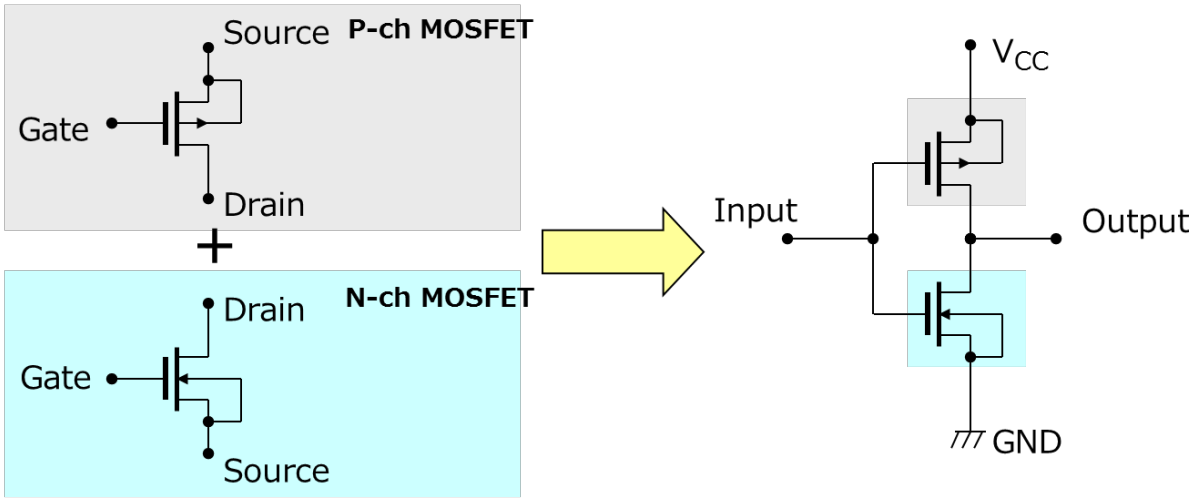
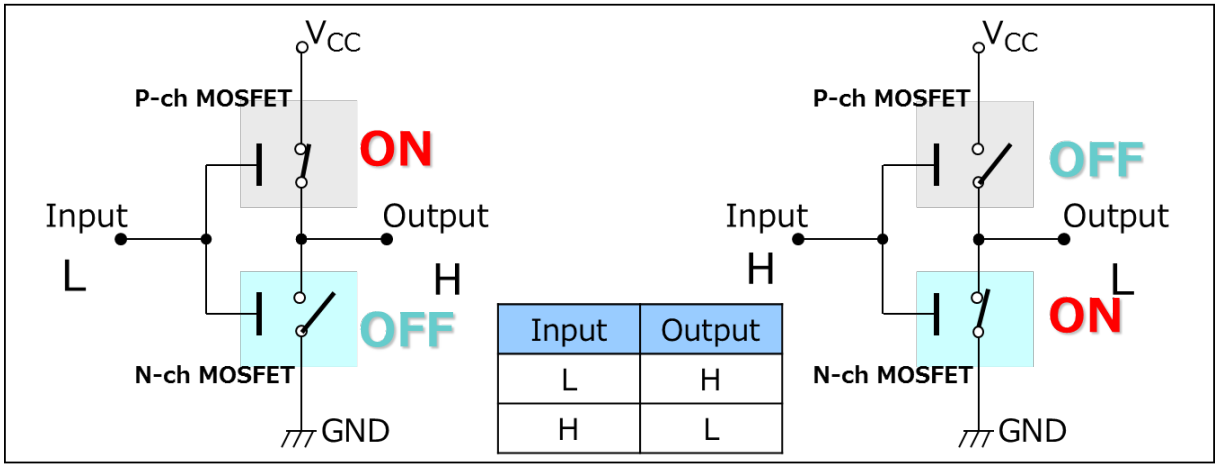


Figure 2.1 Basic inverter circuit

2.2. Basic operation of the CMOS inverter

The MOSFET of the CMOS inverter can be represented as a switch that turns on and off, as shown in Figure 2.2. When the low level (hereinafter referred to as "L") is added to the input, the N-ch MOSFET is turned off and the P-ch MOSFET is turned on. At this time, almost the same voltage as the voltage V_{CC} is output to the output terminal, and the voltage becomes a high level (hereinafter referred to as "H"). When H level is applied to the input, the P-ch MOSFET is turned off and the N-ch MOSFET is turned on. The output is at L level, which is almost the same potential as GND.



Input	Output
L	H
H	L

Figure 2.2 Circuit operation of inverter

2.3. Operation and characteristics of CMOS logic ICs MOSFET

2.3.1. Operation and characteristics of N-ch MOSFET and P-ch MOSFET

In a MOSFET, when the potential difference between the gate and the source is larger than a fixed value (threshold value $|V_{th}|$), the resistance between the drain and the source is reduced (on-state). The resistance between the drain and source at this time is called the on-resistance.

However, the direction of the voltage applied between the gates and sources is different for N-ch MOSFET and P-ch MOSFET. Figure 2.3 shows how the MOSFET turns on.

N-ch MOSFET: Turns on when the gate potential is higher than the source potential by $|V_{th}|$.

P-ch MOSFET: Turns on when the gate potential is lower than the source potential by $|V_{th}|$.

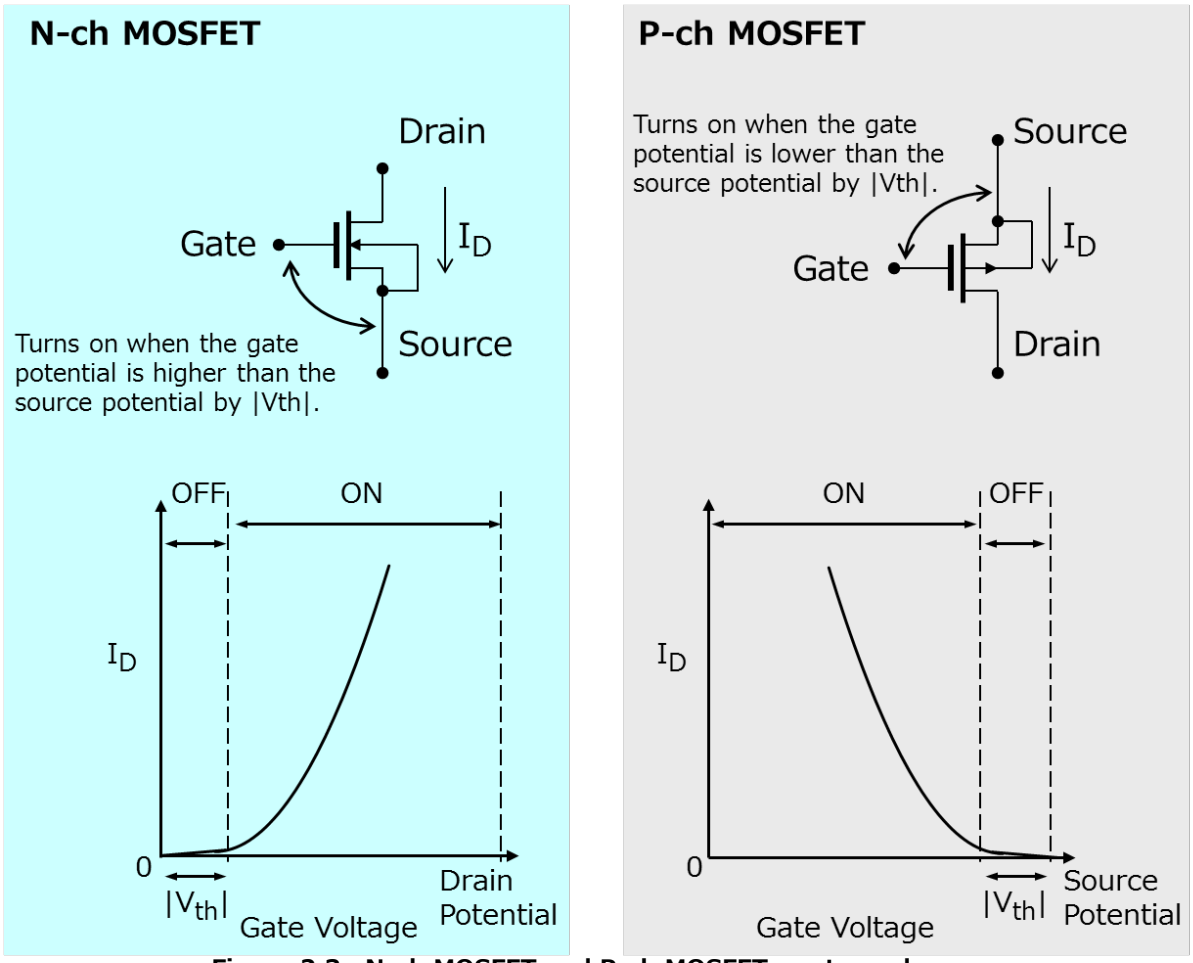


Figure 2.3 N-ch MOSFET and P-ch MOSFET are turned on.

2.3.2. V_{IN}-I_{CC} characteristics of CMOS (N-ch MOSFET +P-ch MOSFET)

Figure 2.4 shows the basic circuits of CMOS.

The basic circuit of CMOS is characterized by a very small current (I_{CC}) between the power supply and GND when V_{IN} is at the V_{CC} or GND level, as either the devices of V_{CC} side or GND side are turned off.

Therefore, in CMOS logic ICs, I_{CC} is very small when the input signals remain unchanged (the input is V_{CC} or GND-level).

Figure 2.5 shows the V_{IN}-I_{CC} characteristics of CMOS.

As described above, the current (I_{CC}) flowing between the power supply and the ground becomes very small when V_{IN} is 0 to $|V_{th}|$, or $V_{CC} - |V_{th}|$ to V_{CC}. However, since a through current flows from P-ch MOSFET to N-ch MOSFET when V_{IN} is between $|V_{th}|$ and $V_{CC} - |V_{th}|$, I_{CC} increases. Therefore, care must be taken not to use signals with extremely slow V_{IN} rise or fall times (referred to as "slow inputs").

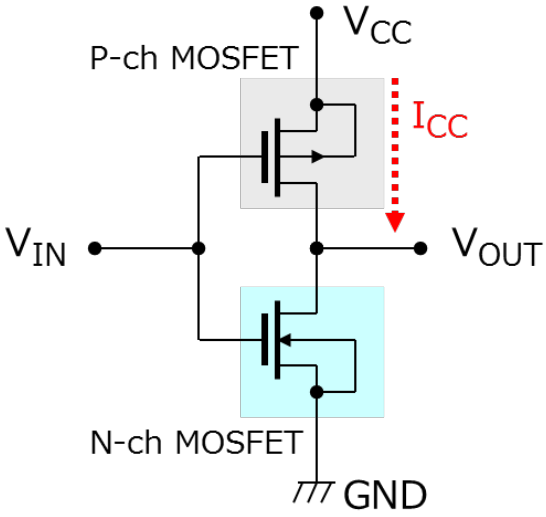


Figure 2.4 Basic circuits of CMOS

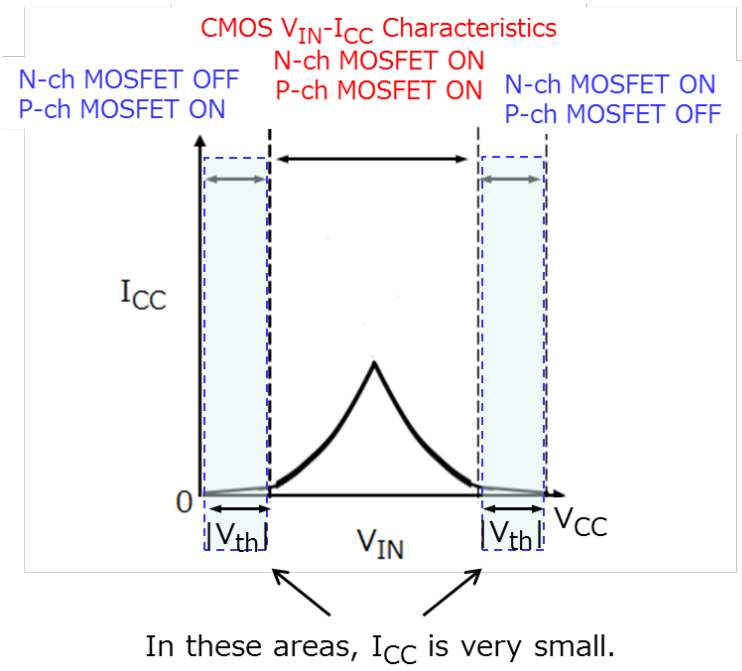


Figure 2.5 V_{IN}-I_{CC} characteristics of CMOS

2.4. Typical functions and operations of CMOS logic ICs

This section explains the operation of typical functions of CMOS logic ICs.

2.4.1. Inverter (NOT) (product examples: 74VHC04, 74VHCU04)

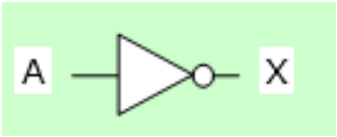
The output (X) of the inverter is inverted to the input (A) signals. Types of inverters include typical inverters and unbuffers.

Typically, inverters are used to invert the logic of an input signal. Three stages of inverter circuits are used to shape a waveform.

An unbuffer, on the other hand, consists of a single-stage inverter circuit, and is used in oscillating circuits and other applications.

Shown below are the inverter's logic symbol (Figure 2.6), truth table (Figure 2.7), timing chart (Figure 2.8), and internal circuit (Figure 2.9).

In the case of the three-stage inverter circuit, the signal changes three times, and the inverted signal is output with respect to the input signal.



Input	Output
A	X
L	H
H	L

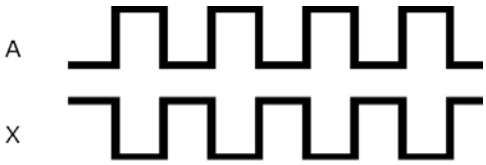


Figure 2.6 Logic symbol **Figure 2.7 Truth table** **Figure 2.8 Timing chart**

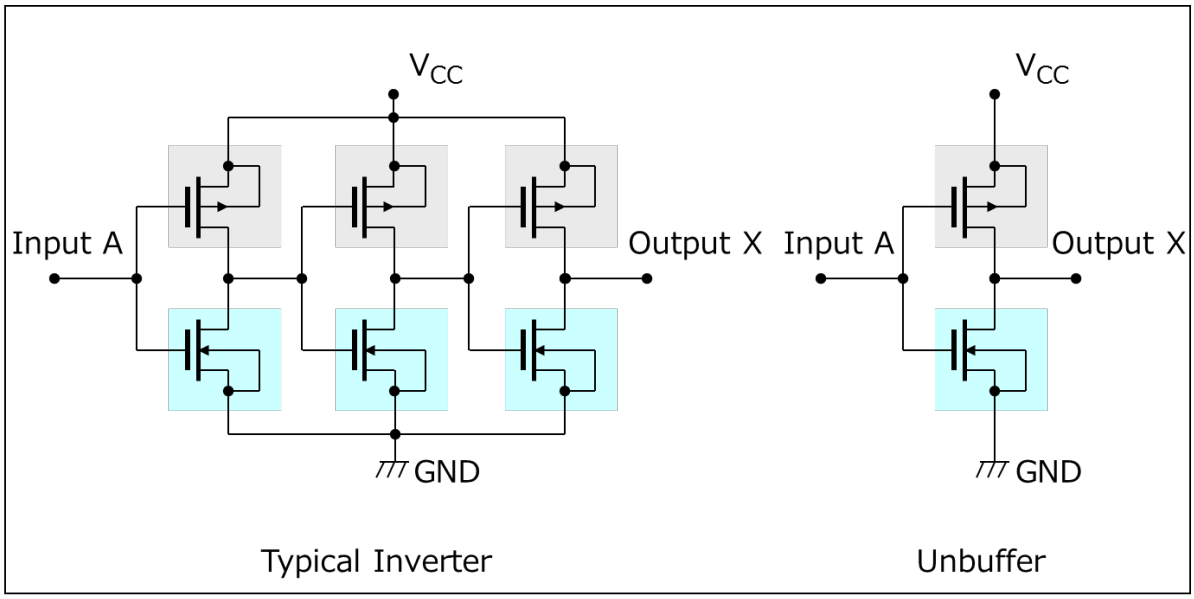


Figure 2.9 Internal circuit of inverter

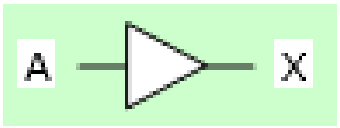
2.4.2. Buffer (product examples: 74VHC126, 74VHC245)

Buffers do not perform logical operations.
Buffers increase the driving capability to increase the number of signal lines connected and shape the waveform.

Buffers are used to increase drive capacity when the load is heavy. They are also used to lower the output impedance when the signal is attenuated by parasitic reactance or capacitance due to long board trace.
Buffers are used in various kinds of electronic devices.

Some types of buffers called transceivers (bidirectional bus buffers) can both send and receive data on one input/output terminal. The transceiver can switch the direction of the signal by the control signal (DIR), and so it is used for bus lines through which data pass in both directions.

The buffer's logic symbol (Figure 2.10), truth table (Figure 2.11), timing chart (Figure 2.12), and internal circuit (Figure 2.13) are shown below.
The buffer uses two inverter circuits.
In the case of the 2-stage inverter circuit, since the signal is changed twice, a signal of the same phase is output with respect to the input signal



Input	Output
A	X
L	L
H	H

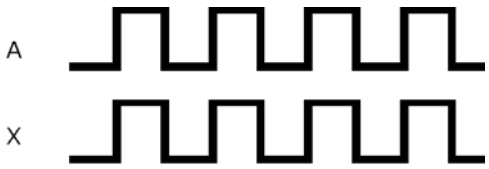


Figure 2.10 Logic symbol **Figure 2.11 Truth table** **Figure 2.12 Timing chart**

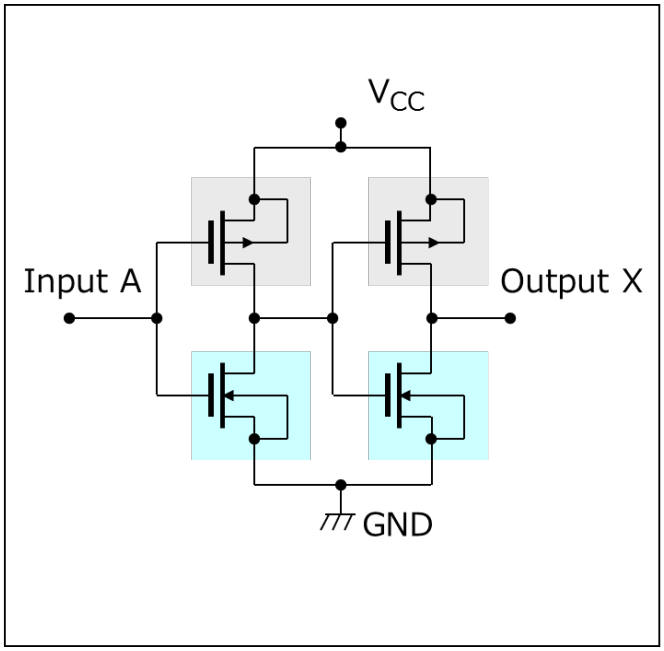


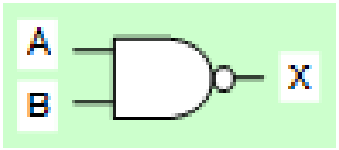
Figure 2.13 Internal circuit of buffer

2.4.3. NAND, NOR, AND, OR, and Exclusive OR (product examples: 74VHC00, 74VHC02, 74VHC08, 74VHC32, 74VHC86)

NAND, NOR, AND, OR, Exclusive OR, and Exclusive NOR are the basic logical arithmetic circuits called gates. Typical examples are NAND.

Shown below are NAND's logic symbol (Figure 2.14), truth table (Figure 2.15), timing chart (Figure 2.16), and internal circuit (Figure 2.17).
NAND consists of two P-ch MOSFETs and two N-ch MOSFETs.
When all inputs are H, the output is L, and in all other combinations, output is H.
For example, when inputs A and B are L, the N-ch MOSFET on the ground side are turned off and the P-ch MOSFET on the V_{CC} side are turned on, and so H is output.
On the other hand, when inputs A and B are H, the P-ch MOSFET on the V_{CC} side is turned off, and the N-ch MOSFET on the GND side is turned on, and so L is output.
When the input A is L and the input B is H, the P-ch MOSFET turns on, one of the N-ch MOSFETs turns off, and so H is output. The same applies in the case where input A is H and input B is L.

Similar to NAND, NOR, AND, OR, Exclusive OR are composed of combinations of P-ch MOSFET and N-ch MOSFET.



Inputs		Output
A	B	X
L	L	H
L	H	H
H	L	H
H	H	L

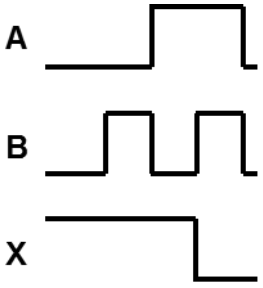


Figure 2.14 Logic symbol **Figure 2.15 Truth table** **Figure 2.16 Timing chart**

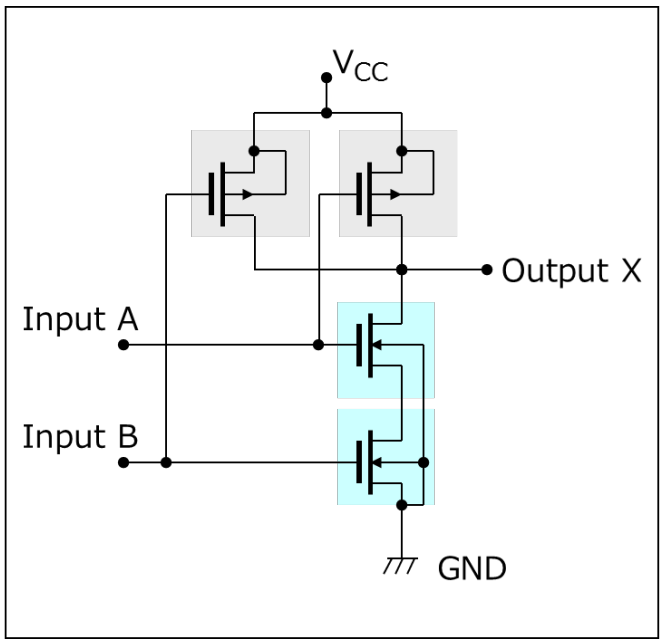


Figure 2.17 Internal circuit of NAND

2.4.4. Decoder (product example: 74VHC138)

The decoder converts N input signals into 2^N output signals.
This signal is typically used for port extension as a chip select signal.

About decoder operation

Shown below are a block diagram (Figure 2.18), a truth table (Figure 2.19), a timing chart (Figure 2.20), and a chip-select image (Figure 2.21), assuming a product that converts three inputs into eight outputs (3 to 8 decoder).

The image of the chip select shows the case where the three input signals (A, B, C) are L. At this time, only X0 of the eight output terminals outputs L, and other output terminals output H. IC0 is selected. In this way, any chip can be selected using a combination of three input signals.

There are 8 outputs for the decoder whereas there are 3 outputs for the MCU. Thus, this is an example of port extension.

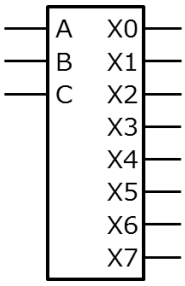


Figure 2.18 Block diagram

Inputs			Outputs							
A	B	C	X0	X1	X2	X3	X4	X5	X6	X7
L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
H	H	L	H	H	H	L	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

Figure 2.19 Truth table

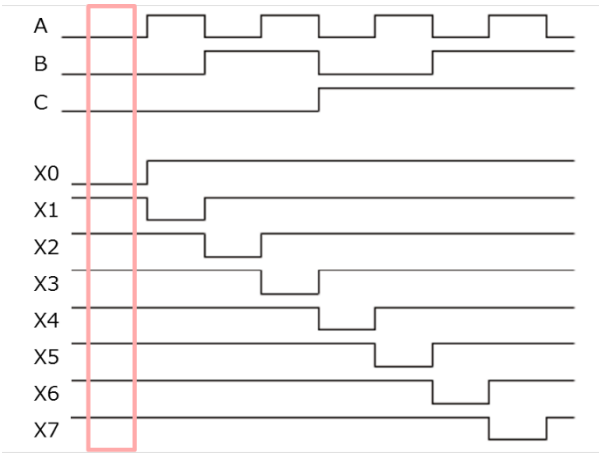


Figure 2.20 Timing chart

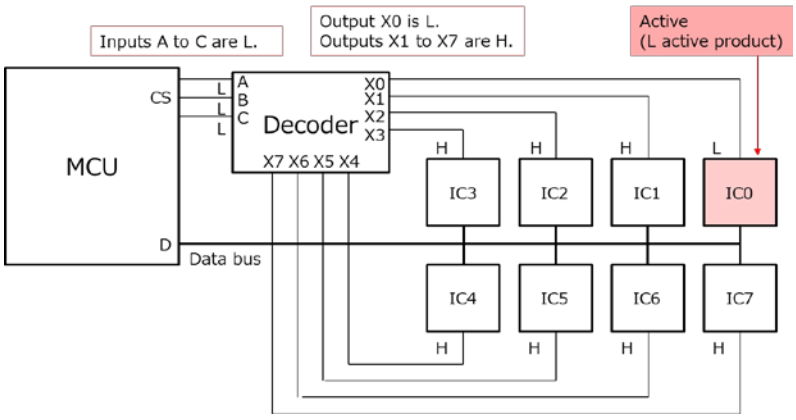


Figure 2.21 Image of chip select

2.4.5. Multiplexer

The multiplexer can select and output one signal from multiple input signals.
The demultiplexer can select and output any one of the multiple outputs of an input signal.
Shown below is an image of a multiplexer and a demultiplexer (Figure 3.22).

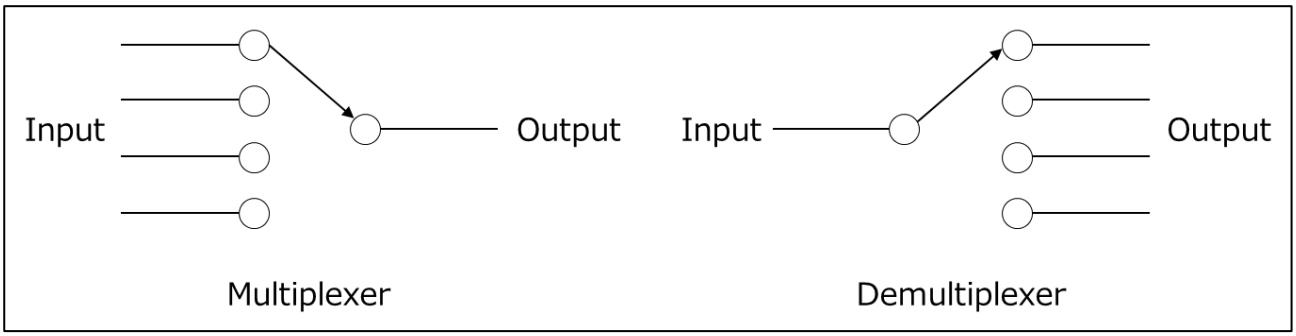


Figure 2.22 Image of multiplexer and demultiplexer

There are two types of multiplexers: digital multiplexers and analog multiplexers.

Digital multiplexer (product examples: 74VHC153, 74VHC157)
A digital multiplexer can select and output one signal from multiple digital input signals.

Analog multiplexer (product examples: 74VHC4051, 74VHC4052, 74VHC4053)
An analog multiplexer can select and output one signal from multiple analog input signals by using analog switches. Analog switches can pass signals in both input and output directions, and so they can act as both multiplexers and demultiplexers. See 2.4.10 for analog switches.

Types of multiplexers (according to the number of channels)
Multiplexers include two-channel multiplexers, which are two-input and one-output products, four-channel multiplexers, which are four-input and one-output products, and eight-channel multiplexers, which are eight-input and one-output products.
Figure 2.23 shows these three types of multiplexers.

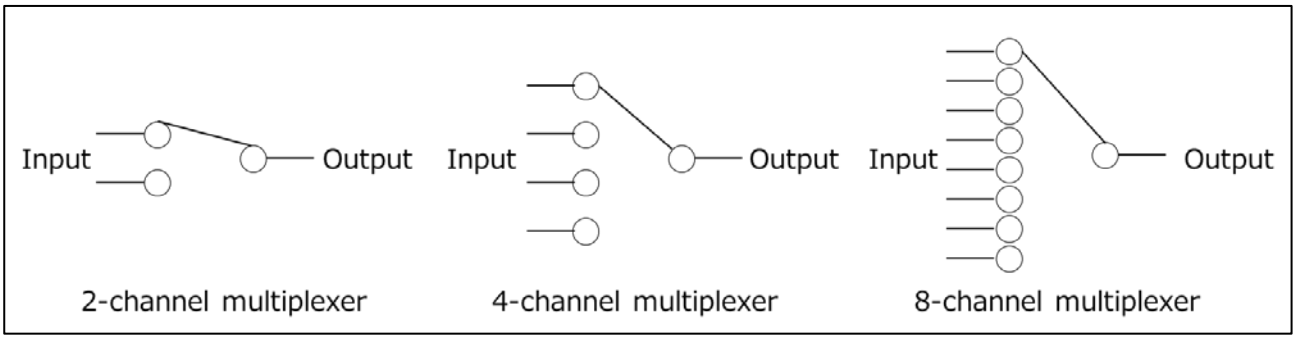


Figure 2.23 Types of multiplexers (according to the number of channels)

Operation of a 2-channel multiplexer

Shown below are a system diagram of a two-channel multiplexer (Figure 2.24), a truth table (Figure 2.25), and a timing chart (Figure 2.26).

When the signal of the select input (SELECT) is L, the input (A) is selected and the logic of the input (A) is output (Y). On the other hand, when the signal of the select input (SELECT) is H, the input (B) is selected and the logic of the input (B) is output to output (Y).

The strobe input (/ST) is used to disable data output. When the input (/ST) is H, the output becomes L unconditionally. /ST represents ST.

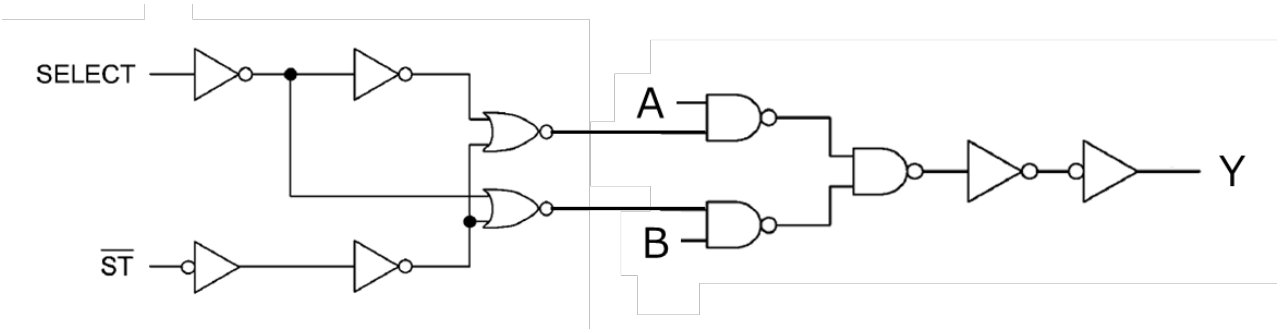


Figure 2.24 System diagram of 2-channel multiplexer

Inputs				Output
$\overline{ST}$	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X: Don't Care

Figure 2.25 2-channel multiplexer truth table

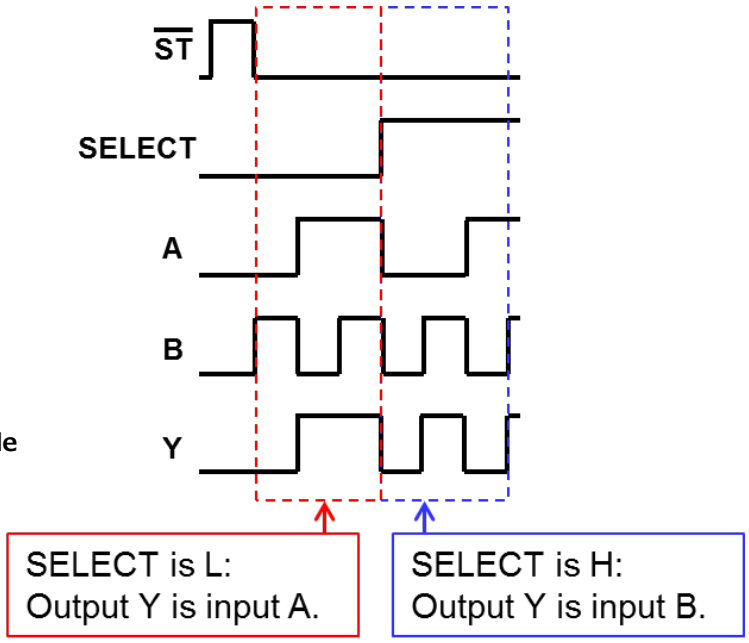


Figure 2.26 2-channel multiplexer timing chart

2.4.6. Latch (product example: 74VHC373)

The latch can hold data under certain conditions.

There are various types of latches, such as D-latches and RS latches. This section explains the operation using the D-latch as an example.

For a D-latch product composed of an input signal (D), a latch enable signal (LE), and an output (Q), the previous output (Q) is held when the latch enable signal (LE) is L, but the same logic as the input logic is output when the latch enable signal (LE) is H. Shown in Figure 2.27 is a timing chart.

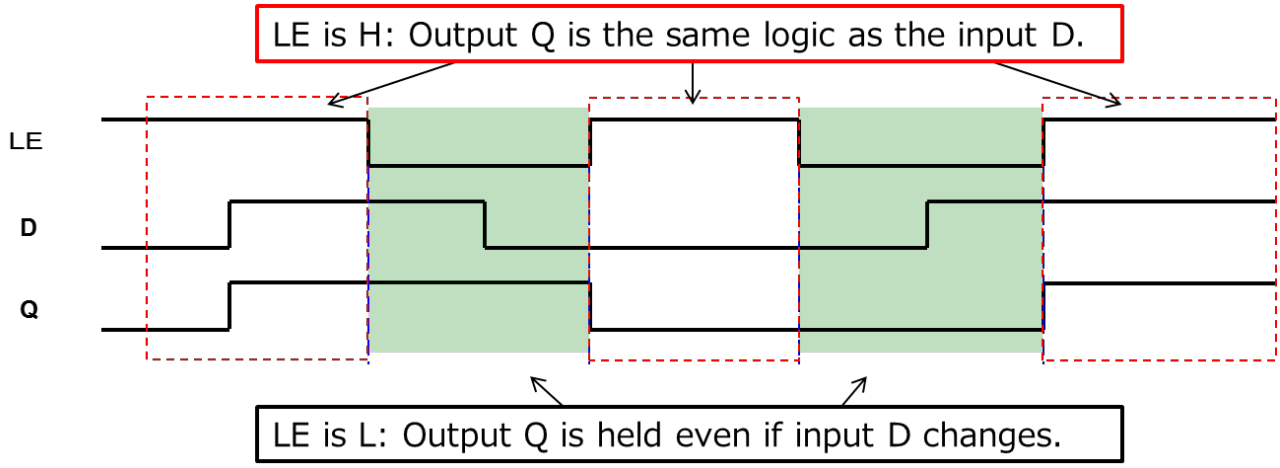


Figure 2.27 Timing chart and output image

Various signal lines can be controlled simultaneously by using multiple latches controlled by the same latch enable signal (LE).

The block diagram of the D-latch (Figure 2.28) and the truth table (Figure 2.29) are shown below.

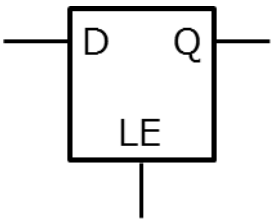


Figure 2.28 Block diagram

Inputs		Output
LE	D	Q
H	L	L
H	H	H
L	X	Qn

X: Don't Care
Qn: Q outputs are latched at the time when the LE input is taken to low logic level.

Figure 2.29 Truth table

Operation of D-latch

The operation of the D-latch is explained using the system diagram (Figure 2.30).

The inverters enclosed in red squares in the system diagram represent clocked inverters. See the following page for internal circuits of clocked inverters. The D-latch consists of two clocked inverters and one inverter.

In the D-latch, when L is input to the latch enable signal (LE), the output of the clocked inverter (1) becomes high impedance, and the input signal is not transmitted to the inverter of the next stage. At this time, the clocked inverter (2) outputs the inverted signal of the output (Q). Since the signal is inverted by the inverter, the data of the output (Q) are held (green arrow in the system drawing). When the latch enable signal (LE) is L, the output does not change even if the input changes.

On the other hand, when H is input to the latch enable signal (LE), the output of the clocked inverter (1) becomes the inverted signal of the input, and the signal is inverted by the next inverter. Therefore, the same logic as the input logic is output to the output (Q). (Blue arrow in the system diagram)

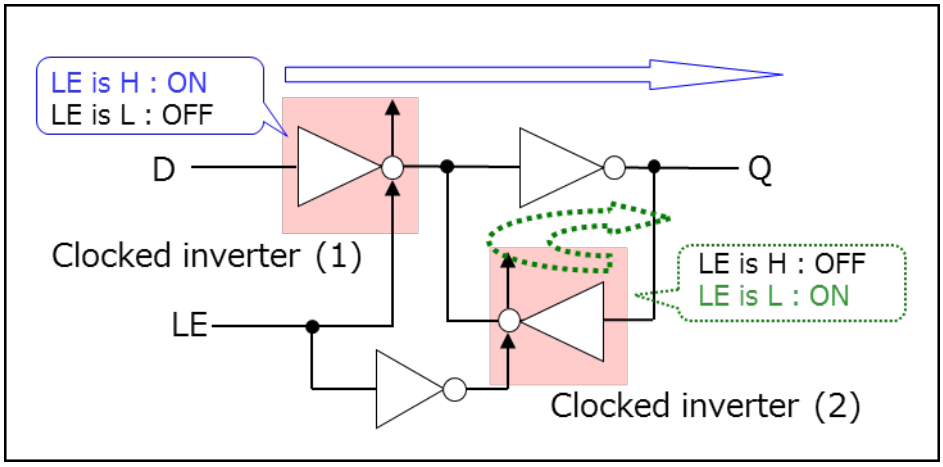


Figure 2.30 System diagram

Clocked inverter

The logic symbol (Figure 2.31), an internal circuit (Figure 2.32), and a truth table (Figure 2.33) of the clocked inverter are shown below.

When the input (φ) is set to H, the N-ch MOSFET on the ground side is turned on and the P-ch MOSFET on the V_{CC} side is also turned on so that this circuit operates as a normal inverter circuit. The signal input to input (A) is inverted and output.

On the other hand, when the input φ becomes L, the N-ch MOSFET on the GND side is turned off and the P-ch MOSFET on the V_{CC} side is turned off so that the output becomes high-impedance.

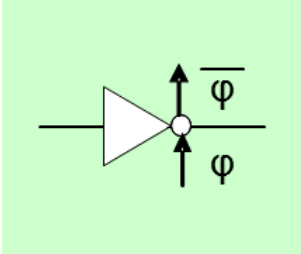


Figure 2.31 Logic symbol of clocked inverter21

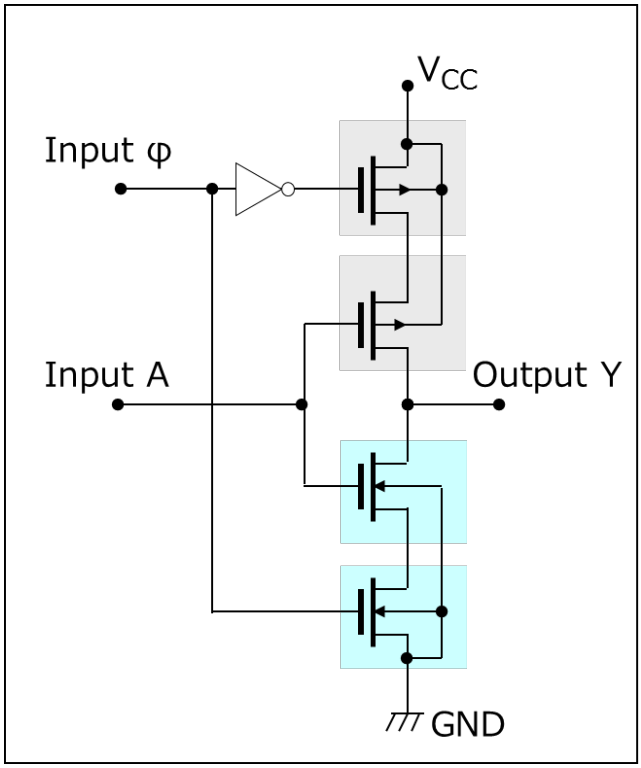


Figure 2.32 Internal circuit of clocked inverter

Inputs		Output
φ	A	X
H	H	L
H	L	H
L	X	Z

X: Don't Care
Z: High Impedance

Figure 2.33 Truth table

2.4.7. Flip-flop (product example: 74VHC74)

Flip-flops can hold data under certain conditions. Flip-flops are sometimes referred to as FFs for short. There are several types of flip-flops, including D-type flip-flops and JK-type flip-flops. This section explains the operation of the D-type flip-flop as an example.

The difference from the D-latch is that the output data are held even when the clock falls. (In the case of the D-latch, when the LE input is H, the same logic as the input logic is output.)

In the case of a product composed of an input (D), a clock (CK), and an output (Q), the input (D) is held and the same signal is output when the clock (CK) rises. Until the next rise edge of clock (CK) input, output (Q) does not change even if input (D) changes. When the clock (CK) is not rising, the input (D) held by the immediately preceding rising clock (CK) continues to be output. Shown in Figure 2.34 is a timing chart. Some products have CLR and PR inputs that can initialize the internal hold signal.

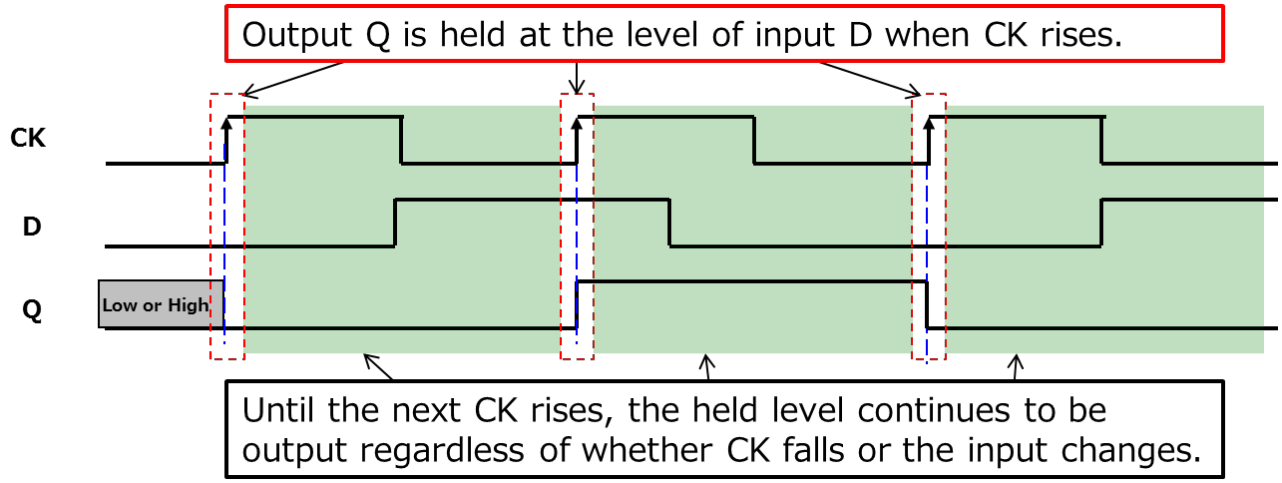


Figure 2.34 Timing chart and output image

Applications of flip-flops include asynchronous signal synchronization, digital signal delay circuits, counters, and frequency dividers.

Shown below are a block diagram of a D-type flip-flop (Figure 2.35) and a truth table (Figure 2.36).

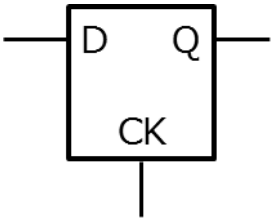


Figure 2.35 Block diagram

Inputs		Output
CK	D	Q
↑	L	L
↑	H	H
↓	X	Qn

X: Don't Care
Qn: No Change

Figure 2.36 Truth table

Operation of D-type flip-flop

The operation of the D-type flip-flop is explained using the system diagram (Figure 2.37).
The D-type flip-flop is constructed by connecting two stages of D-latch circuits. Refer to 2.4.6 for the latch operation.

For the D-type flip-flop, the latch circuit (1) operates when the clock (CK) rises. While the clock (CK) is H, since the latch circuit (1) continues to operate and the clocked inverter at the first stage of the latch circuit (2) also operates, the data held in the latch circuit (1) are output to the output (Q) (blue arrow in the system diagram). The output does not change even if the input signal changes.
When the clock (CK) becomes L, the latch circuit (2) operates and continues to output the data held by the latch circuit (1) (green arrow in the system diagram). Even at this time, the output does not change even if the input signal changes.
Note that the output (Q) before reading the rising edge of the clock (CK) is unknown.

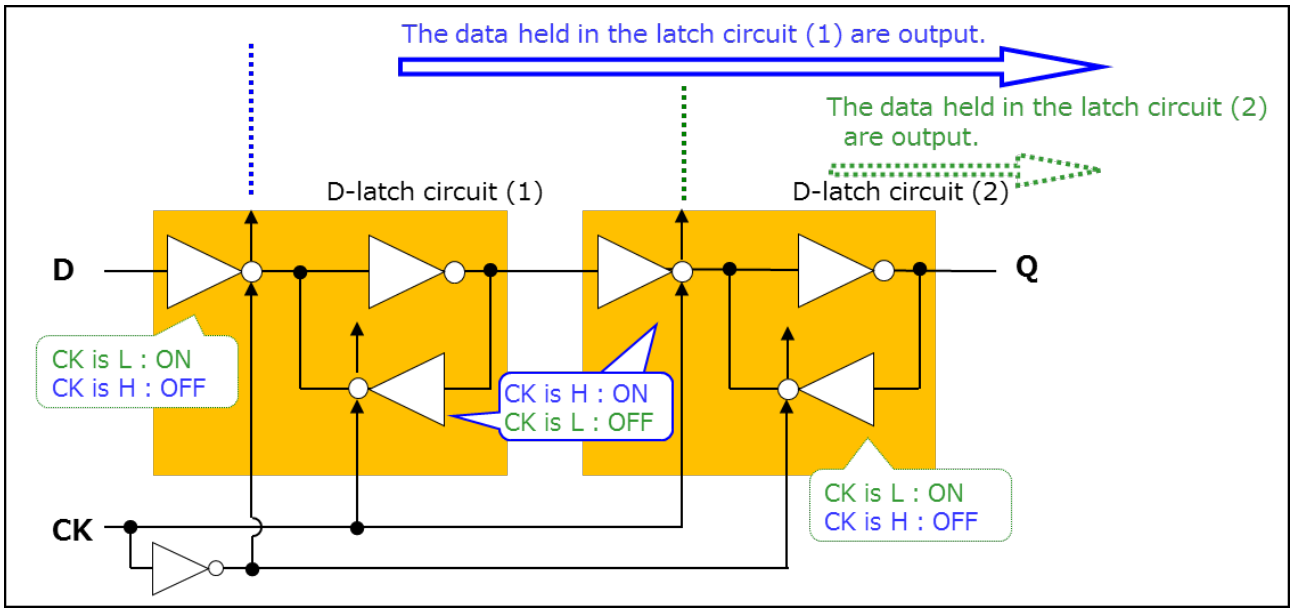


Figure 2.37 System diagram

2.4.8. Counter (product examples: 74VHC393, 74VHC161)

The counter performs up-counter (addition) and down-counter (subtraction) in accordance with the input clock (CK). A 4-bit counter can count up to 16, an 8-bit counter up to 256, and a 14-bit counter up to 16384. Some products have a CLR input that can initialize the internal hold signal.
Counters are built into various types of equipment, including digital timers, calculators, and stopwatches.

There are two types of counters: CK asynchronous (ripple-carry method) and CK synchronous (parallel-carry method). In the case of CK asynchronous, assuming that the propagation delay time is tpd, the n-stage tpd is n times tpd and greatly delayed.
If you assemble logic using the output signal, a hazard may occur in the output of the assembled logic.

Shown below are a block diagram (Figure 2.38) and a truth table (Figure 2.39) of a 4-bit up-counter. The counter consists of four flip-flops.

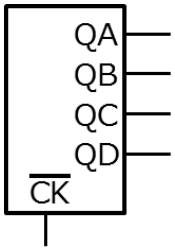


Figure 2.38 Block diagram

Input	Outputs			
$\overline{CK}$	QD	QC	QB	QA
↓	Count up			
↑	No change			

Figure2.39 Truth table

Operation of the up counter

The operation of the up counter is explained using the system diagram (Figure 2.40) and the timing chart (Figure 2.41).

In the case of the up-counter, the output (/Q) of the first flip-flop is connected to the input (CK) of the second flip-flop. Similarly, the output (/Q) of the second flip-flop is connected to the input (CK) of the third flip-flop. The same applies to the third and fourth flip-flop.

In the first flip-flop, the output (/Q) switches at the falling edge of input (/CK). The second flip-flop operates at the falling edge of output (QA). The third and subsequent flip-flops operate at the falling edge of the output (Q) of the preceding flip-flop. /Q represents Q and /CK represents CK.

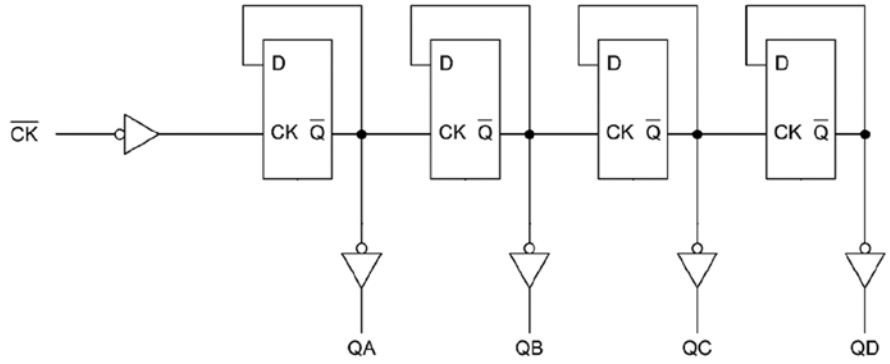


Figure 2.40 System diagram

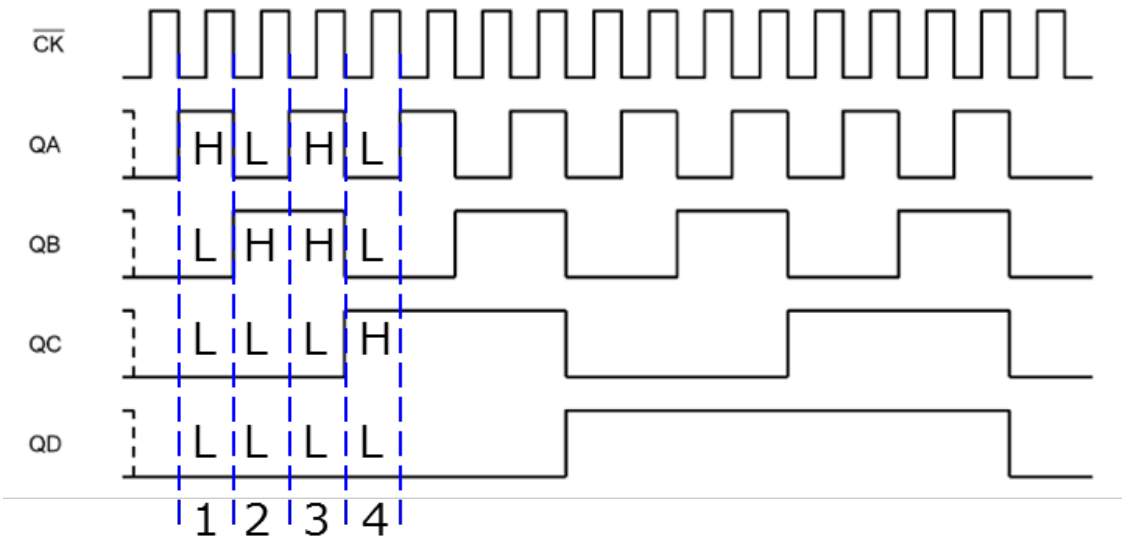


Figure 2.41 Timing chart

2.4.9. Shift register (product example: 74VHC164)

The shift register converts serial data to parallel data (SI-PO) or parallel data to serial data (PI-SO). Parallel-serial conversion is used to reduce the number of transmission lines (reduce the number of bits). Some products have a CLR input that can initialize the internal hold signal.

The block diagram (Figure 2.42) and the truth table (Figure 2.43) of the shift register are shown below. The shift register is composed of multiple flip-flops.

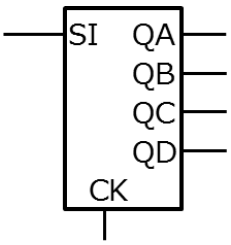


Figure 2.42 Block diagram

Inputs		Outputs			
CK	SI	QA	QB	QC	QD
↑	L	L	QAn	QBn	QCn
↑	H	H	QAn	QBn	QCn

QAn to QCn: The level of QA to QD, respectively, before the most recent positive edge of the CK.

Figure 2.43 Truth table

Operation of the Shift register

The operation of the shift register is explained using the system diagram (Figure 2.44) and the timing chart (Figure 2.45).

In the case of the shift register, the output (Q) of the first flip-flop is connected to the input (D) of the second flip-flop. Similarly, the output (Q) of the second flip-flop is connected to the input (D) of the third flip-flop. The same applies to the third and fourth flip-flops.

The input (SI) is connected to the input (D) of the first flip-flop. Input (SI) data are output to QA at the rising edge of the clock (CK). When the clock (CK) rises four times and the input (SI) signal is transmitted to the fourth flip-flop, the serial signal input to SI is converted into parallel signals (QD, QC, QB, and QA).

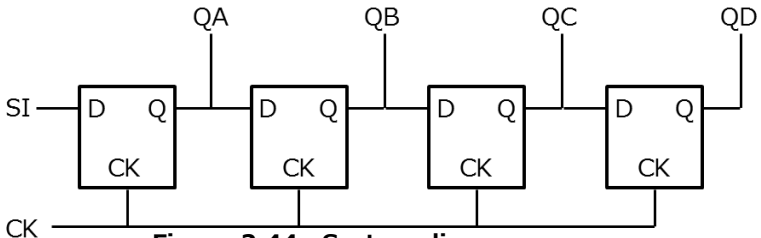


Figure 2.44 System diagram

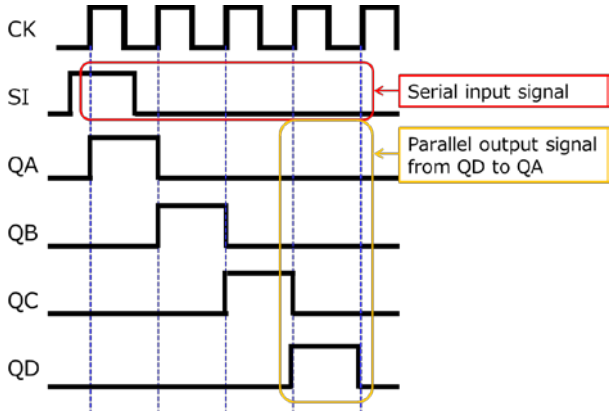


Figure 2.45 Timing chart (image of serial-in parallel conversion)

2.4.10. Analog switch (bilateral switch) (product example: 74VHC4066)

An analog switch can control the transmission and interruption of an analog signal such as a sine wave by turning the switch on and off.
The analog switch is constructed by connecting N-ch MOSFET and P-ch MOSFET in parallel in order to reduce on-resistance and improve linearity of input/output characteristics.
The analog switch characteristics in the data sheet include typical values such as sine wave distortion, frequency response, feed-through attenuation, and crosstalk.

Shown below are the logic symbol (Figure 2.46), the truth table (Figure 2.47), the timing chart (Figure 2.48), and the internal circuit (Figure 2.49) of an analog switch.

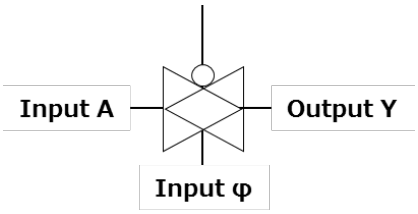


Figure 2.46 Logic symbol

Inputs		Output
φ	A	Y
H	H	H
H	L	L
L	X	Z

X: Don't Care
Z: High Impedance

Figure 2.47 Truth table

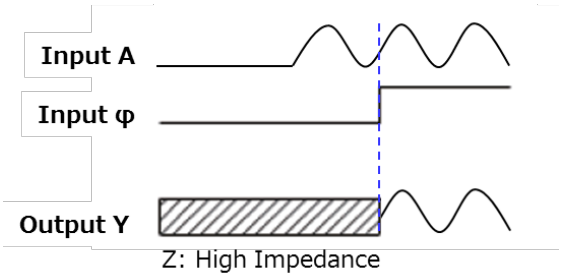


Figure 2.48 Timing chart

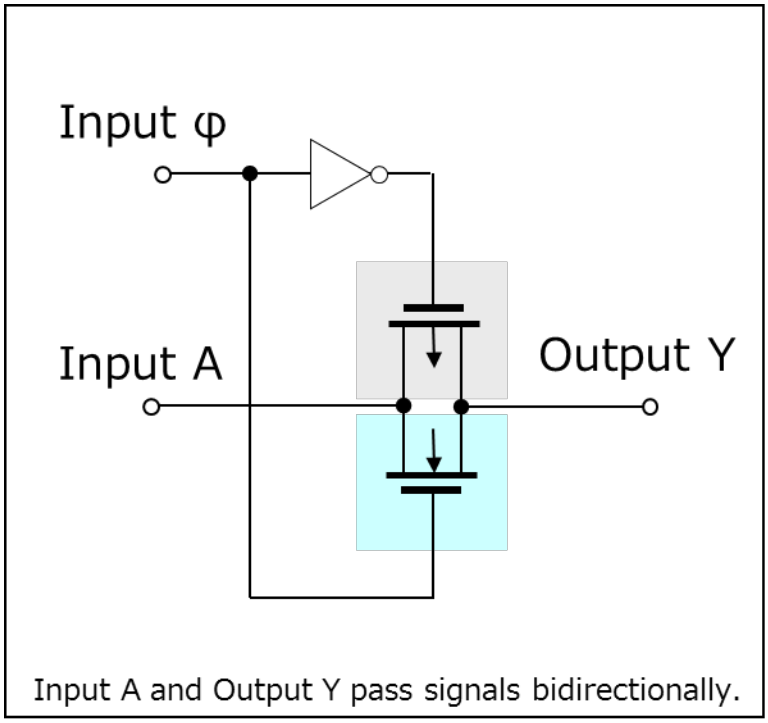


Figure 2.49 Internal circuit of analog switch

3. Conclusion

The typical applications, functions (Inverter, Buffers, Flip-flops, etc.), operations, and structures of CMOS logic ICs have been described. Please use it as a help when using CMOS logic IC.

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Compatibility with 5 V Systems	Standard	TC4000B	3 to 18	65 (@5.0V)	±0.51 (@5.0V)	-	-
	High-speed	TC74HC	2 to 6	23 (@4.5V)	±4.0 or ±6.0 (@4.5V)	-	-
		74HC*					
		TC74HCT	4.5 to 5.5			-	-
		74HCT*					
	Advanced	TC74AC	2 to 5.5	8.5 (@4.5V)	±24 (@4.5V)	-	-
		TC74ACT	4.5 to 5.5				
	Very High-speed	TC74VHC	2 to 5.5	8.5 (@4.5V)	±8.0 (@4.5V)	0 to 5.5	-
		74VHC					
		TC74VHCT	4.5 to 5.5				0 to 5.5
		74VHCT					
		TC74VHCV	1.8 to 5.5		±16 (@4.5V)		
		74VHCV					
Compatible with low-voltage systems	Low-voltage	TC74LCX	1.65 to 3.6	6.5 (@3.0V)	±24 (@3.0V)	0 to 5.5	0 to 5.5
		74LCX					
	Very Low-voltage	TC74VCX	1.2 to 3.6	4.2 (@2.3V)	±24 (@3.0V)	0 to 3.6	0 to 3.6

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