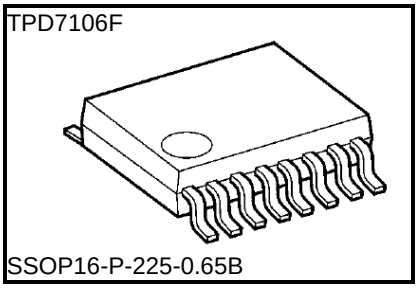
TOSHIBA Intelligent Power Device Silicon Power MOS Integrated Circuit

TPD7106F

1 channel High-Side N channel Power MOSFET Gate Driver

1. Description

TPD7106F is a 1channel high-side N channel power MOSFET gate driver. This IC contains a charge pump circuit, allowing easy configuration of a high-side switch for large-current applications.



2. Applications

- Junction Boxes for Automotive.
- Power distribution modules for Automotive.
- Semiconductor relays.

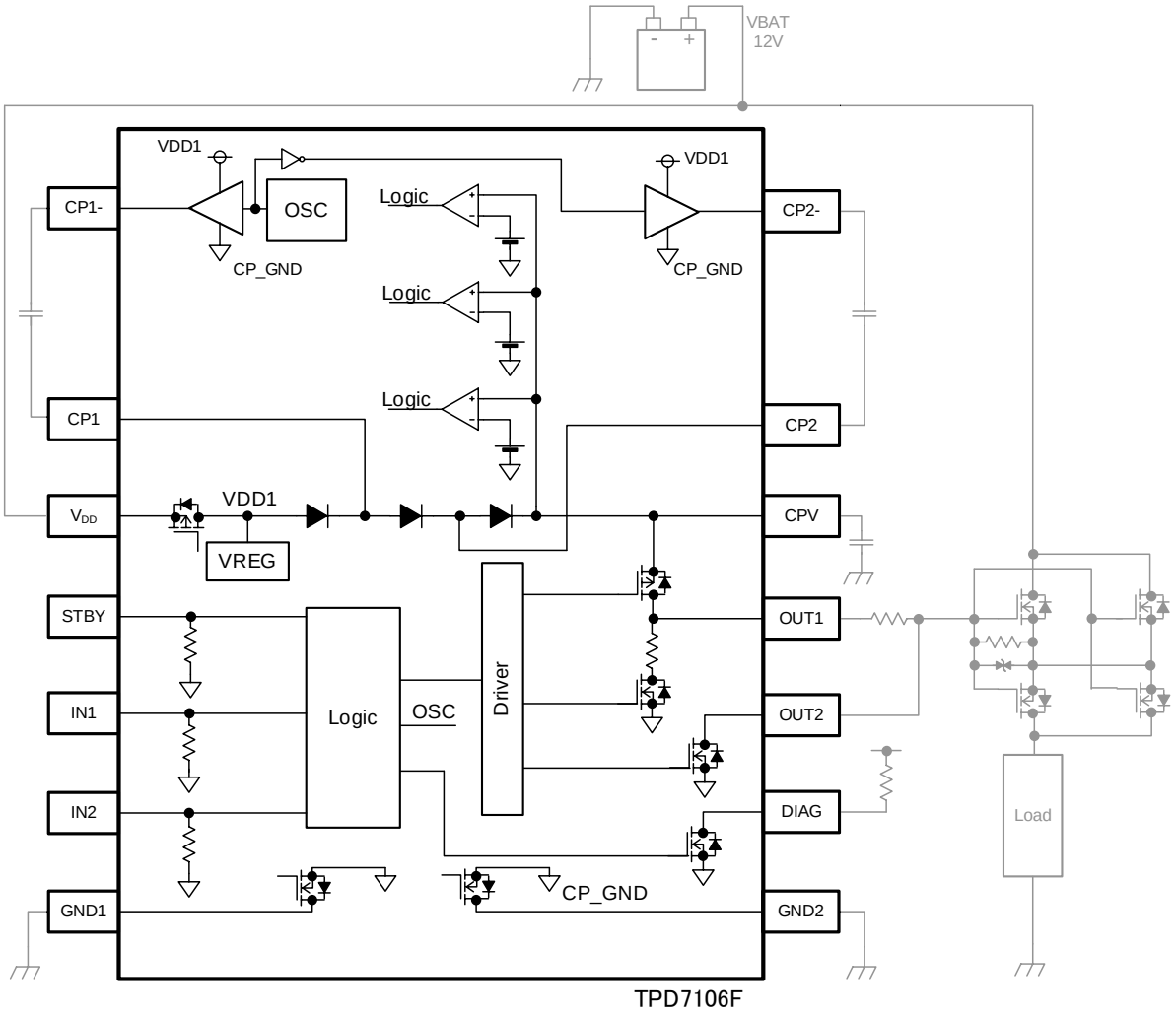
3. Features

- AEC-Q100 qualified.
- Built in the charge pump circuit (Charge pump capacitor is external).
- Output current is -10mA / +400mA, and the drive by parallel use of N channel power MOSFET is possible.
- Built in the protection for reverse connection of power supply.
- Built in the diagnosis output for under voltage of Charge pump circuit.
- SSOP16 package for surface mounting.

Note: Due to its MOS structure. This product is sensitive to static electricity.

Start of commercial production
2020-03

4. Block Diagram



Note: Some of the functional blocks, circuits or constants labels in the block diagram may have been omitted or simplified for clarity.

Figure 4.1 Block Diagram

5. Pin Assignments (top view)

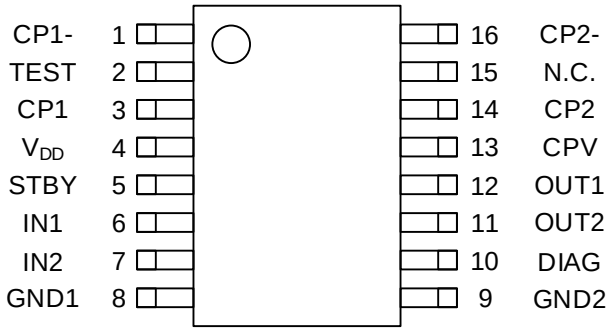


Figure 5.1 Pin Assignments

6. Pin Description

Table 6.1 Pin Description

Pin No	Symbol	Description
1	CP1-	The terminal for charge pump capacitor connection.
2	TEST	The terminal for and internal circuit test. Normal operation = connect to Ground.
3	CP1	The terminal for charge pump capacitor connection.
4	V_{DD}	Power supply pin.
5	STBY	Standby mode control pin.
6	IN1	Input pin. Built in pull down resistor.(for Normal operation)
7	IN2	Input pin. Built in pull down resistor.(for rapid off)
8	GND1	Ground pin.
9	GND2	Ground pin.
10	DIAG	Diagnostic output (Open drain).
11	OUT2	Output pin for an external N channel power MOSFET drive(for rapid off)
12	OUT1	Output pin for an external N channel power MOSFET drive(for Normal switching)
13	CPV	Output of charge pump voltage.
14	CP2	The terminal for charge pump capacitor connection.
15	N.C	No-Connect pin.
16	CP2-	The terminal for charge pump capacitor connection.

7. Operational Description

7.1. Gate drive of Power MOSFET

7.1.1. On driver

In response to FET turn-on instructions (V_{IN1}=V_{IH}), a charge pump circuit and the drive circuit operate from input terminal IN1, and it drives N channel power MOSFET of a high side with sufficient gate voltage. (V_{OUT1}=V_{DD}+12V (typ.))

- V_{IN1}: IN1 pin input voltage
- V_{IH}: High level input voltage
- V_{OUT1}: OUT1 pin output voltage

7.1.2. Off driver (Normal Off)

The OFF operation in normal turns off external FET by M2 in Figure 7.1 in response to FET drive instructions (V_{IN1}=V_{IL}) from input terminal IN1 (drive on resistance = 630Ω (typ.)).

- V_{IL}: Low level input voltage

7.1.3. Off driver (Rapid Off)

Abnormalities, such as external FET and short circuits which occurred around load, are detected, and when it is required to make external FET turn off for a short time, in response to FET rapid OFF instructions (V_{IN2}=V_{IH}), the following figure M3 operates from input terminal IN2, and it turns off external FET quickly (Driver on resistance = 5Ω (typ.)). In addition, although rapid off-driver operating time (t_{O2ON}) is a maximum of 200μs.

- V_{IN2}: IN2 pin input voltage

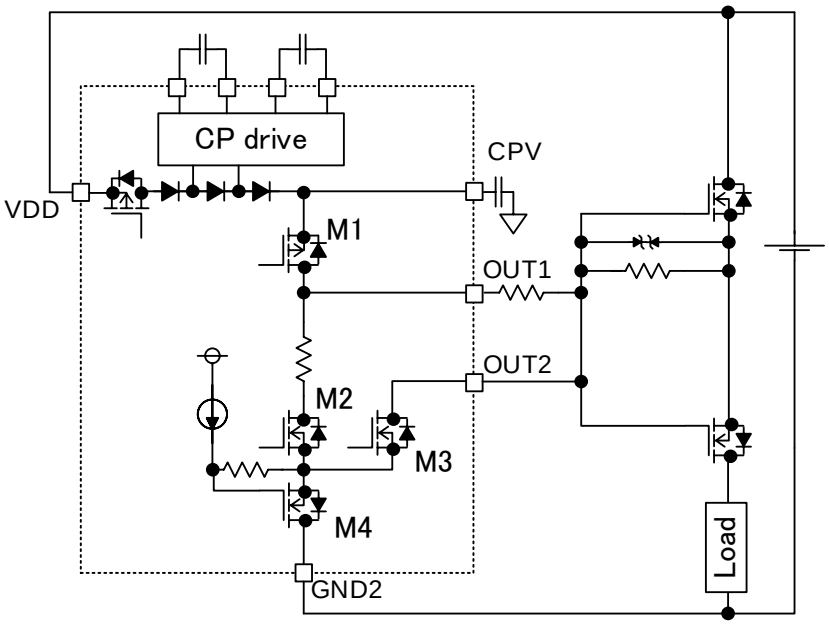


Figure 7.1 Output driver part.

Table 7.2 Truth table (1)

IN1	IN2	STBY	OUT1	OUT2	state
X	X	L	Hiz	Hiz	Stand-by mode
L	L	H	L	Hiz	Normal operation
H	L	H	H	Hiz	
L	H	H	L	L	Rapid off mode
H	H	H	L	L	

7.2. Protection for reverse connection of power supply

When a power supply is connected by reverse polarity, the current from a GND terminal is intercepted by M4 and M5, and external FET is turned off.

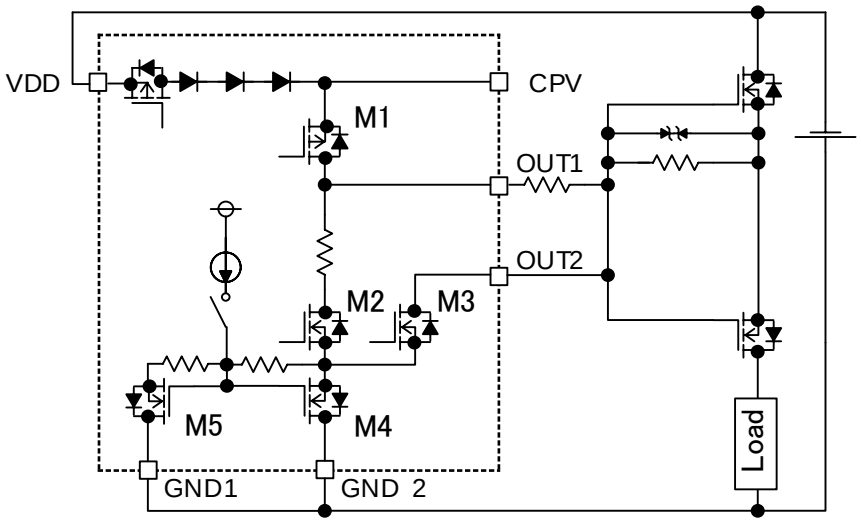


Figure 7.3 Protection for reverse connection.

7.3. Detection for under voltage of charge pump

CPV terminal voltage is supervised and a charge pump voltage fall is detected. If it becomes below the charge pump fall judging voltage VCPL, a DIAG terminal will serve as L State. Output terminal OUT1 and OUT2 maintain operation. In addition, when STBY is L State, a charge pump circuit stops.

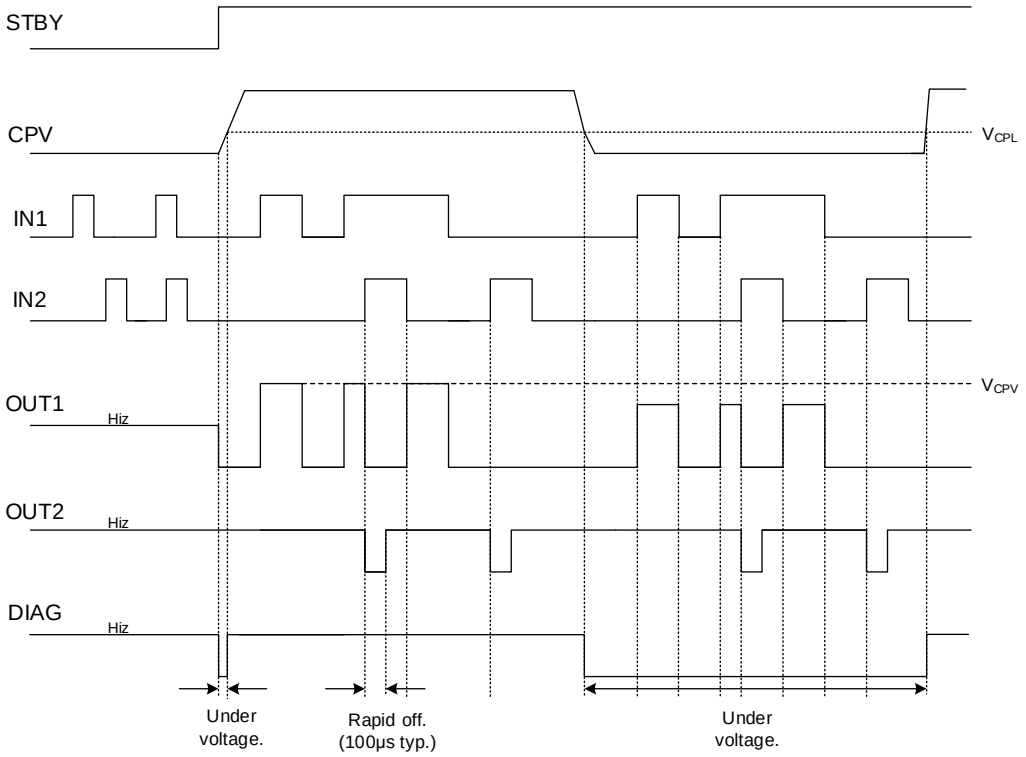


Figure 7.4 Timing chart.

Note: When STBY is momentarily made into L State from H State and it returns to H State again, even if CPV terminal voltage holds more than VCPL, a DIAG terminal may serve as L State.

7.4. Truth Table (protect function and diagnosis output)

Table 7.5 Truth table (2)

IN1	IN2	STBY	Charge pump		Rapd off drive	OUT1			OUT2		DIAG	
			V_{CPV}	Boost operation			M1 Note3	M2 Note3		M3 Note3		M6 Note3
X	X	L	V_{CPV}=L	stop	Disable	Hiz	OFF	OFF	Hiz	OFF	H (pull up)	OFF
L	L	H	$V_{CPV} \leqq V_{CPL}$	Operation	Disable	L	OFF	ON	Hiz	OFF	L	ON
H	L				Disable	H	ON	OFF	Hiz	OFF		
L	H Note1				Enable	L	OFF	ON	L	ON		
	H Note2				Disable	L	OFF	ON	Hiz	OFF		
H	H Note1				Enable	L	OFF	ON	L	ON		
	H Note2				Disable	L	OFF	ON	Hiz	OFF		
L	L		$V_{CPV} > V_{CPL}$		Disable	L	OFF	ON	Hiz	OFF	H (pull up)	OFF
H	L				Disable	H	ON	OFF	Hiz	OFF		
L	H Note1				Enable	L	OFF	ON	L	ON		
	H Note2				Disable	L	OFF	ON	Hiz	OFF		
H	H Note1				Enable	L	OFF	ON	L	ON		
	H Note2				Disable	L	OFF	ON	Hiz	OFF		

Note1: Rapid off drive operation time (100μs typ.)
Note2: After Rapid off drive.
Note3: Refer to the following figure of the device name.

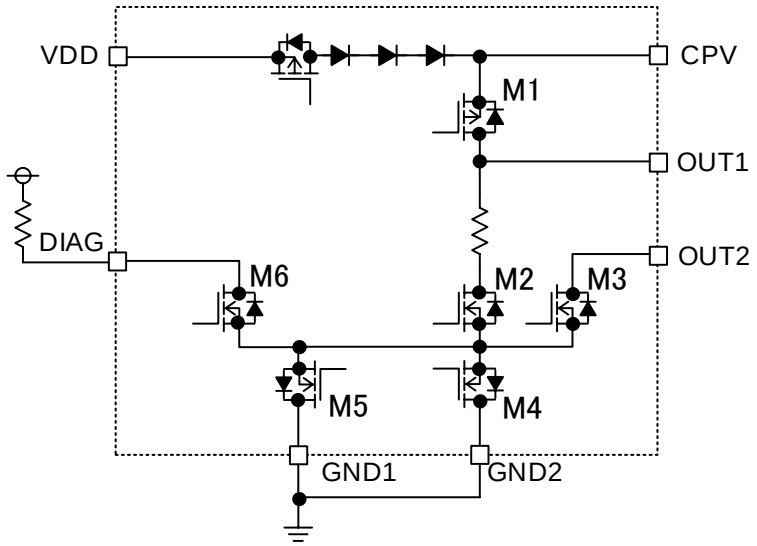


Figure 7.6 TPD7106F Output part.

8. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings

(T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit	Note
Supply voltage	DC	$V_{DD\ (1)}$	–18 to 27	V	-
	Pulse	$V_{DD\ (2)}$	40	V	t≤500ms
Input voltage(1)		V_{STBY}	–0.3 to 40.0	V	-
Input voltage(2)		V_{IN1},V_{IN2}	–0.3 to 6.0	V	-
CPV voltage		V_{CPV}	40	V	-
TEST pin voltage		V_{TEST}	40	V	-
Output source current		$I_{OUT1\ (1)}$	–10	mA	-
Output sink current		$I_{OUT1\ (2)}$	+10	mA	-
Output sink current		I_{OUT2}	+400	mA	-
DIAG Output voltage		V_{DIAG}	–0.3 to 40.0	V	-
DIAG Output current		I_{DIAG}	5	mA	-
Power dissipation		P_D	1.16	W	-
Operating temperature		T_{opr}	–40 to 150	°C	-
Junction temperature		T_j	150	°C	-
Strage temperature		T_{stg}	–55 to 150	°C	-

Note1: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.)

8.1. Thermal Resistance

Table 8.2 Thermal resistance

Charateristics	Symbol	Rating	unit
Thermal resistance(junction-to-ambient)	$R_{th\ (j–a)}$	108	°C / W

Note2: Glass epoxy board
Material: FR-4(4 layer) Board size: 76.2mmx114.3mmx1.6mm

9. Operating Ranges

Table 9.1 Operating Ranges

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Operating supply voltage	V_{DD}	T_j = -40 to 150°C	4.5	12.0	27.0	V

10. Electrical Characteristics

Table 10.1 Electrical Characteristics

(Unless otherwise specified, T_j = -40 to 150°C, V_{DD} = 4.5 to 27.0V)

Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Supply current	$I_{DD(1)}$	V_{DD}	V_{DD} = 12V, V_{STBY} = V_{IL}, T_j = 25°C	-	-	5.0	μA
	$I_{DD(2)}$	V_{DD}	$V_{IN1,2}$ = V_{IL}, V_{STBY} = V_{IH}, C1,C2 = 0.01μF	-	3.2	6.0	mA
	$I_{DD(3)}$	V_{DD}	V_{IN1} = V_{IH}, V_{STBY} = V_{IH}, C1,C2 = 0.01μF, OUT1,OUT2 = open.	-	-	6.0	mA
High level input voltage	V_{IH}	IN1,IN2, STBY	-	2.0	-	-	V
Low level input voltage	V_{IL}		-	-	-	0.8	
Input current	I_{IH}	IN1,IN2, STBY	V_{IN} = 5V, Note1	-	50	100	μA
	I_{IL}		V_{IN} = 0V	-1	-	1	
High level output voltage	V_{OH1}	OUT1	V_{DD} = 18 to 27V, C1,C2 = 0.01μF, V_{IN1} = V_{IH}, V_{STBY} = V_{IH}, I_{OUT1} = -0.1mA	V_{DD} +7.0	-	40.0	V
	V_{OH2}	OUT1	V_{DD} = 8 to 18V, C1,C2 = 0.01μF, V_{IN1} = V_{IH}, V_{STBY} = V_{IH}, I_{OUT1} = -0.1mA	V_{DD} +10.0	V_{DD} +12.0	V_{DD} +14.0	
	V_{OH3}	OUT1	V_{DD} = 4.5 to 8V, V_{IN1} = V_{IH}, V_{STBY} = V_{IH}, I_{OUT1} = -0.1mA	V_{DD} +5.4	V_{DD} +7.0	V_{DD} +14.0	
Output clamp voltage	V_{OCL}	OUT1	V_{IN1} = V_{IH}, V_{STBY} = V_{IH}, C1,C2 = 0.01μF, I_{OUT1} = +0.1mA	34	37	40	V
Low level output voltage	V_{OL1}	OUT1	V_{IN1} = V_{IL}, V_{STBY} = V_{IH}, C1,C2 = 0.01μF, I_{OUT1} = +0.1mA	-	-	0.1	V
	V_{OL2}	OUT2	V_{IN2} = V_{IH}, V_{STBY} = V_{IH}, C1,C2 = 0.01μF, I_{OUT2} = +0.1A	-	0.5	1.3	
Diagnosis output leakage current	I_{DIAGH}	DIAG	V_{IN1}=V_{IL}, V_{DIAG}=5V	-	-	1	μA
Diagnosis output voltage	V_{DIAGL}	DIAG	V_{STBY} = V_{IH}, I_{DIAG} = 500μA	-	0.22	0.40	V
Charge pump frequency	f_{OSC}	CP1, CP2	V_{STBY} = V_{IH}	30	55	80	kHz
Charge pump under voltage detection voltage	V_{CPL}	CPV	V_{IN1} = V_{IH}, V_{STBY} = V_{IH}	V_{DD} +4.0	V_{DD} +4.7	V_{DD} +5.4	V
Charge pump under voltage Hysteresis	ΔV_{CPL}	CPV		0.25	0.50	1.00	V
Output driver on resistance	R_{ONH}	OUT1	V_{IN1} = V_{IH}, V_{STBY} = V_{IH},I_{OUT1} = -5mA	-	16	40	Ω
	R_{ONL1}	OUT1	V_{IN1} = V_{IL}, V_{STBY} = V_{IH},I_{OUT1} = +5mA	-	630	800	
	R_{ONL2}	OUT2	V_{IN2} = V_{IH}, V_{STBY} = V_{IH},I_{OUT2} = +0.1A	-	5	13	

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Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Switching time	t_{ON}	IN1, OUT1	Refer to test circuit 1, T_j=25°C	-	0.1	0.5	ms
	t_{OFF1}			-	0.4	0.5	
	t_{OFF2}	IN2, OUT2	Refer to test circuit 2, T_j=25°C	-	10	15	μs
Rapid off drive operation time	t_{O2ON}	IN2, OUT2	T_j=25°C	50	100	200	μs
Output current in reverse connection	I_{REV1}	OUT1	Refer to test circuit 3 V_{DD}=-4.5 to -18V	-10	-	-	μA
	I_{REV2}	OUT2		-10	-	-	μA

Note1: Built in pull down resistance 100kΩ(typ.).
Note2: Typical value is V_{DD}=12V and T_j=25°C condition.

11. Test Circuit

11.1. Test circuit 1

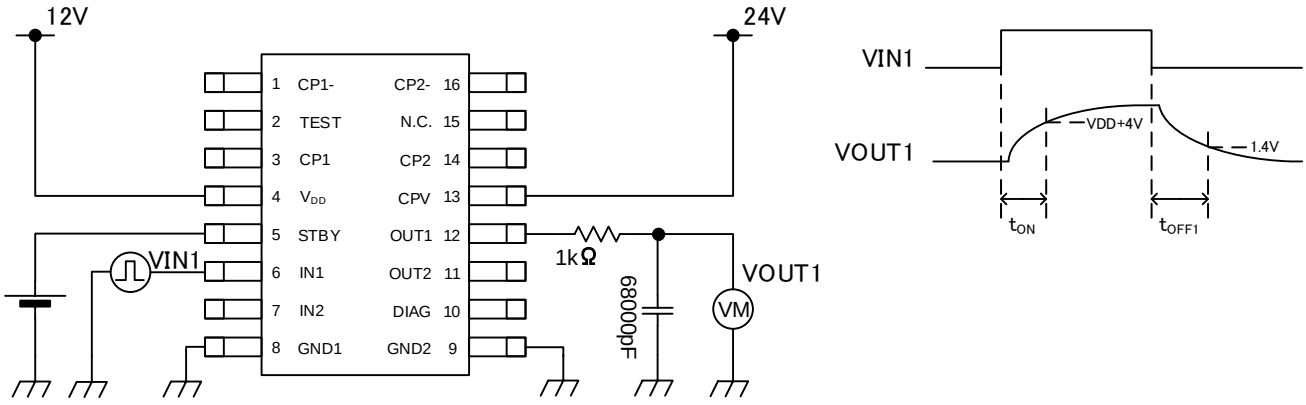


Figure 11.1　Switching time measurement circuit (1)

11.2. Test circuit 2

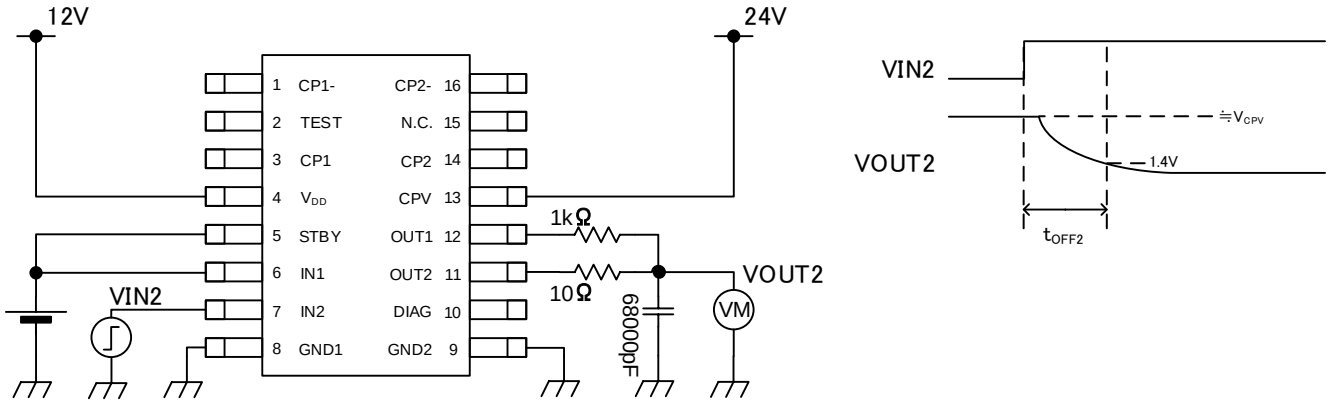


Figure 11.2　Switching time measurement circuit (2)

11.3. Test circuit 3

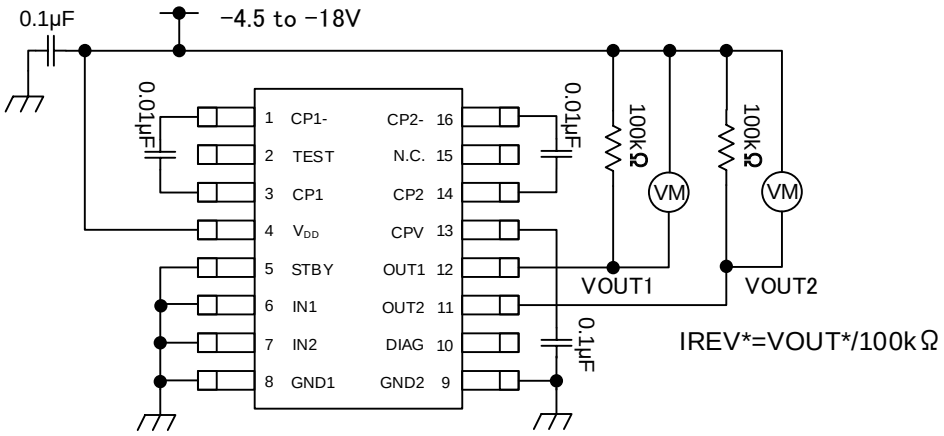


Figure 11.3 Output current in reverse connection measurement circuit

12. Characteristic curves

The below characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

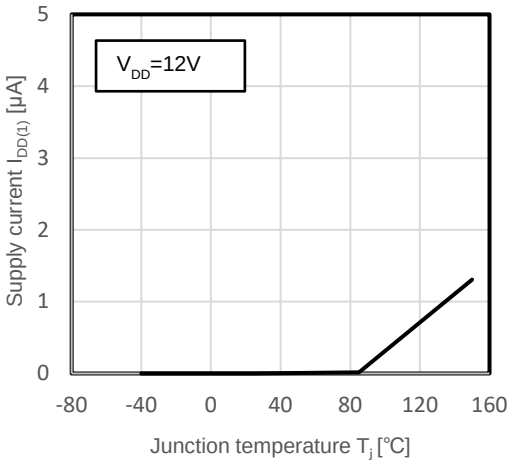


Figure 12.1 $I_{DD(1)}$ - T_j

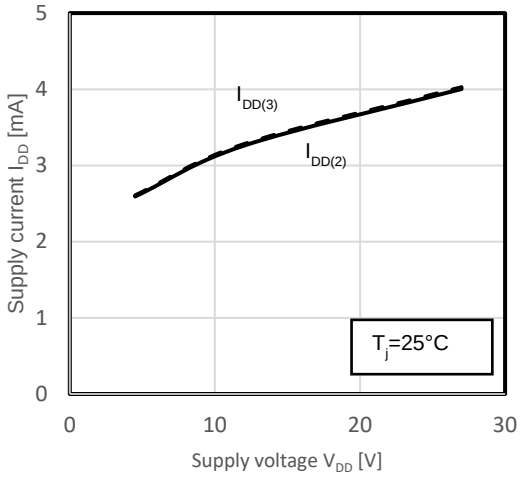


Figure 12.2 I_{DD} - V_{DD}

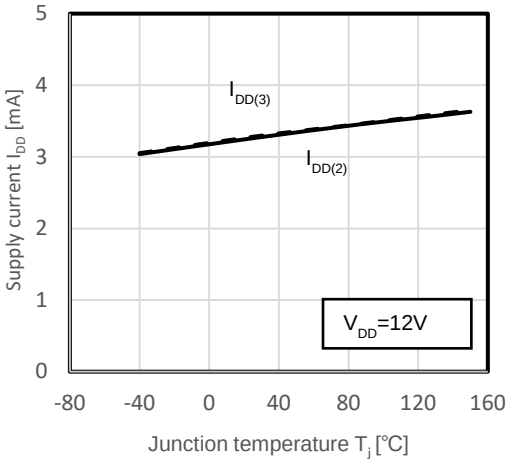


Figure 12.3 I_{DD} - T_j

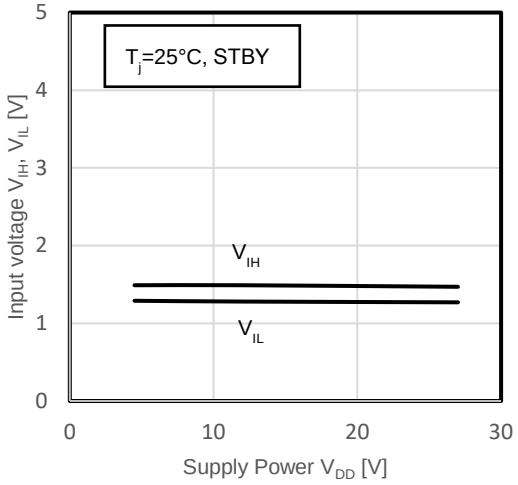


Figure 12.4 V_{IH},V_{IL} - V_{DD}

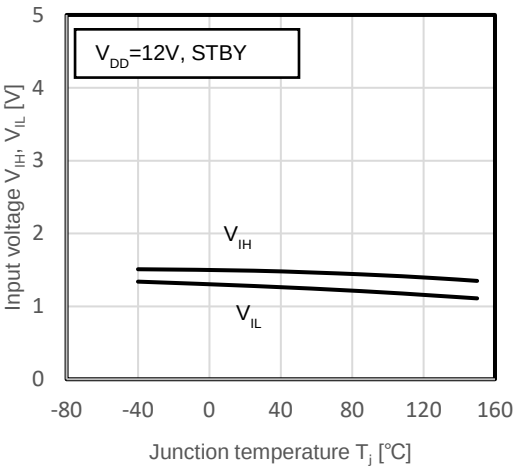


Figure 12.5 V_{IH},V_{IL} - T_j

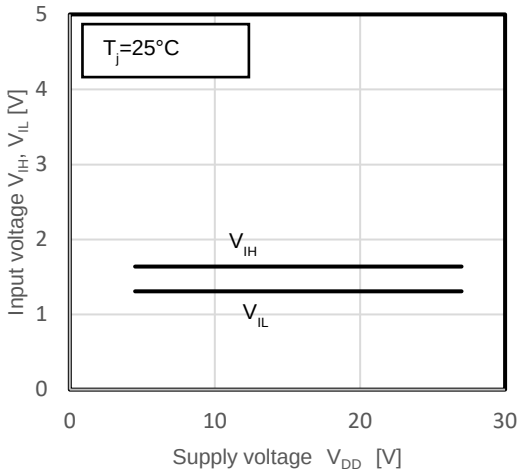


Figure 12.6 V_{IH},V_{IL} - V_{DD}

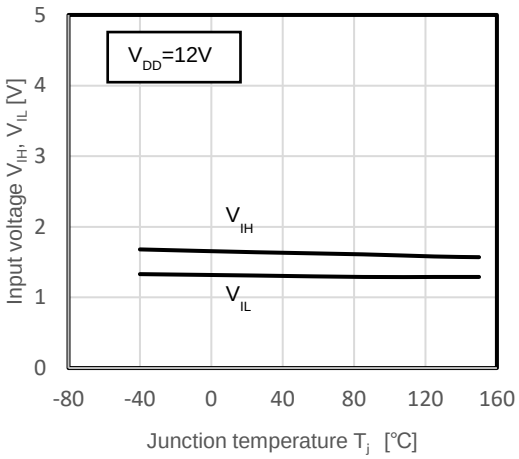


Figure 12.7 V_{IH},V_{IL} - T_j

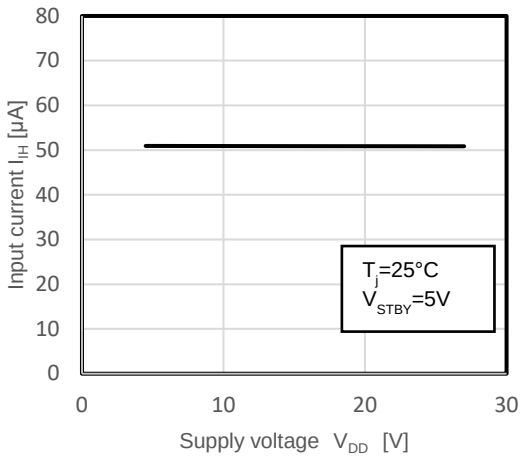


Figure 12.8 I_{IH} - V_{DD}

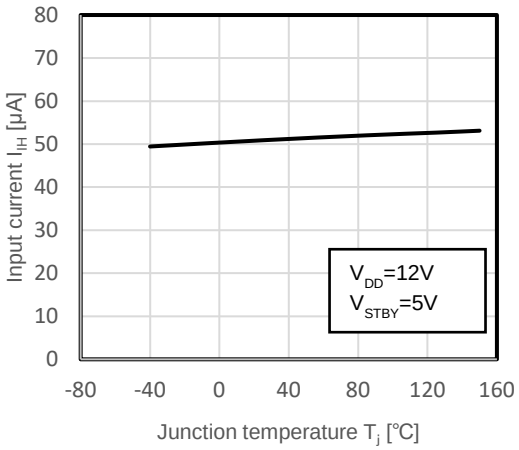


Figure 12.9 I_{IH} - T_j

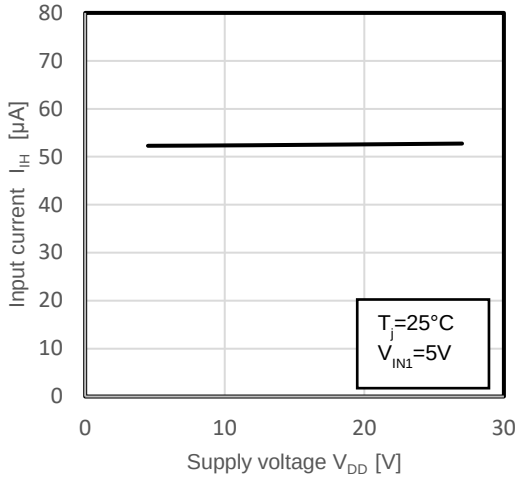


Figure 12.10 I_{IH} - V_{DD}

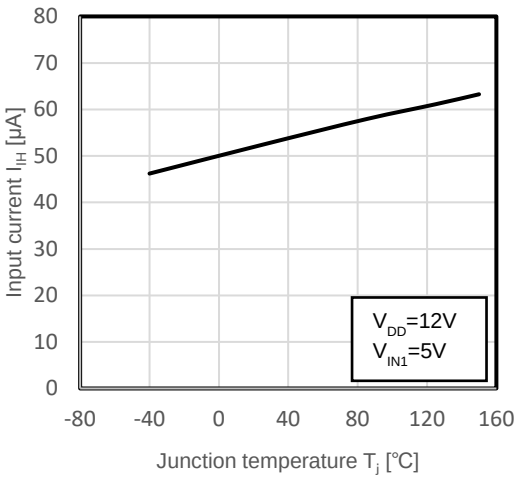


Figure 12.11 I_{IH} - T_j

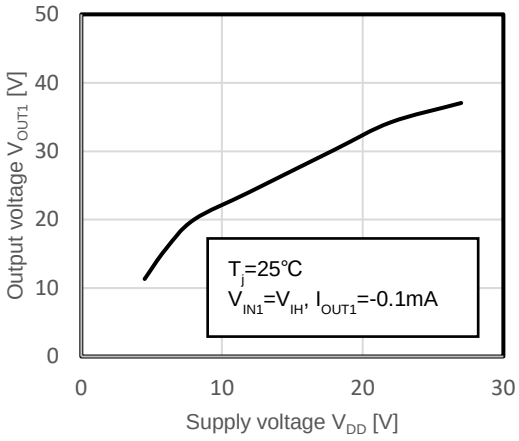


Figure 12.12 V_{OUT1} - V_{DD}

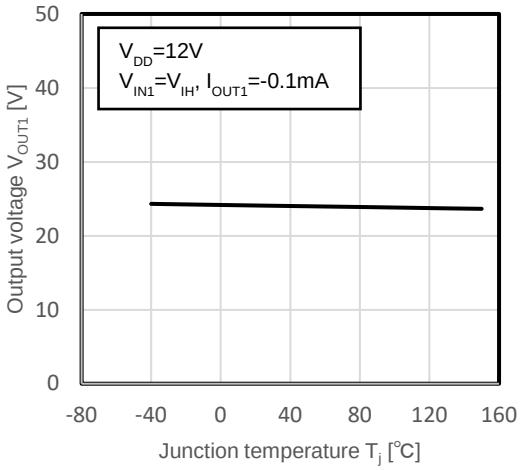


Figure 12.13 V_{OUT1} - T_j

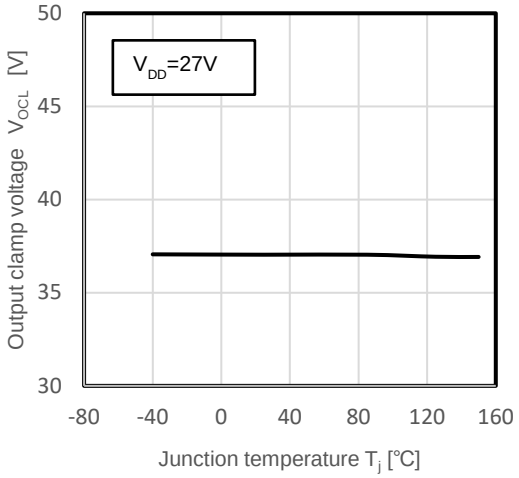


Figure 12.14 V_{OCL} - T_j

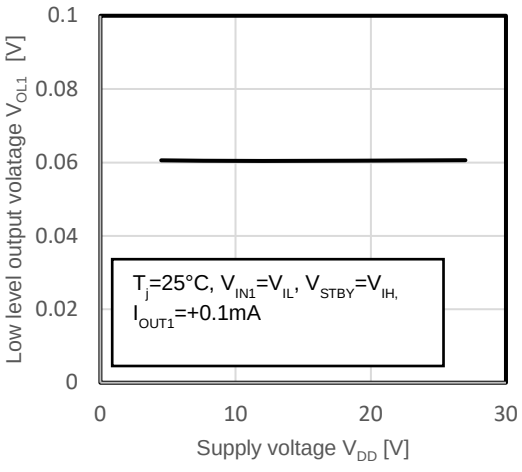


Figure 12.15 V_{OL1} - V_{DD}

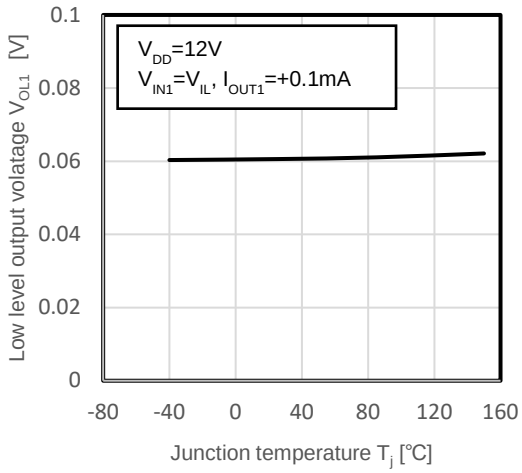


Figure 12.16 V_{OL1} - T_j

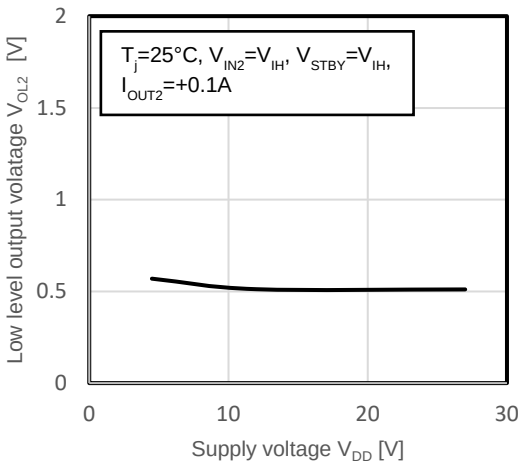


Figure 12.17 V_{OL2} - V_{DD}

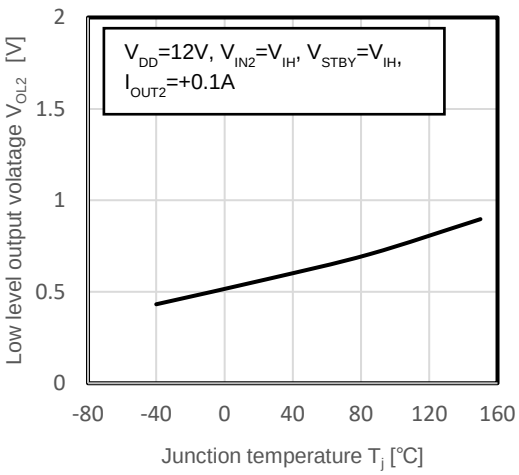


Figure 12.18 V_{OL2} - T_j

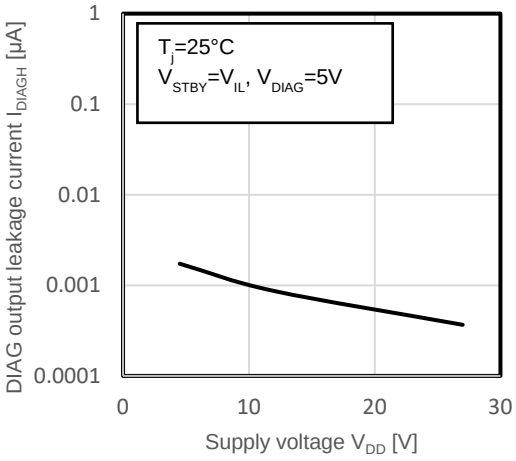


Figure 12.19 I_{DIAGH} - V_{DD}

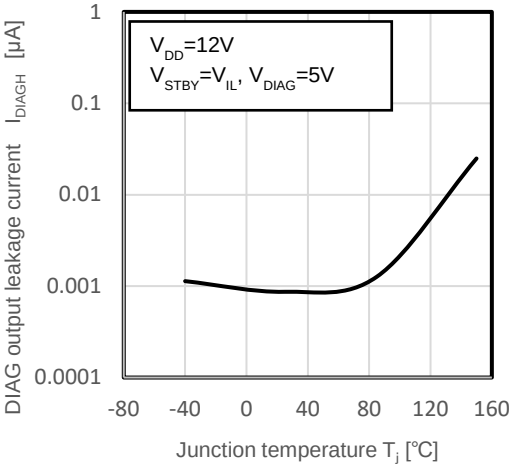


Figure 12.20 I_{DIAGH} - T_j

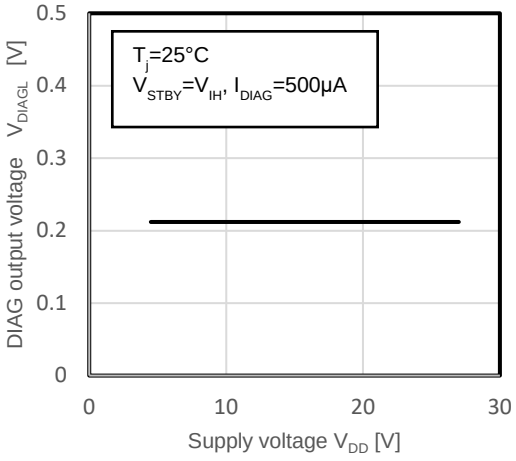


Figure 12.21 I_{DIAGL} - V_{DD}

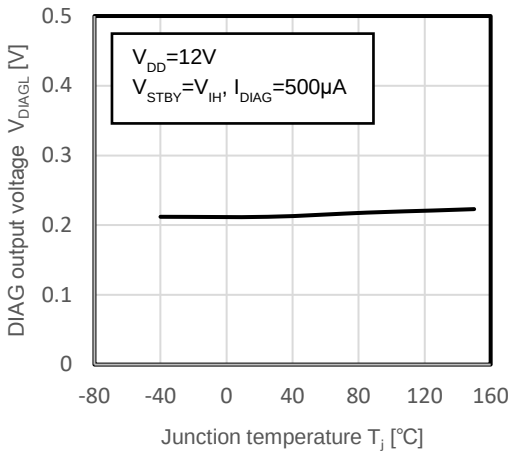


Figure 12.22 I_{DIAGL} - T_j

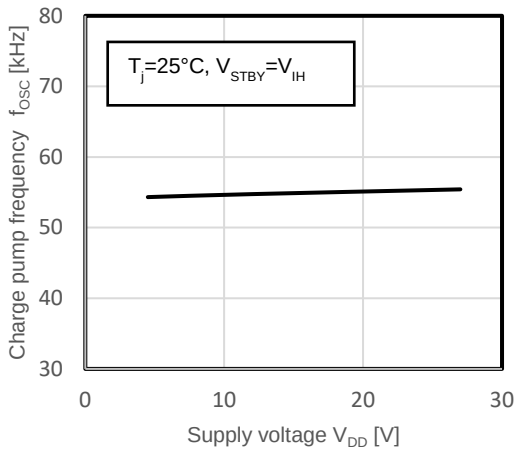


Figure 12.23 f_{OSC} - V_{DD}

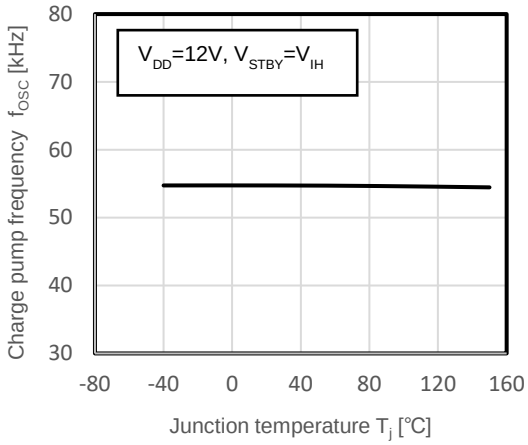


Figure 12.24 f_{OSC} - T_j

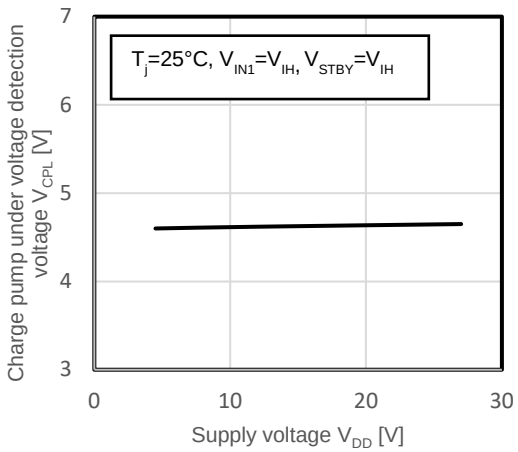


Figure 12.25 V_{CPL} - V_{DD}

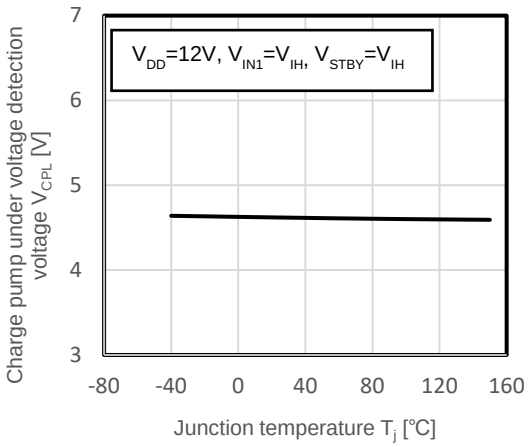


Figure 12.26 V_{CPL} - T_j

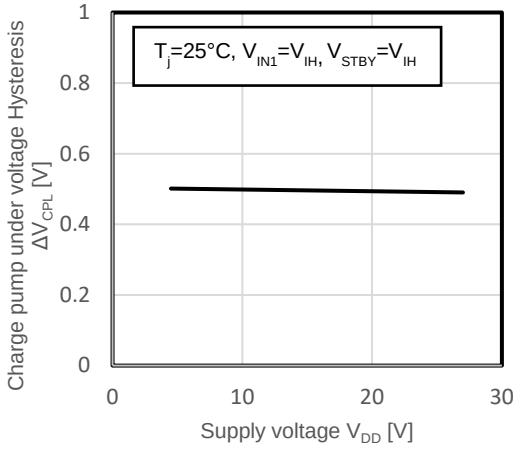


Figure 12.27 ΔV_{CPL} - V_{DD}

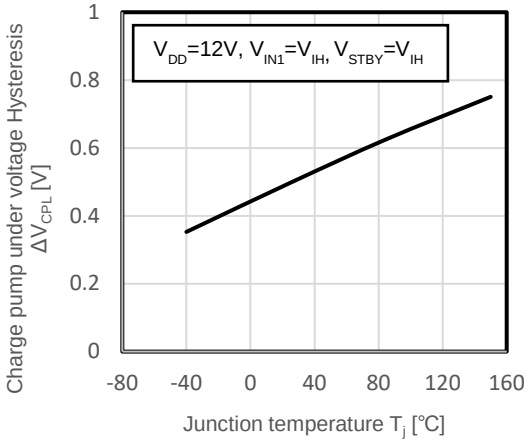


Figure 12.28 ΔV_{CPL} - T_j

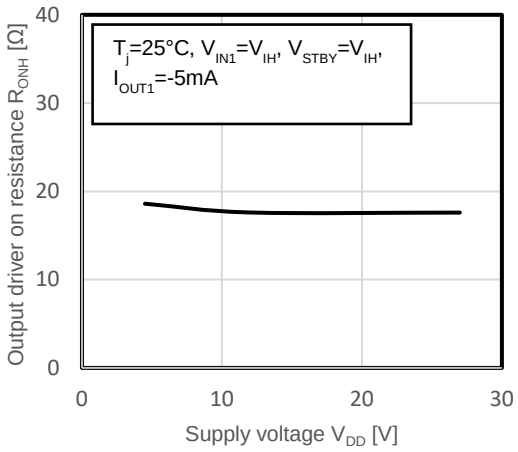


Figure 12.29 R_{ONH} - V_{DD}

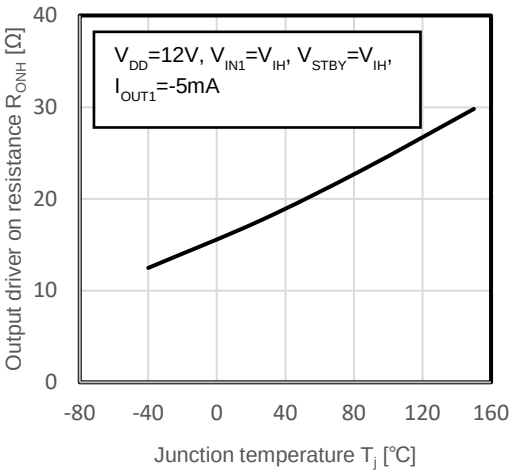


Figure 12.30 R_{ONH} - T_j

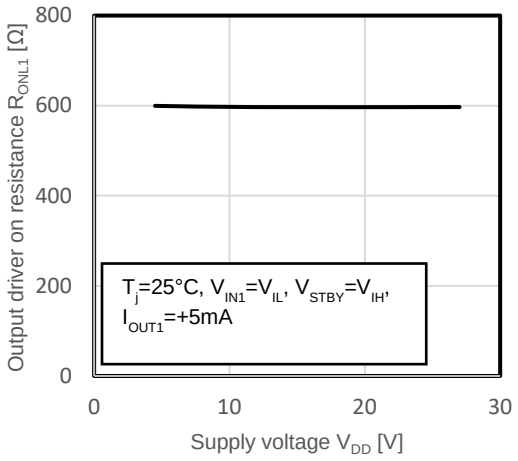


Figure 12.31 R_{ONL1} - V_{DD}

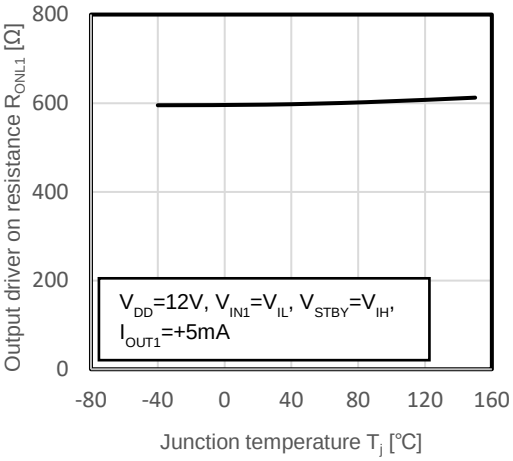


Figure 12.32 R_{ONL1} - T_j

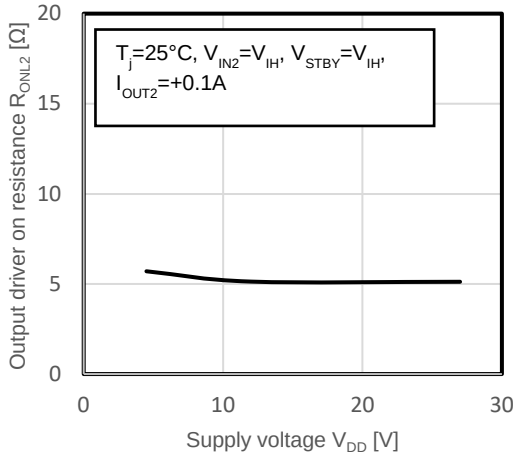


Figure 12.33 R_{ONL2} - V_{DD}

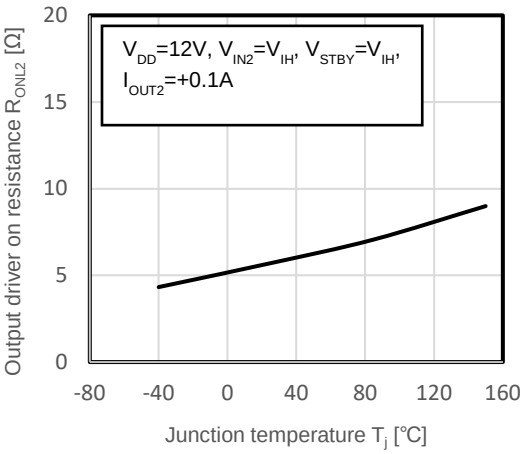


Figure 12.34 R_{ONL2} - T_j

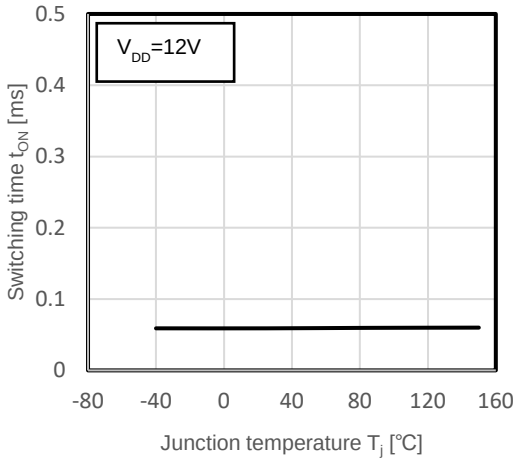


Figure 12.35 t_{ON} - T_j

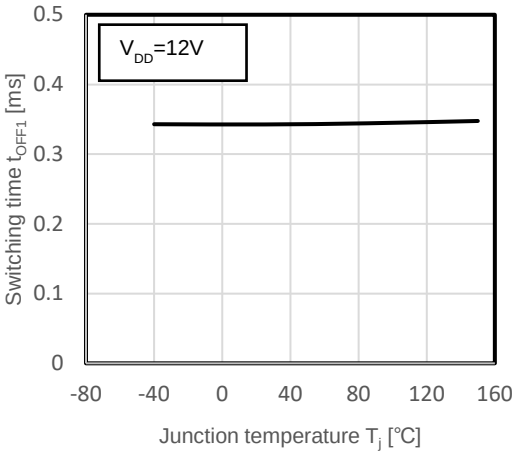


Figure 12.36 t_{OFF1} - T_j

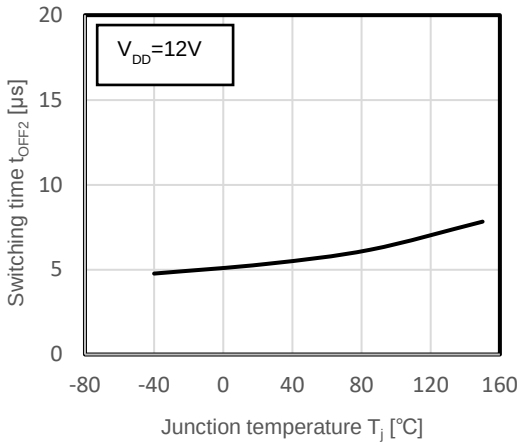


Figure 12.37 t_{OFF2} - T_j

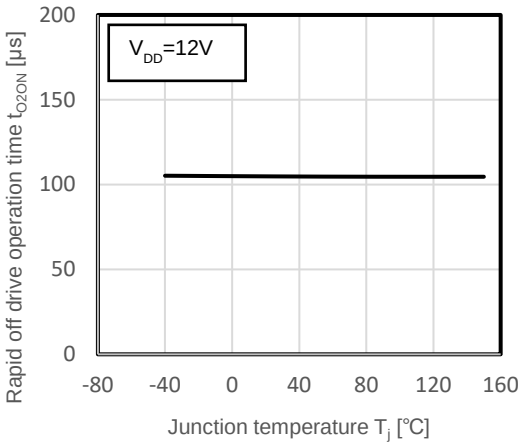


Figure 12.38 t_{O2ON} - T_j

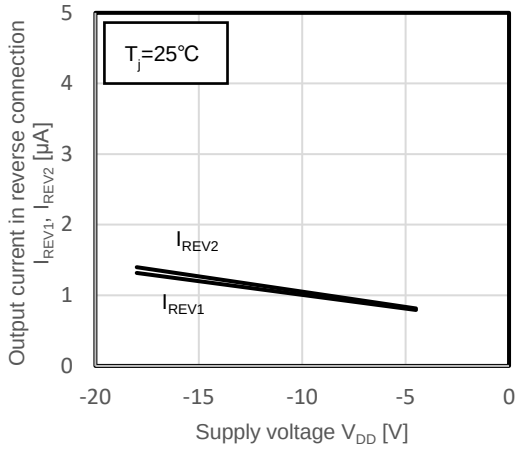


Figure 12.39 I_{REV1}, I_{REV2} - V_{DD}

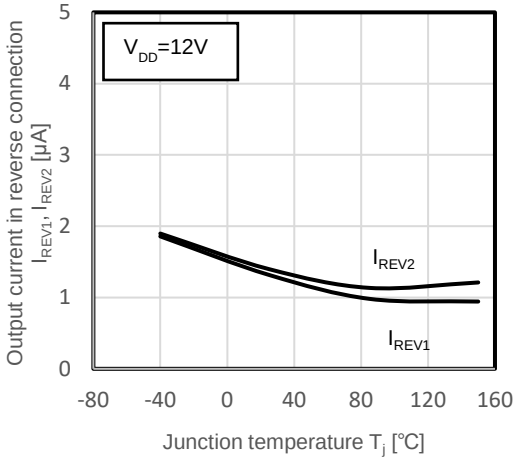
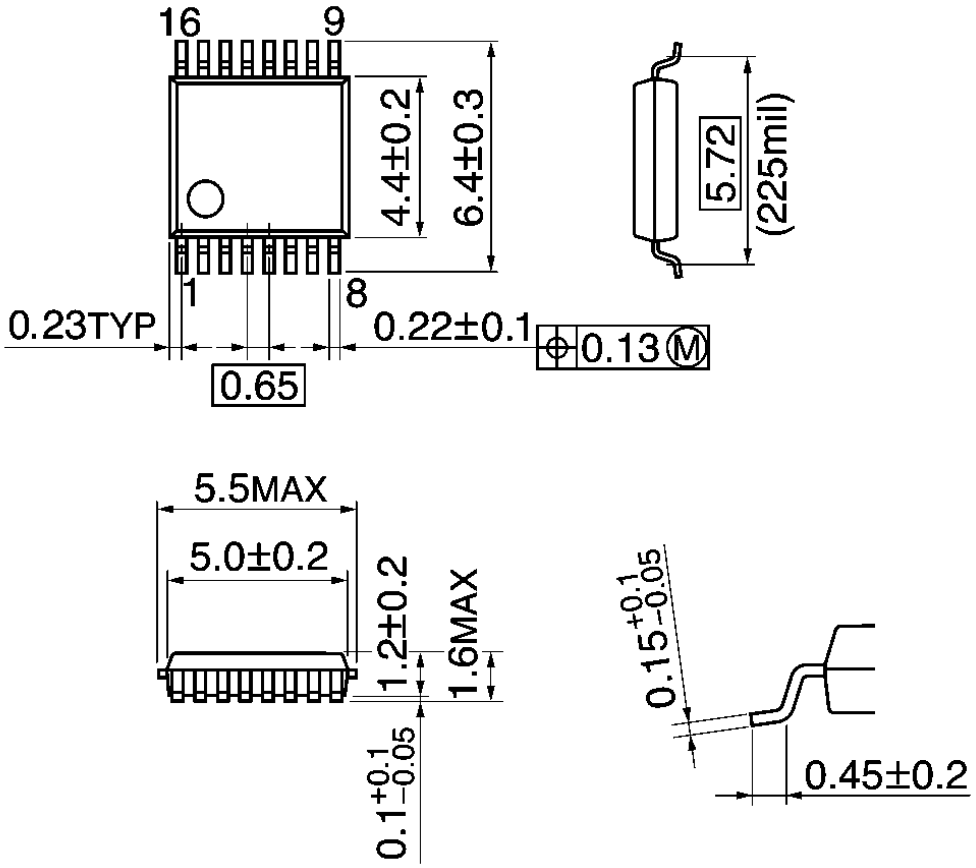


Figure 12.40 I_{REV1}, I_{REV2} - T_j

13. Package Information

13.1. Package Dimensions

Unit: mm



Weight: 0.074 g (typ.)

Figure 13.1 Package Dimensions

13.2. Marking

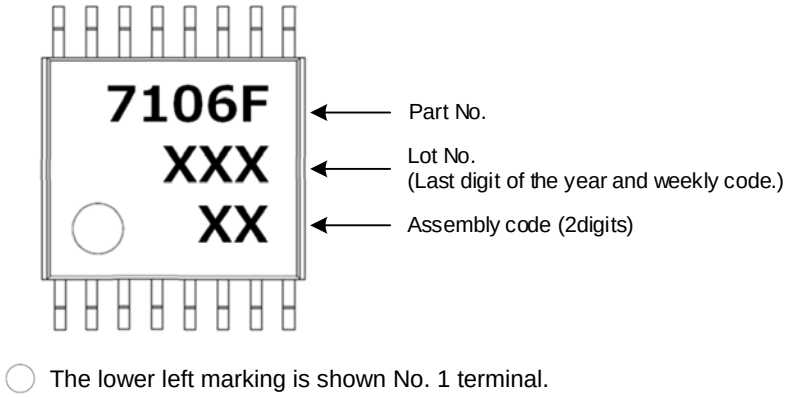


Figure 13.2 Marking

13.3. Land Pattern Dimensions for Reference only

Unit: mm

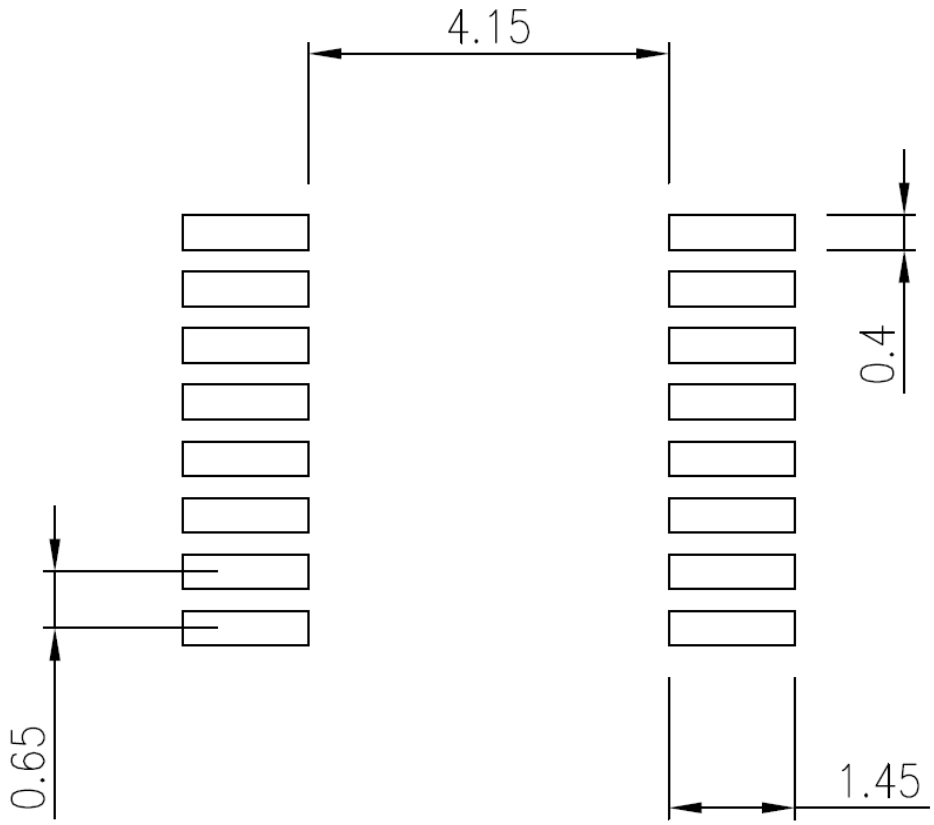


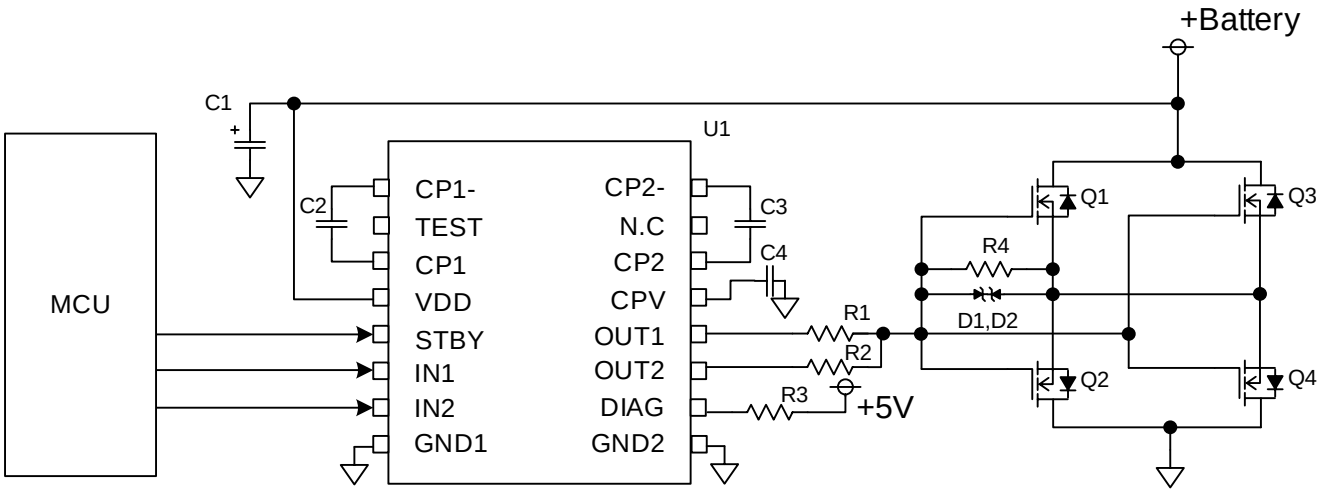
Figure 13.3 Land Pattern Dimensions for Reference only

14. IC Usage Considerations

14.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.
(2) Immediately after power activation, by the constant of external elements, since a pulse may occur in a DIAG output signal, please do not use the DIAG output signal immediately after power activation for diagnosis of operation of a product.

15. Application Circuit Example



- U1: TPD7106F
- Q1,Q2,Q3,Q4: N channel power MOSFET/40V
- D1,D2: CRZ16
- R1: 1kΩ
- R2: 10Ω
- R3: 10kΩ
- R4: 200kΩ
- C1: 10μF/50V
- C2,C3: 0.1μF/50V
- C4: 1μF/50V

Figure 15.1 Application Circuit Example

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