

MOSFETs Silicon P-Channel MOS (U-MOSVI)

# SSM6J501NU

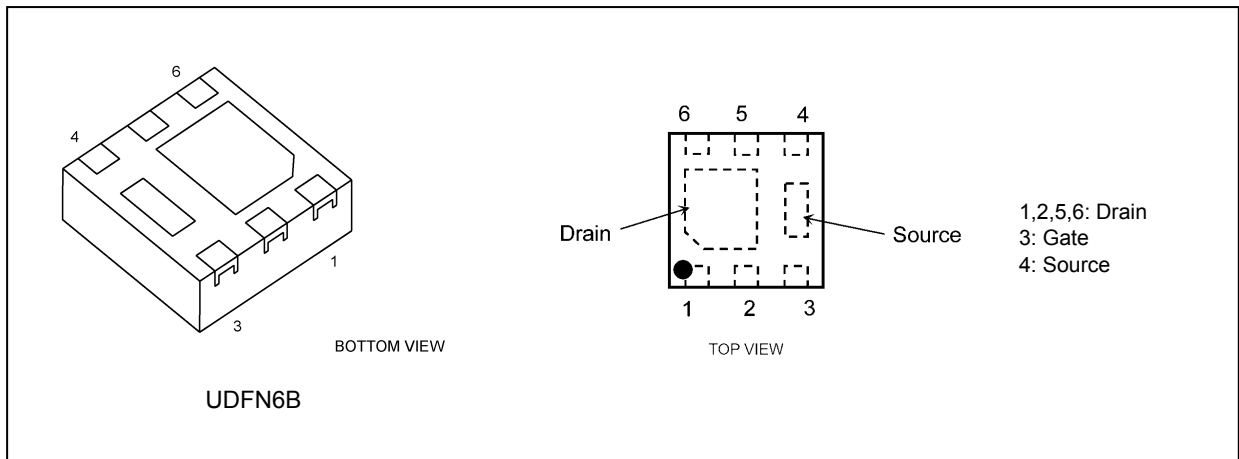
## 1. Applications

- Power Management Switches

## 2. Features

- (1) 1.5-V drive
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 43 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.5 \text{ V}$ )
  - $R_{DS(ON)} = 26.5 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.8 \text{ V}$ )
  - $R_{DS(ON)} = 19 \text{ m}\Omega$  (max) (@ $V_{GS} = -2.5 \text{ V}$ )
  - $R_{DS(ON)} = 15.3 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.5 \text{ V}$ )

## 3. Packaging and Pin Assignment



Start of commercial production  
2010-11

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	-20	V
Gate-source voltage	$V_{GSS}$	$\pm 8$	V
Drain current (DC) (Note 1), (Note 4)	$I_D$	-10	A
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	-30	
Power dissipation (Note 3)	$P_D$	1.25	W
Power dissipation $t \leq 10\text{ s}$ (Note 3)		2.5	
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$

Note 2: Pulse width (PW)  $\leq 10\text{ ms}$ , duty  $\leq 1\%$

Note 3: Device mounted on a FR4 board. (25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu Pad : 645 mm<sup>2</sup>)

Note 4: The maximum current rating is package limited.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-ambient thermal resistance (Note 3)	$R_{th(ch-a)}$	100	$^\circ\text{C/W}$

### 6. Electrical Characteristics

#### 6.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	—	—	-1	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0\text{ V}$	-20	—	—	V
Drain-source breakdown voltage (Note 5)	$V_{(BR)DSX}$	$I_D = -1\text{ mA}, V_{GS} = 5\text{ V}$	-15	—	—	V
Gate threshold voltage (Note 6)	$V_{th}$	$V_{DS} = -3\text{ V}, I_D = -1\text{ mA}$	-0.3	—	-1.0	V
Drain-source on-resistance (Note 7)	$R_{DS(ON)}$	$I_D = -4.0\text{ A}, V_{GS} = -4.5\text{ V}$	—	12	15.3	m $\Omega$
		$I_D = -4.0\text{ A}, V_{GS} = -2.5\text{ V}$	—	14	19	
		$I_D = -4.0\text{ A}, V_{GS} = -1.8\text{ V}$	—	17	26.5	
		$I_D = -2.0\text{ A}, V_{GS} = -1.5\text{ V}$	—	20	43	
Forward transfer admittance (Note 7)	$ Y_{fs} $	$V_{DS} = -3\text{ V}, I_D = -2.0\text{ A}$	11	22	—	S

Note 5: If a forward bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 6: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (-1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 7: Pulse measurement.

#### 6.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	2600	—	pF
Reverse transfer capacitance	$C_{rss}$		—	280	—	
Output capacitance	$C_{oss}$		—	290	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = -10\text{ V}, I_D = -2.0\text{ A},$ $V_{GS} = 0\text{ to }-2.5\text{ V}, R_{GS} = 4.7\text{ }\Omega$ Duty $\leq 1\%$ , Input: $t_r, t_f < 5\text{ ns}$ Common source, See Chapter 6.3.	—	45.2	—	ns
Switching time (turn-off time)	$t_{off}$		—	201	—	

#### 6.3. Switching Time Test Circuit

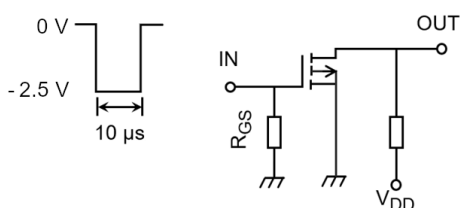


Fig. 6.3.1 Switching Time Test Circuit

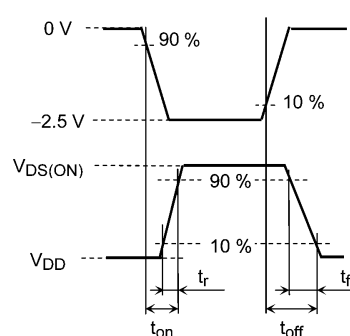


Fig. 6.3.2 Input Waveform/Output Waveform

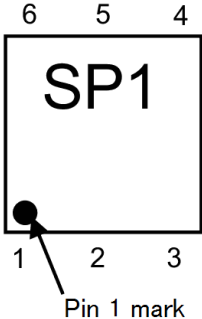
#### 6.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = -10\text{ V}, I_D = -10\text{ A},$ $V_{GS} = -4.5\text{ V}$	—	29.9	—	nC
Gate-source charge 1	$Q_{gs1}$		—	3.0	—	
Gate-drain charge	$Q_{gd}$		—	5.6	—	

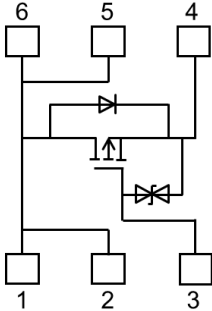
6.5. Source-Drain Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 7)	$V_{DSF}$	$I_{DR} = 4\text{ A}$ , $V_{GS} = 0\text{ V}$	—	0.7	1.1	V

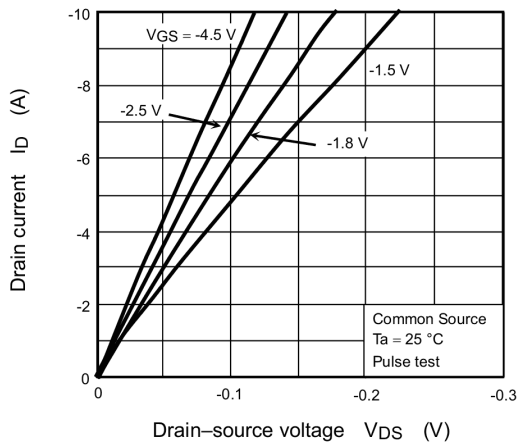
7. Marking



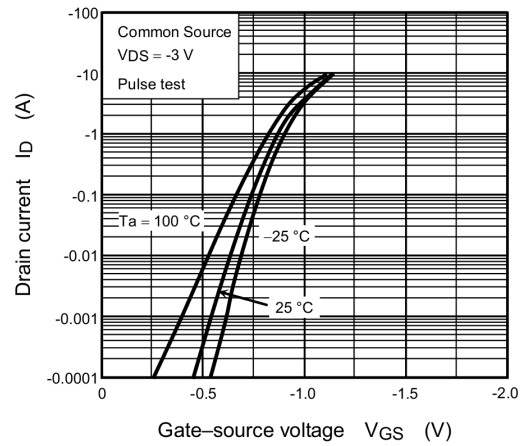
8. Internal Circuit



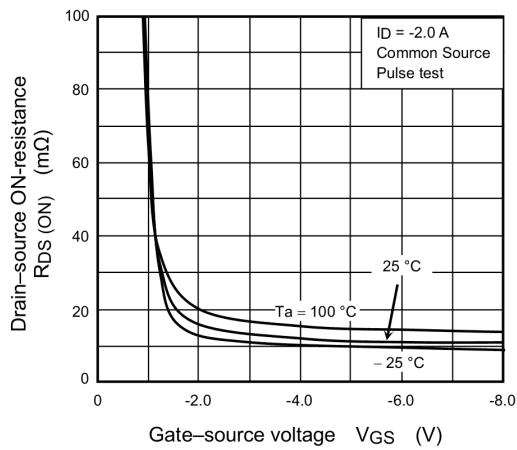
### 9. Characteristics Curves (Note)



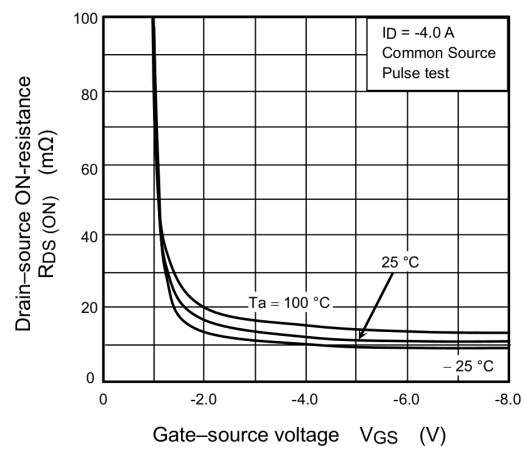
**Fig. 9.1**  $I_D - V_{DS}$



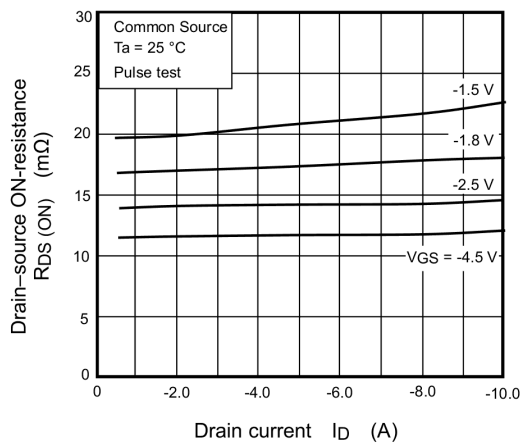
**Fig. 9.2**  $I_D - V_{GS}$



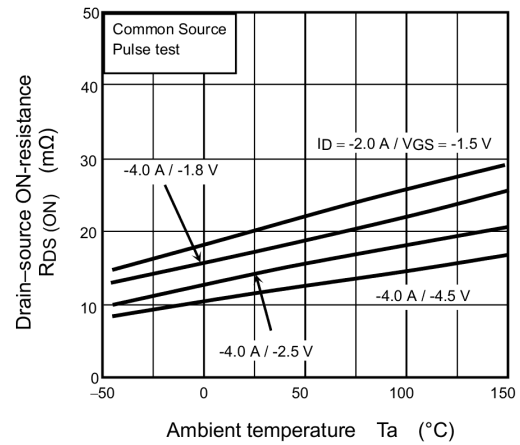
**Fig. 9.3**  $R_{DS(ON)} - V_{GS}$



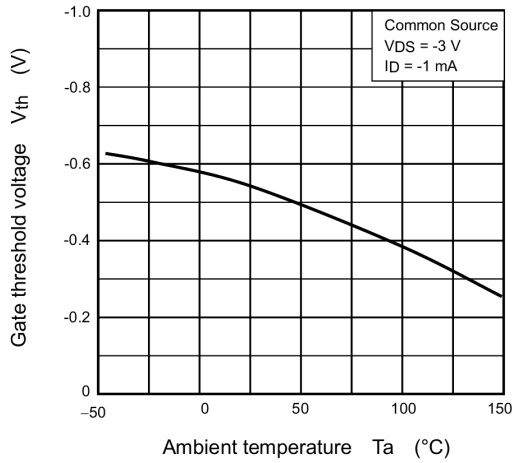
**Fig. 9.4**  $R_{DS(ON)} - V_{GS}$



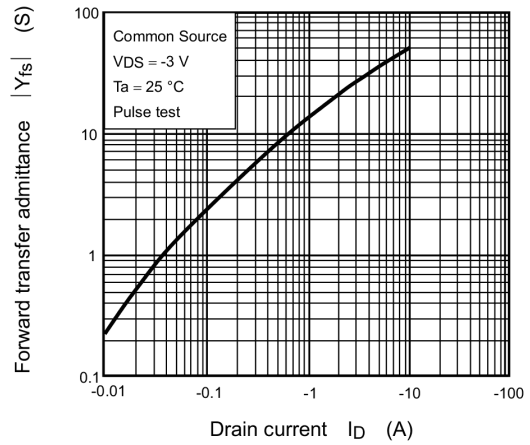
**Fig. 9.5**  $R_{DS(ON)} - I_D$



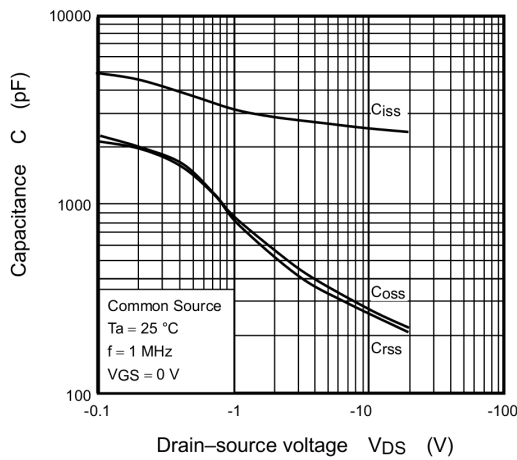
**Fig. 9.6**  $R_{DS(ON)} - T_a$



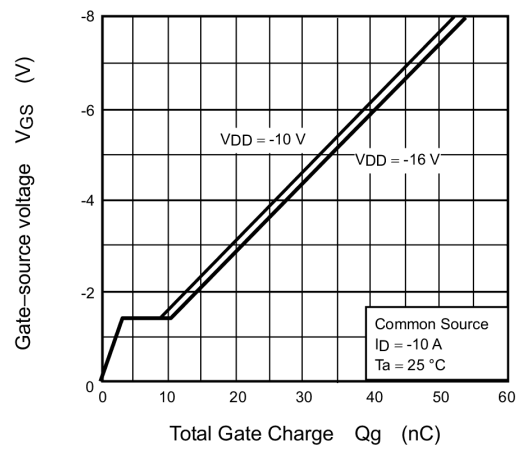
**Fig. 9.7  $V_{th} - T_a$**



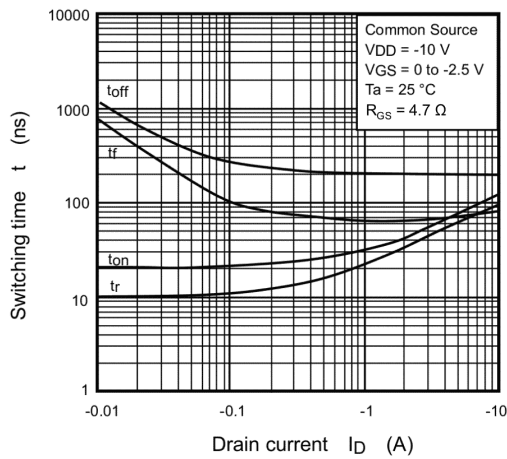
**Fig. 9.8  $|Y_{fs}| - I_D$**



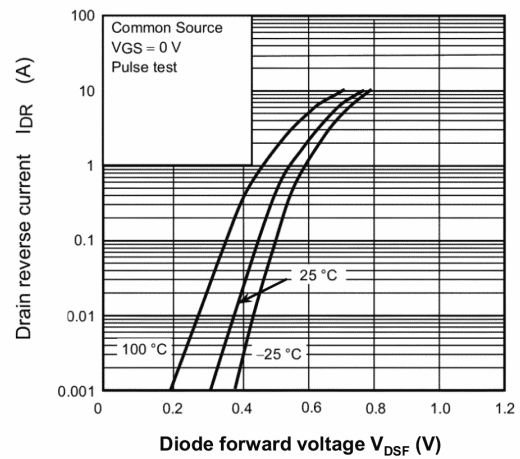
**Fig. 9.9  $C - V_{DS}$**



**Fig. 9.10 Dynamic Input Characteristics**



**Fig. 9.11  $t - I_D$**



**Fig. 9.12  $I_{DR} - V_{DSF}$**

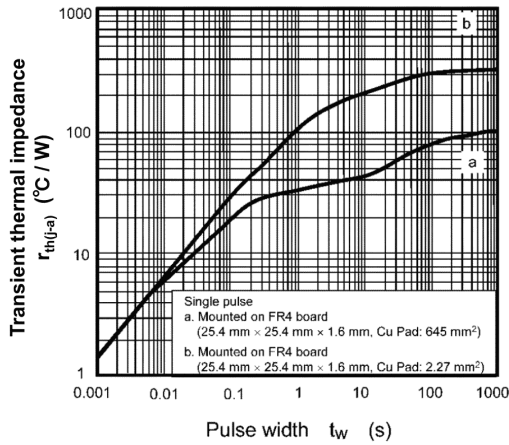


Fig. 9.13  $r_{th(j-a)} - t_w$

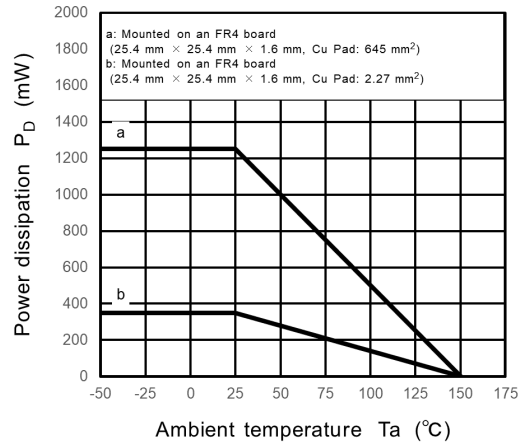


Fig. 9.14  $P_D - T_a$

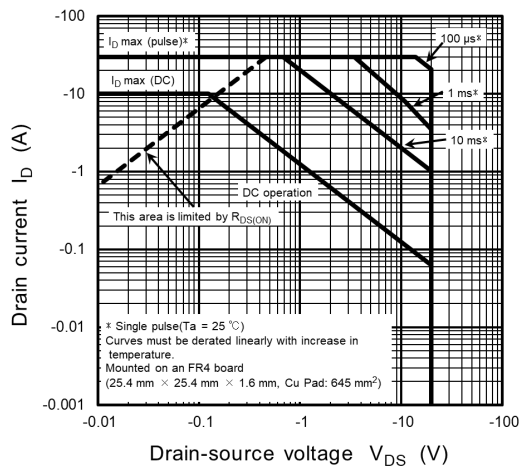


Fig. 9.15 Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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