M4K Group (1) Application Note Startup (CMSIS System & Clock Configuration)

Outlines

This application note describes the operation of the CMSIS System & Clock Configuration. This application note is a reference material for developing products using each function of M4K Group (1). This document helps the user check operation of the product and develop its program.

Table of Contents

Outlines 1
Table of Contents 2
1. Preface 4
2. Reference Document 4
3. Function to Use 4
4. Target Device 4
5. Operation Confirmation Condition 5
6. Outlines of Function 5
6.1. Watchdog Timer Setting 5
6.2. Clock Generator Setting 5
7. Startup and “system” File 6
7.1. Outlines of Operation 6
7.2. Watchdog Timer Setting 6
7.3. Clock Setting 6
7.4. PLL Setting 7
7.5. Change of Clock Frequency 7
8. Points to Remember on Handling of Sample Programs 8
9. Revision History 8
RESTRICTIONS ON PRODUCT USE 9

1. Preface

The initial settings should be done when the sample program is executed.
The settings of the watchdog timer and the clocks are done.

In this sample program, the watchdog timer is supposed to be disabled (invalid) after the reset deassertion.
For the details, refer to “Clock Control and Operation Mode” and “Clock Selection Watchdog Timer” in the Reference manual.

2. Reference Document

1. Datasheet
   TMPM4K Group (1) datasheet Rev2.0 (Japanese edition)
2. Reference manual
   Clock Control and Operation Mode (CG-M4G(1)-C) Rev2.0 (Japanese edition)
   Clock Selective Watchdog Timer (SIWDT-A) Rev3.0 (Japanese edition)

3. Function to Use

IP	Channel	Port	Function/Operation mode
Clock Control and Operation Mode	-	-	An external oscillator is used. PLL oscillation
Clock Selective Watchdog Timer	-	-	Watchdog timer is disabled.

4. Target Device

The target devices of this application note are as follows;

TMPM4K4FYAUG	TMPM4K4FWAUG	TMPM4K4FUAUG	TMPM4K4FSAUG
TMPM4K4FYAFG	TMPM4K4FWAFG	TMPM4K4FUAFG	TMPM4K4FSAFG
TMPM4K2FYADUG	TMPM4K2FWADUG	TMPM4K2FUADUG	TMPM4K2FSADUG
TMPM4K1FYAUG	TMPM4K1FWAUG	TMPM4K1FUAUG	TMPM4K1FSAUG
			TMPM4K0FSADUG

* This sample program operates on the evaluation board of TMPM4K4FYAUG.
If other function than the TMPM4K4 one is checked, it is necessary that CMSIS Core related files (the startup file and I/O header file) should be changed properly.
Additionally, the name of microcontroller which is set to the project should be changed.
The BSP related file is dedicated to the evaluation board (TMPM4K4FYAUG). If other function than the TMPM4K4 one is checked, the BSP related file should be changed properly.

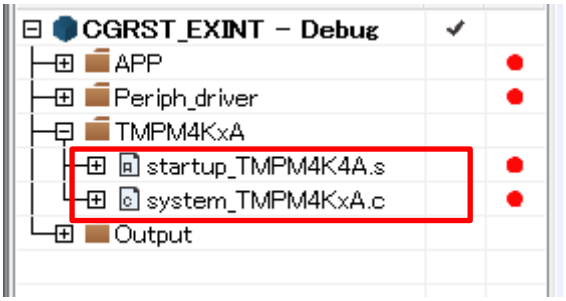
5. Operation Confirmation Condition

Used microcontroller	TMPM4K4FYAUG
Used board	TMPM4K4 evaluation board (Product of ESP-kikaku Co. Ltd.)
Integrated development environment	IAR Embedded Workbench for ARM 8.22.2
Integrated development environment	Arm® Keil® MDK Version 5.24.2.0
Sample program	v1.0.0

6. Outlines of Function

The settings of the watchdog timer and the CG should be done.
After the reset deassertion, the startup process above is executed and the “main” process should be done.
This application note describes the following files;

- startup_TMPM4K4A.s
- system_TMPM4KxA.c



6.1. Watchdog Timer Setting

The setting of the watchdog timer should be done.
The sample program does not use this function (Stop state).
The control register is set to the disable code.

6.2. Clock Generator Setting

The external (f_{EHOSC}) and internal (f_{IHOSC1}) system clocks are set.
In the sample program, the external system clock is set.
In addition, the division ratio of the clock for the output control and the multiplying ratio of the PLL clock are set.

7. Startup and System File

The sample program is prepared for the TMPM4K4 operation.

7.1. Outlines of Operation

The settings are done for the watchdog timer, the system core clock, and the PLL.
After the settings complete, the “main” process in each sample application program is executed.

7.2. Watchdog Timer Setting

In the sample program, the watchdog timer has been set to “disable”.
“SIWD_SETUP” should be changed as follows to enable it.
The setting can be modified by a macro change in “system_TMPM4KxA.c”.
The change of “SIWD_SETUP” (1U) to (0U) makes the watchdog timer enabled.
When the sample program is used with the watchdog timer “enable”, the watchdog timer operates with the initial value.
The initial value is reset after the watchdog timer operation is detected.

7.3. Clock Setting

The external oscillation clock or the internal oscillation clock can be selected.
In the sample program, the external oscillation clock is selected initially.

```
CLOCK_SETUP    (1U)
```

If the (1U) is changed to (0U), the internal oscillation clock is selected.

7.4. PLL Setting

The f_{PLL} clock is generated by the clock multiplying circuit which determines the optimized multiple rate of the frequency of the high-speed oscillator clock fosc (6 MHz to 12 MHz).
The sample program operates with an external 10-MHz clock.

The sample program has been set to using the f_{PLL} = 80 MHz and the 4-division rate.
The input frequencies of 6, 8, 10, and 12 MHz are supported.
f_{PLL} = 80 MHz is generated using the following multiplying values.

External clock frequency * (Multiplying value/Division value) = Operation frequency

6MHz	6.00MHz * (53.3125 / 4) = 79.97MHz
8MHz	8.00MHz * (40.0000 / 4) = 80.00MHz
10MHz	10.00MHz * (32.0000 / 4) = 80.00MHz
12MHz	12.00MHz * (26.6250 / 4) = 79.88MHz

TMPM4K4 has a PLL circuit for the ADC.
The maximum frequency of the clock f_{PLLADC} for the ADC is 120 MHz.
When an external clock frequency is 10 MHz, the following setting sets to f_{PLLADC} = 120 MHz.
The formula is the same as the formula for f_{PLL}.

External clock frequency * (Multiplying value/Division value) = Operation frequency

10 MHz 10.00MHz * (24.0000 / 2) = 120.00MHz

7.5. Change of Clock Frequency

The system clock frequency can be divided by the clock gear in ***[CGSYSCR]***.
#define SYSCR_ Val (0x00000000UL)
The prescaler clock selection and the system clock gear selection can be done by changing the setting value above.

Prescaler clock: fc setting
System clock gear: fc setting

8. Points to Remember on Handling of Sample Programs

When using the sample program with other than “Operation Confirmation Condition” please check the operation sufficiently.

9. Revision History

Revision	Date	Description
1.0	2019-10-16	First release

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