TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHCT9125AFK
TC74VHCT9126AFK

TC74VHCT9125AFK 5-bit Universal Schmitt Buffer with 3-State Outputs
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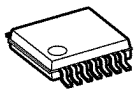


VSSOP14-P-0030-0.50

Weight
VSSOP14-P-0030-0.50 : 0.02 g (typ.)

The TC74VHCT9125A/9126A are an ultra-high-speed 5-bit Schmitt buffer fabricated using silicon-gate CMOS technology.

The TC74VHCT9125A/9126A combines low power consumption of CMOS with Schottky TTL speeds.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Y1 to Y4 outputs can be put in the high-impedance state by placing a logic HIGH on the Enable ($\overline{G}$) input. The CONT input determines the logical inversion of data.A logic LOW on the CONT input configures the TC74VHC9125A/9126A as an inverter; a logic HIGH on the CONT input configures the TC74VHCT9125A/9126A as a buffer.

TC74VHCT9125A Y5 output is an inverting type, and the TC74VHCT9126A Y5 output is a non-inverting type.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHC9125A/9126A are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

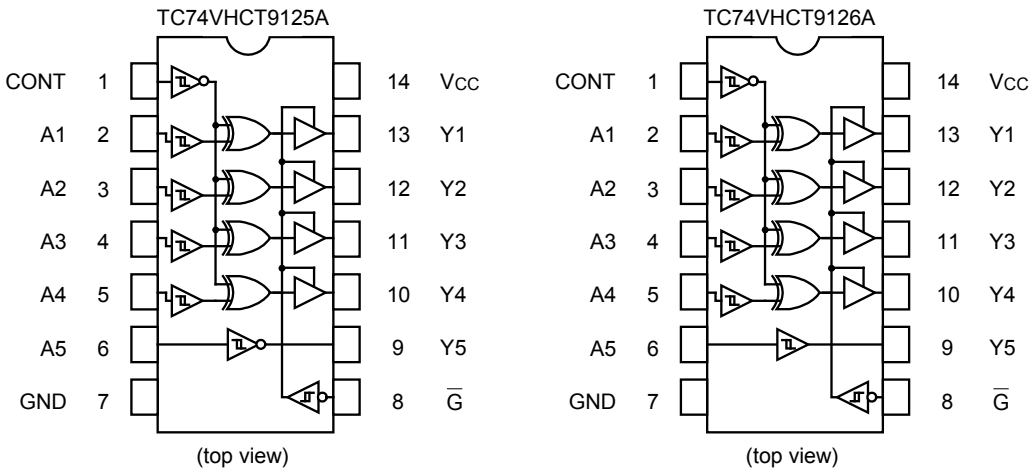
Note: Output in off-state

Features

- High speed: t_{pd} = 6.6 ns (typ.) (V_{CC} = 5 V)
- Low supply current: I_{CC} = 2 μA (max) (Ta = 25°C)
- Compatible with TTL inputs
  V_{IL} = 0.5 V (max)
  V_{IH} = 2.1 V (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Input terminals are at the opposite side of Output terminals

Start of commercial production
2010-07

Pin Assignment



Truth Table

Inputs			Outputs
$\overline{G}$	CONT	A1 to 4	Y1 to 4
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H

Inputs	Outputs	
A5	Y5(9125)	Y5(9126)
L	H	L
H	L	H

X : Don’t care

Z : High impedance

Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating		Unit
Supply voltage range	V_{CC}	−0.5 to 7.0		V
DC input voltage	V_{IN}	−0.5 to 7.0		V
DC output voltage	V_{OUT}	−0.5 to 7.0	(Note 2)	V
		−0.5 to V_{CC} + 0.5	(Note 3)	
Input diode current	I_{IK}	−20		mA
Output diode current	I_{OK}	±20	(Note 4)	mA
DC output current	I_{OUT}	±25		mA
DC V_{CC}/ground current	I_{CC}	±50		mA
Power dissipation	P_D	180		mW
Storage temperature	T_{stg}	−65 to 150		°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note1)

Characteristics	Symbol	Rating		Unit
Supply voltage	V_{CC}	4.5 to 5.5		V
Input voltage	V_{IN}	0 to 5.5		V
Output voltage	V_{OUT}	0 to 5.5	(Note 2)	V
		0 to V_{CC}	(Note 3)	
Operating temperature	T_{opr}	−40 to 85		°C

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: Output in off-state

Note 3: High or low state.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
Positive threshold voltage	V_P	—		4.5	—	—	1.90	—	1.90	V
				5.5	—	—	2.10	—	2.10	
Negative threshold voltage	V_N	—		4.5	0.50	—	—	0.50	—	V
				5.5	0.60	—	—	0.60	—	
Hysteresis voltage	V_H	—		4.5	0.40	—	1.40	0.40	1.40	V
				5.5	0.40	—	1.50	0.40	1.50	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.5	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA
	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output leakage current (Power-OFF)	I_{OPD}	V_{OUT} = 5.5 V		0	—	—	0.5	—	5.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (A1 to 4 - Y1 to 4)	t_{pLH} t_{pHL}	—	5.0 ± 0.5	15	—	6.6	8.5	1.0	10.0	ns
				50	—	8.1	11.5	1.0	13.0	
Propagation delay time (CONT-Y1 to 4)	t_{pLH} t_{pHL}	—	5.0 ± 0.5	15	—	8.0	10.5	1.0	12.0	ns
				50	—	9.9	14.5	1.0	17.0	
Propagation delay time (A5 – Y5)	t_{pLH} t_{pHL}	—	5.0 ± 0.5	15	—	6.0	8.0	1.0	9.5	ns
				50	—	7.9	10.5	1.0	12.0	
3-state output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	5.0 ± 0.5	15	—	6.4	8.5	1.0	10.0	ns
				50	—	8.4	12.5	1.0	14.5	
3-state output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	5.0 ± 0.5	50	—	6.7	11.5	1.0	13.0	ns
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Output capacitance	C_{OUT}	—			—	9	—	—	—	pF
Power dissipation capacitance (Note 2)	C_{PD}	f_{IN} = 1 MHz			—	14	—	—	—	pF

Note 1: Parameter guaranteed by design.

$t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

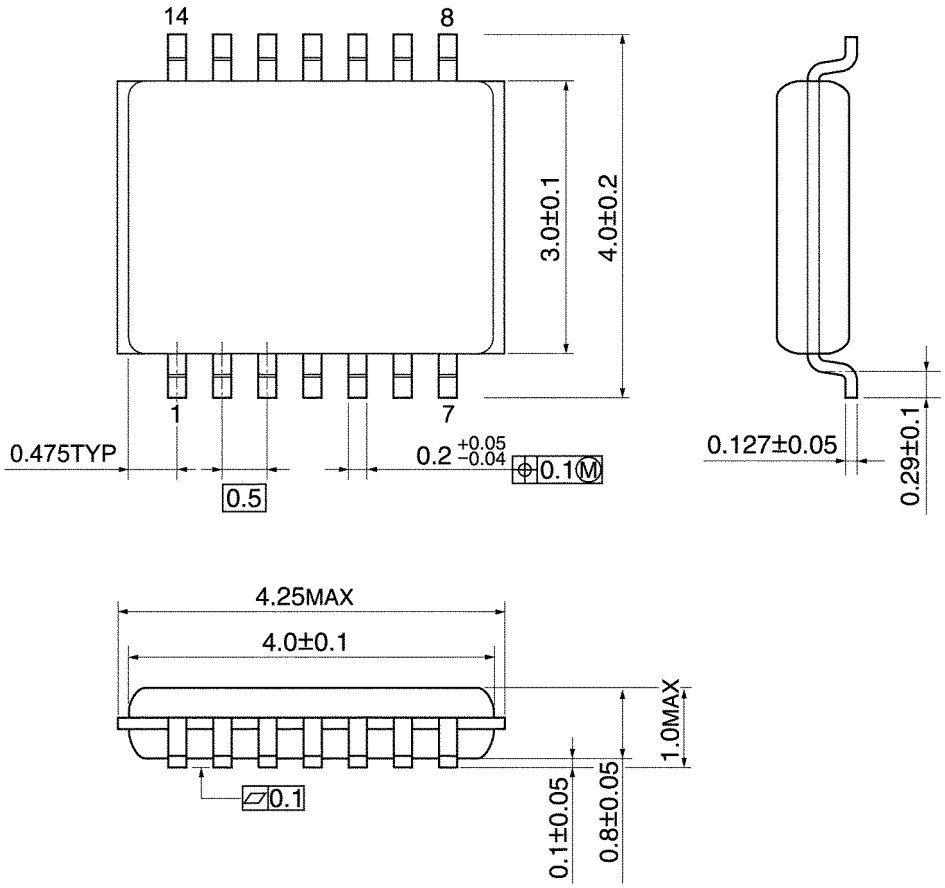
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 5$ (per bit)

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.6	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−0.2	−0.8	V
Minimum high level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	2.1	V
Maximum low level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	0.5	V

Package Dimensions

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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