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Dear Customers,

March, 2019

Reference Manual Correction: Serial Peripheral Interface(TSPI) of TXZ Family

This informs you that we found the following corrections should be made to the reference manual of Serial Peripheral Interface(TSPI) as shown below. If you have any questions or require any further informaiton, please contact your local Toshiba representatives.

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1. Products

M3H Group(1)

TMPM3H0FS	TMPM3H0FM		
TMPM3H1FW	TMPM3H1FU	TMPM3H1FS	TMPM3H1FP
TMPM3H2FW	TMPM3H2FU	TMPM3H2FS	
TMPM3H3FW	TMPM3H3FU	TMPM3H3FS	
TMPM3H4FW	TMPM3H4FU	TMPM3H4FS	
TMPM3H5FW	TMPM3H5FU	TMPM3H5FS	
TMPM3H6FW	TMPM3H6FU	TMPM3H6FS	

M3H Group(2)

TMPM3HLFY	TMPM3HLFZ	TMPM3HLFD
TMPM3HMFY	TMPM3HMFZ	TMPM3HMFD
TMPM3HNFY	TMPM3HNFZ	TMPM3HNFD
TMPM3HPFY	TMPM3HPFZ	TMPM3HPFD
TMPM3HQFY	TMPM3HQFZ	TMPM3HQFD

2. Corresponding Reference Manual

Serial Peripheral Interface (TSPI-B)	Revison 2.0 or earlier

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3. Correction

The reference manual will be corrected as follows, due to the 1st edge sample mode function of slave operation is not supported.

1. Outline

Table 1.1 Functional outline (SPI mode, slave)

Function classification		Function	A Functional Description or the range
SPI mode (Slave)	Transceiver Control	Transfer mode	Single transfer (one burst transfer) Burst transfer (2 to 255 times transfer) Continuously transfer (No limit of transfer times specification)
		Data sampling timing	Data is sampled with 1st edge. **Delete** Data is sampled with 2nd edge.
		CS control	TSPIxCSIN Polarity: Selection of positive logic/ negative logic is possible.
	Ganged Control	Interruption	Transmit interrupt (Transmit completion interrupt, Transmit FIFO interrupt) Receive interrupt (Receive completion interrupt, Receive FIFO interrupt) Error Interrupt (Vertical parity error interrupt, Over run interrupt, Under run interrupt, Trigger error
		Various status detection	TSPI modify status, Transmit shift operation, Transmit completion, Transmit FIFO fill level/ empty detection, Receive operation, Receive completion, Receive FIFO fill level /full detection
		DMA demand	Transmit:Single DMA request, Burst DMA request Receive: Single DMA request, Burst DMA request
	Special Control	Output level of TSPIxTXD during an idle term	High, Low, a last bit data hold, Hi-z
		Output level of TSPIxTXD when underrun error occurred	High, Low
		Software reset	Reset by software.

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3.3.5.3. Continuously transfer

It is the mode which repeats the burst transfer of one frame without specifying the number of transfer frames. In SPI mode, in the case of a master, TSPIxCS0/1/2/3 are certainly deasserted for every one-frame transfer, and TSPIxCS0/1/2/3 are asserted at the time of transfer of the following frame.

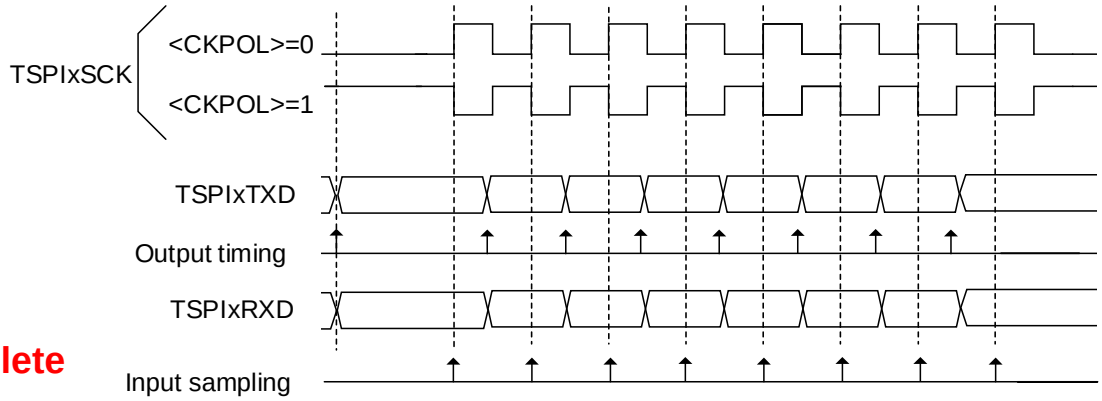
Note1: When in the continuously transfer mode, set to 1st edge sampling of data (*[TSPIxFMTR0]* <CKPHA>=0) and slave mode transmission, a underrun flag is set to "1" (*[TSPIxERR]* <UDRERR>=1) immediately after final data transmission.

Note2: When in the continuously transfer mode, set to 1st edge sampling of data (*[TSPIxFMTR0]* <CKPHA>=0) and slave mode transmission, If reception is continued in the state of FIFO full (*[TSPIxSR]*<RFFLL>=1), an overrun flag will be set to "1" (*[TSPIxERR]*<OVRERR>=1) immediately after final data reception.

Delete

3.3.6. Data sampling timing

[SPI mode(slave) 1st edge data sampling<CKPHA>=0]



Delete

Figure 3.1 Data sampling timing of SPI mode (slave)

4.2.3. *[TSPIxCR2]* (TSPI Control Register 2)

Note1: Each setting is invalid when performing continuous transfer with SPI mode / slave operation / 1st edge data sampling. An undefined value is output.

Delete

Note2: Depending on the product, the set value is fixed. For details, refer to "Product information" of reference manual.

Note3: Set the fill level within available values shown in "Table 3.2 Data format and settable fill level".

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4.2.6. *[TSPIxFMTR0]* (TSPI Format Control Register 0)

Bit	Bit Symbol	After reset	Type	Function
16	CS0POL	0	R/W	Polarity of TSPIxCS0(Master operation) Polarity of TSPIxCSIN(Slave operation) 0: Negative logic 1: Positive logic
15	CKPHA	1	R/W	Polarity of serial clock 0: Data is sampled on the first edge. **(Master operation)** 1: Data is sampled on the second edge. **Add**
14	CKPOL	1	R/W	Polarity of idle period of serial clock (Note2) 0: TSPIxSCK is "Low" level at idle. 1: TSPIxSCK is "High" level at idle.