TOSHIBA

Dear Customers,

March, 2019

Data sheet Correction: External Bus Interface of TX04 Series

This informs you that we found the following corrections should be made to the datasheets as shown below. If you have any questions or require any further informaiton, please contact your local Toshiba representatives.

1. Products

TMPM462F15FG
TMPM462F10FG
TMPM461F15FG
TMPM461F10FG

2. Correction

対象：2018 年 10 月 15 日以前発行のデータシート

Delete description about External Bus Interface Clock Output

Example : TMPM462

[Error1]

4. External bus interface (EBIF)
   - Expandable to 16MB (shared with program and data)
   - Supports separate/multiplex bus : 8-bit/16-bit width
   - Chip select/wait controller: 4 channels
   - External wait function (High active or low active can be selected.)
   - Clock output function (Clock output synchronized with bus cycle) Max. 30MHz

[Correction1]

Deleted.

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[Error2]

1.4.1.1 Peripheral functions

Table 1-1 The number of pins and Pin names

Peripheral function	Pin name	Input or Output	Function
Clock / Mode control	SCOUT	Output	System clock output
External interrupt	INTx	Input	External interrupt input pin x External interrupt input pin x has a noise filter (Filter width 30ns typ.).
	$\overline{NMI}$	Input	Non-maskable interrupt input pin x Non-maskable interrupt input pin x has a noise filter (Filter width 30ns typ.).
µDMA	$\overline{DMAREQx}$	Input	DMA request input pin
External bus interface	An	Output	Address bus output
	Dn	I/O	Data bus input / output
	ADn	I/O	Address and data bus input / output
	$\overline{RD}$	Output	Read strobe output pin
	$\overline{WR}$	Output	Write strobe output pin
	ALE	Output	Address latch enable output pin
	$\overline{BELL}$	Output	Byte enable output pin
	$\overline{BELH}$	Output	Byte enable output pin
	$\overline{CSn}$	Output	Chip select output pin
	WAIT	Input	Wait input pin
	BCLK	Output	Clock output pin
16 bit timer / even counter	TBxIN0	Input	Input capture input pin
	TBxIN1	Input	Input capture input pin

[Correction2]

Deleted.

[Error3]

Pin No.	PORT	Function A	Function B					Port Specification			
			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
PORTK											
163	PK0			UT0TXD	UT0IROUT			PU	Yes	N/A	SMT
166	PK1			UT0RXD	UT0IRIN			PU	Yes	N/A	SMT
167	PK2		$\overline{BELL}$	UT0DCD				PU	Yes	N/A	SMT
168	PK3		$\overline{BELH}$	UT0DSR				PU	Yes	N/A	SMT
169	PK4		$\overline{WR}$	UT0DTR				PU	Yes	N/A	SMT
170	PK5		$\overline{RD}$	UT0RIN				PU	Yes	N/A	SMT
171	PK6		WAIT	$\overline{UT0CTS}$				PU	Yes	N/A	SMT
172	PK7		BCLK	$\overline{UT0RTS}$				PU	Yes	N/A	SMT
173	PK8	INTC $\overline{BOOT}$						PU	Yes	N/A	SMT

[Correction3]

Deleted.

[Error4]

Table 2-3 Pin specifications

Separate bus	Multiplex bus	Port
A0 to A7 (Note1)	-	PA0 to PA7
		PL0 to PL7
A8 to A15	-	PB0 to PB7
A16 to A23 A0 to A7	A16 to A23	PC0 to PC7
D0 to D15	AD0 to AD15	PD0 to PD15
-	ALE	PC8
$\overline{RD}$		$\overline{PK5}$
$\overline{WR}$		PK4
$\overline{BELL}$		PK2
$\overline{BELH}$		PK3
$\overline{CS0}$		PC9
$\overline{CS1}$		PC10
$\overline{CS2}$		PC11
$\overline{CS3}$		PE0
WAIT		PK6
BCLK		PK7

[Correction4]

Deleted.

Except above corrections, please refer to « Correction list » below ;

Correction list

Error	Correction
9. Input / Output port	**9. Input / Output port**
Table 9-10 PORT K Setting List	Table 9-10 PORT K Setting List
PK7: BCLK	Deleted BCLK setting in PK7
10. External Bus Interface (EBIF)	**10. External Bus Interface (EBIF)**
Table 10-1 Features of External bus interface	Table 10-1 Features of External bus interface
Clock output : This function can output clock synchronizing with bus cycles. Control pins : Clock output function: All above pins and BCLK	Deleted Deleted "Clock output function: All above pins and BCLK".
10.3.1 Registers List	10.3.1 Registers List
External Bus Clock Output Control Register EXBCLKCTL 0x0060	Deleted
10.3.5 EXBCLKCTL (External Bus Clock Output Control Register)	Deleted this section.
10.5 Bus Clock	10.5 Bus Clock
External bus operation is synchronous with the bus clock. System clock (fsys) is used as a bus clock when clock output function is not used; when the clock output function is used, output clock (BCLK) is used as a bus clock.	External bus operation is synchronous with the bus clock. System clock (fsys) is used as a bus clock.
10.6 Clock Output Function	Deleted this section.
10.7 External Bus Operations (Separate Bus Mode)	10.7 External Bus Operations (Separate Bus Mode)
when the clock output function is not used; when the clock output function is used, it becomes 1 cycle of BCLK specified with EXBCLKCTL<CLKDIV>.	Deleted
10.8 External Bus Operations (Multiplexed Bus Mode)	10.8 External Bus Operations (Multiplexed Bus Mode)
when the clock output function is not used; when the clock output function is used, it becomes 1 cycle of BCLK defined by EXBCLKCTL<CLKDIV>.	Deleted
10.9.2 Connection Example of External 16-bit SRAM and NOR-Flash (Synchronous multiplex mode)	Deleted this section.
27. Electrical Characteristics	**27. Electrical Characteristics**
27.5.4.3 AC Characteristics(BCLK asynchronous mode Separate Bus Mode)	27.5.4.3 AC Characteristics (asynchronous mode Separate Bus Mode)
27.5.4.4 AC Characteristics (BCLK asynchronous mode multiplex Bus mode)	27.5.4.4 AC Characteristics (asynchronous mode multiplex Bus mode)
27.5.4.5 AC Characteristics (BCLK synchronous mode Separate /multiplex Bus n	Deleted this section.