32-bit RISC Microcontroller

TMPM4K Group(2)

Reference manual

Memory Map
(MMAP-M4K(2))

Revision 1.0

2018-05

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

Related document

Document name
Arm documentation set for the Arm Cortex-M4

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 …
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine Plus
CG	Clock control and Operation Mode
DAC	Digital to Analog Converter
DNF	Digital Noise Filter
FC	Flash control
FLASHIF	Flash interface
I^2C	Inter-Integrated Circuit
IA(INT-I/F)	Interrupt control register A
IB(INT-I/F)	Interrupt control register B
IMN	Interrupt Monitor
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug interface
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
POR	Power On Reset Circuit
RLM	low-speed oscillation / power supply control / reset
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event counter
UART	Universal Asynchronous Receiver Transmitter

1. Memory Map

The memory maps for TMPM4K Group(2) are based on the Arm® Cortex®-M4(with FPU) processor core memory map.

The internal ROM, internal RAM and special function registers (SFR) of TMPM4K Group(2) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4(with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register area is the processor core's internal register region.

For more information on each region, see the "Arm documentation set for the Arm Cortex-M4".

Note that access to regions indicated as "Fault" causes a memory fault if memory faults are enabled, or causes a hard fault if memory faults are disabled. Also, do not access the vendor-specific region.

1.1. TMPM4KxFD

- Code Flash : 512KB
- RAM : 24KB
- Data Flash : 32KB
- Products : TMPM4KLFDUG, TMP4KLFDFG, TMPM4KMFDFG, TMPM4KMFDDFG, TMPM4KNFDFG, TMPM4KNFDDFG, TMPM4KPFDDFG, TMPM4KQFDFG

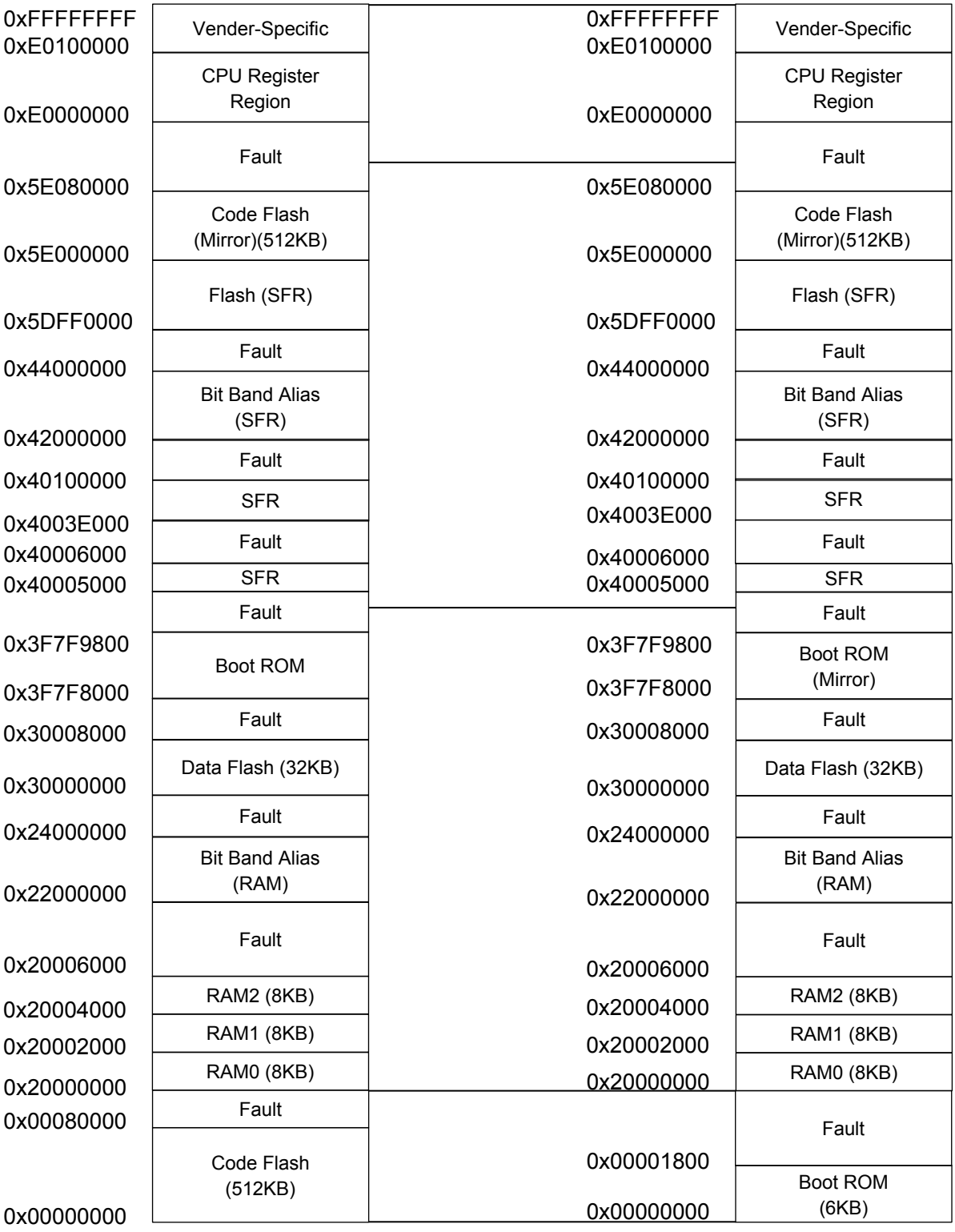

Figure 1.1TMPM4KxFD

1.2. TMPM4KxFY

- Code Flash : 256KB
- RAM : 24KB
- Data Flash : 32KB
- Products : TMPM4KLFYUG, TMP4KLFYFG, TMPM4KMFYFG, TMPM4KMFYDFG, TMPM4KNFYFG, TMPM4KNFYDFG, TMPM4KPFYDFG, TMPM4KQFYFG

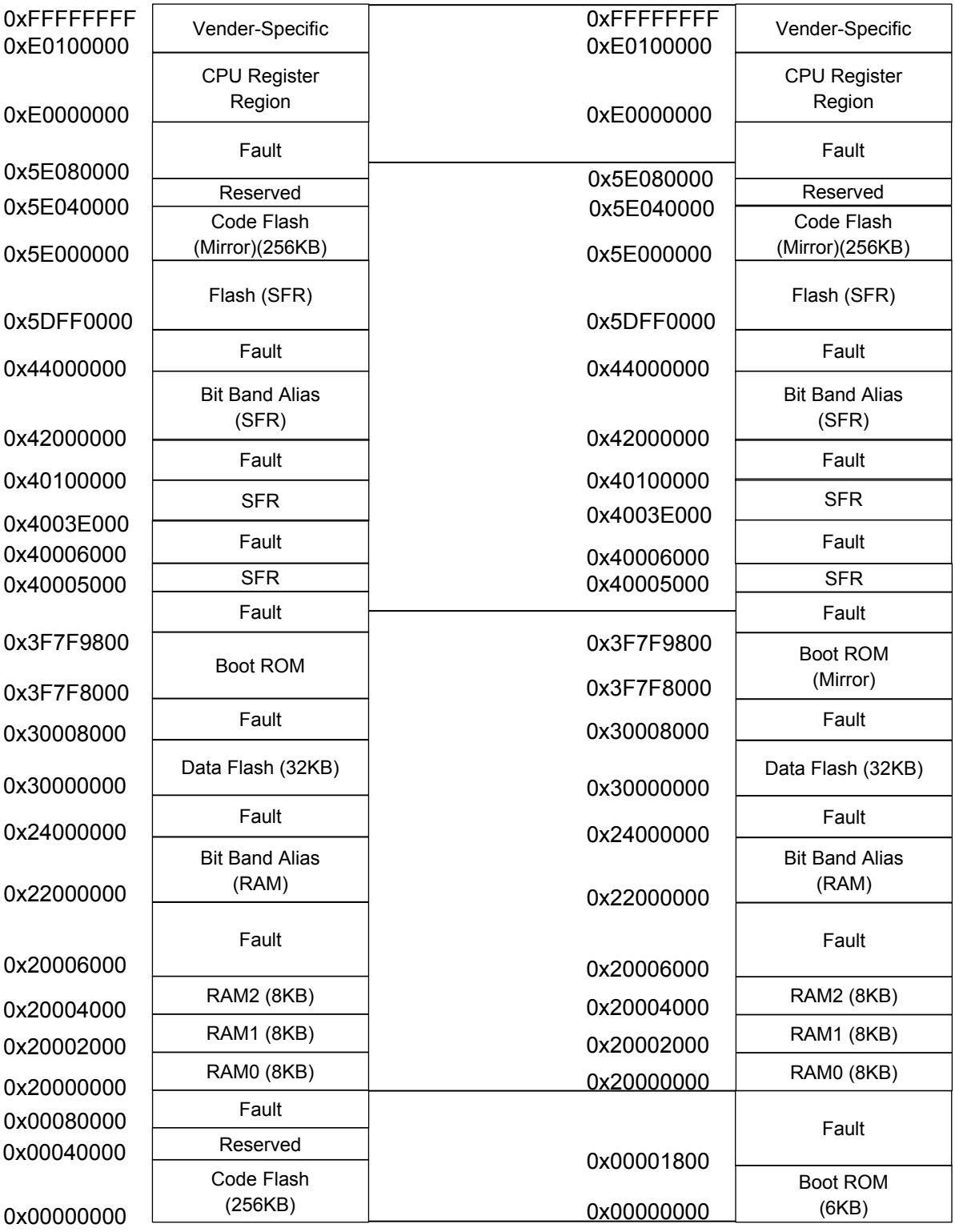

Figure 1.2 TMPM4KxFY

1.3. TMPM4KxFW

- Code Flash : 128KB
- RAM : 24KB
- Data Flash : 32KB
- Products : TMPM4KLFWUG, TMP4KLFWFG, TMPM4KMFWFG, TMPM4KMFWDFG, TMPM4KNFWFG, TMPM4KNFWDFG, TMPM4KPFWDFG, TMPM4KQFWFG

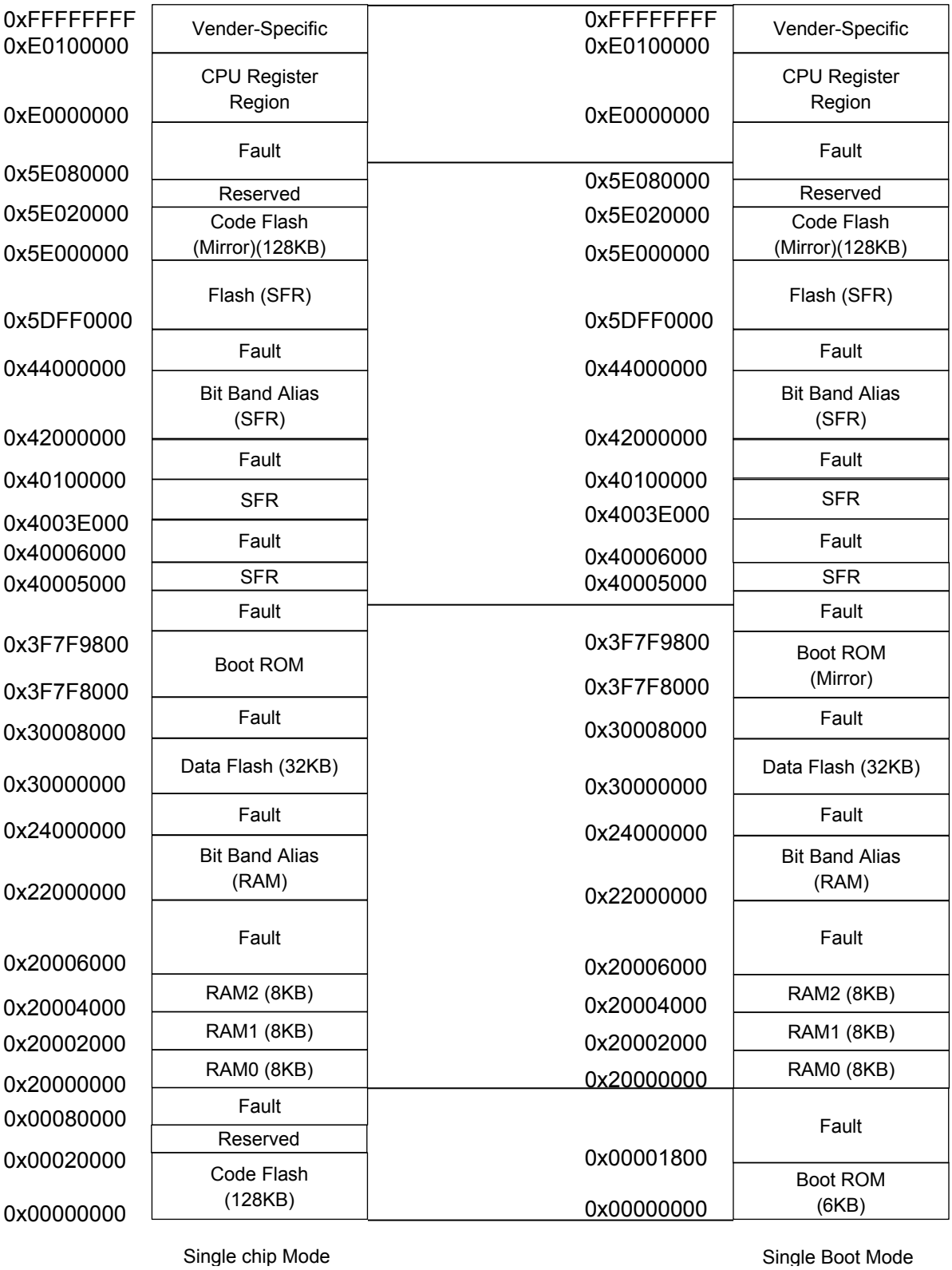

Figure 1.3 TMPM4KxFW

2. Bus Matrix

TMPM4K Group(2) contains the CPU Core of the main master and sub masters. The sub masters include DMAC controller (DMAC) and NBDIF.

Main masters connect to slave ports (S0 to S3) of Bus Matrix. In the bus matrix, master ports (M0 to M9) connect to peripheral functions via connections described as (○) or (●) in the following figure. (●) shows a connection to a mirror area.

Sub-masters connect to slave ports (SS0 to SS2) of Bus Matrix. In the bus matrix, sub ports (SM0 to M8) connect to peripheral functions via connections described as (○) or (●) in the following figure.

While multiple slaves are connected to the same bus master line in the Bus Matrix, if multiple slave accesses are generated at the same time, a priority is given to access from a master with the smallest slave number.

2.1. Structure

2.1.1. Single chip mode

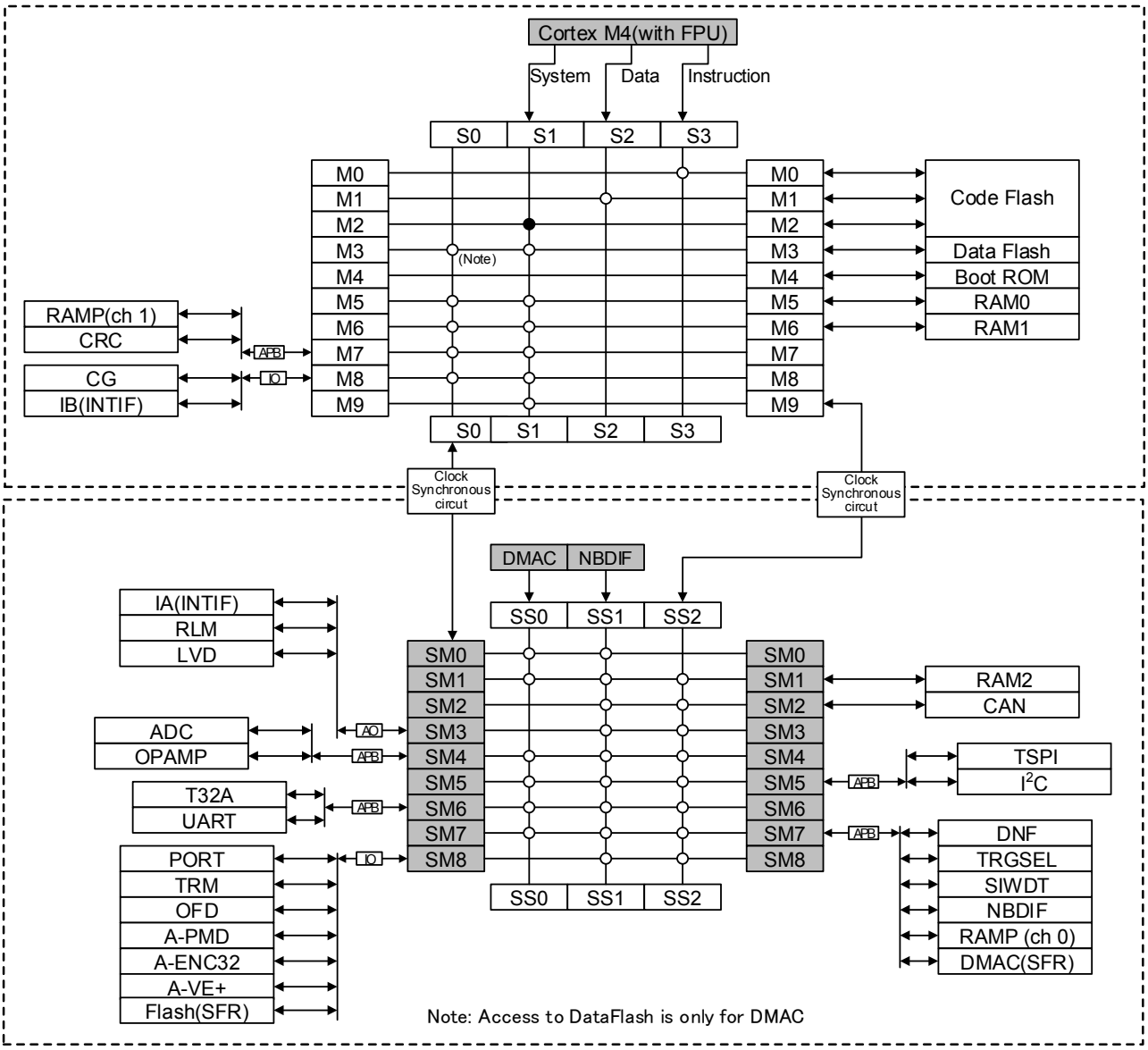

Figure 2.1 Single chip mode

APB: Advanced Peripheral Bus, AO: 8bit-Bus for Backup domain, IO: 32bit-Bus for Main domain

2.1.2. Single boot mode

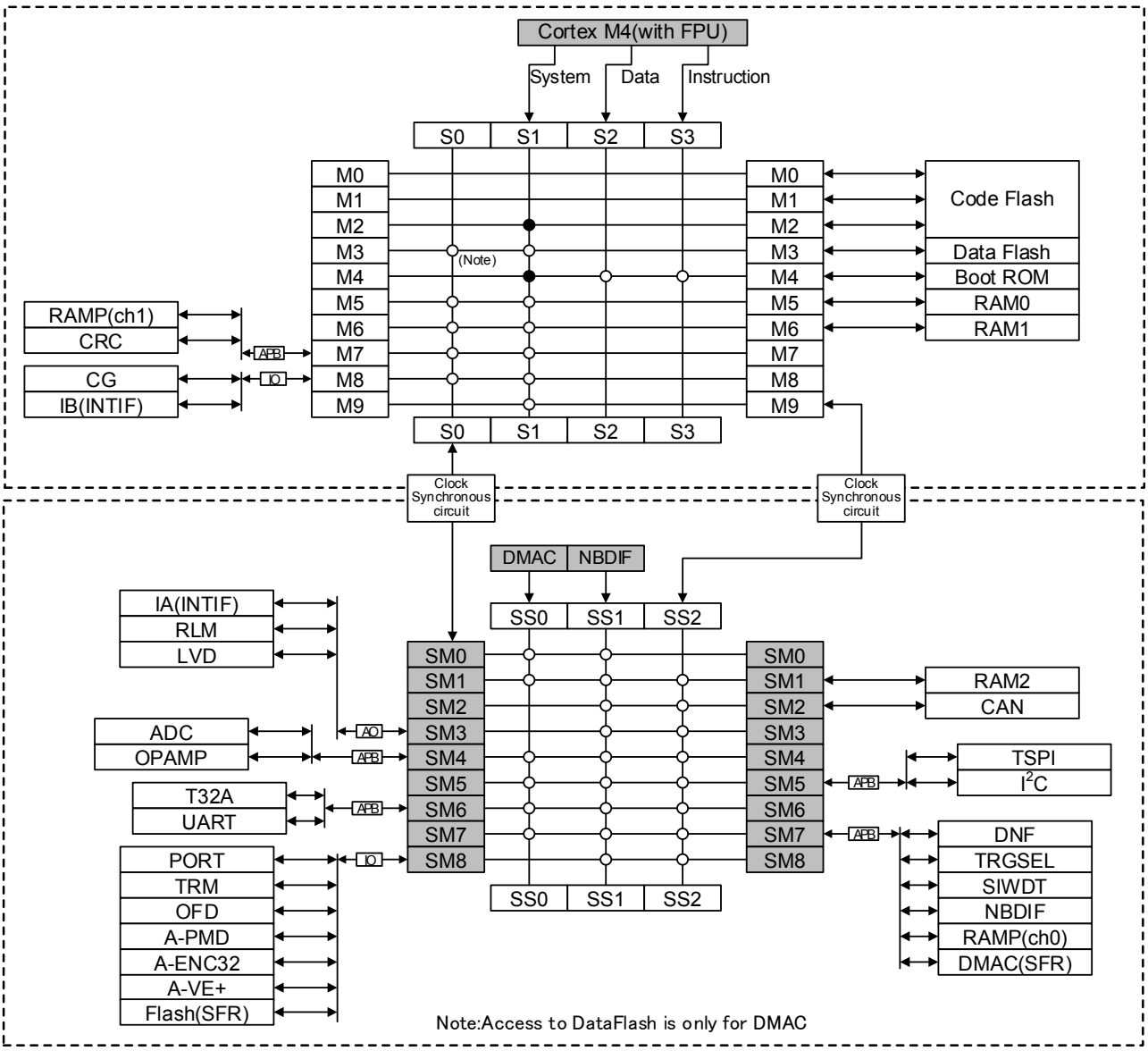

Figure 2.2 Single boot mode

APB: Advanced Peripheral Bus, AO: 8bit-Bus for Backup domain, IO: 32bit-Bus for Main domain

2.2. Connection table

2.2.1. Code area/ SRAM area

(1) Single chip mode

Table 2.1 Single chip mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Code Flash	M0	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	-	✓	Fault
0x00080000	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x20004000	RAM2	SM1	✓	✓	✓	-	-
0x20006000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	-	-
0x24000000	Fault	-	✓	✓	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible, Fault: Bus error

(2) Single boot mode

Table 2.2 Single boot mode

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x00000000	Boot ROM	M4	Fault	Fault	-	✓	✓
0x00001800	Fault	-	Fault	Fault	-	-	-
0x20000000	RAM0	M5	✓	✓	✓	-	-
0x20002000	RAM1	M6	✓	✓	✓	-	-
0x20004000	RAM2	SM1	✓	✓	✓	-	-
0x20006000	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	-	-
0x24000000	Fault	-	✓	✓	Fault	-	-
0x30000000	Data Flash	M3	✓	Fault	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M4	Fault	Fault	✓	-	-
0x5E000000	Code Flash (Mirror)	M2	Fault	Fault	✓	-	-

✓: Accessible, -: not accessible d, Fault: Bus error

2.2.2. Peripheral area/ External bus area

Table 2.3 Peripheral area/ External bus area

Start Address	Slave		Sub master		Main master		
			DMAC	NBDIF	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3
0x40000000	Fault	-	Fault	Fault	Fault	-	-
0x40005000	CAN	SM2	Fault	✓	✓	-	-
0x40006000	Fault	-	Fault	Fault	Fault	-	-
0x4003E000	IA	SM3	Fault	✓	✓	-	-
0x4003E400	RLM		Fault	✓	✓	-	-
0x4003EC00	LVD		Fault	✓	✓	-	-
0x40043000	RAMP(ch 1)	M7	✓	✓	✓	-	-
0x40043100	CRC		✓	✓	✓	-	-
0x40043200	Reserved	-	-	-	-	-	-
0x40083000	CG	M8	✓	✓	✓	-	-
0x40083200	IB		✓	✓	✓	-	-
0x40083400	Reserved	-	-	-	-	-	-
0x400A0200	DNF	SM7	✓	✓	✓	-	-
0x400A0400	TRGSEL		✓	✓	✓	-	-
0x400A0600	SIWDT		✓	✓	✓	-	-
0x400A0800	DNF		✓	✓	✓	-	-
0x400A2000	NBDIF		✓	✓	✓	-	-
0x400A3000	RAMP(ch 0)		✓	✓	✓	-	-
0x400A4000	DMAC(SFR)		✓	✓	✓	-	-
0x400BA000	ADC	SM4	✓	✓	✓	-	-
0x400BD000	AMP		✓	✓	✓	-	-
0x400BD100	Reserved	-	-	-	-	-	-
0x400C1000	T32A	SM6	✓	✓	✓	-	-
0x400CA000	TSPI	SM5	✓	✓	✓	-	-
0x400CE000	UART	SM6	✓	✓	✓	-	-
0x400D1000	I^2C	SM5	✓	✓	✓	-	-
0x400D3000	Reserved	-	-	-	-	-	-
0x400E0000	PORT	SM8	Fault	✓	✓	-	-
0x400E3000	TRM		Fault	✓	✓	-	-
0x400E4000	OFD		Fault	✓	✓	-	-
0x400E9000	A-PMD		Fault	✓	✓	-	-
0x400EA000	A-ENC32		Fault	✓	✓	-	-
0x400EB000	A-VE+		Fault	✓	✓	-	-
0x40100000	Fault	-	Fault	Fault	Fault	-	-
0x42000000	Bit Band Alias	-	Fault	Fault	✓	-	-
0x44000000	Fault	-	Fault	Fault	Fault	-	-
0x5DFF0000	Flash(SFR)	SM8	Fault	✓	✓	-	-

✓: Accessible, -: not accessible, Fault: Bus error

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2018-05-21	New Release

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