CMOS Digital Integrated Circuit Silicon Monolithic

TMPM4L Group(1)

LQFP48 7x7mm 0.5mm pitch
LQFP44 10x10mm 0.8mm pitch

General Description

- Arm® Cortex®-M4 processor with FPU, Operation frequency: 1 to 80 MHz.
  Operation voltage: 2.7 to 5.5 V
- Code flash: 128 KB.
- Package: 44-pin and 48-pin. 2 types of packages are available.
- Hardware IPs such as A-VE, 12-bit ADC, and PMD+ are provided for implementation of vector control

Applications

Motors, major appliances using motors, and industrial equipment.

Features

- Arm Cortex-M4 processor with FPU
  - Operation frequency: 1 to 80 MHz
  - Memory Protection Unit (MPU)
- Operation voltage and Power consumption
  - Operation voltage: 2.7 to 5.5 V
  - Low-power consumption operation: IDLE, STOP1
- Operation temperature: -40 to +105°C
- Internal memory
  - Code flash: 128KB, rewritable up to 10,000 times
  - RAM: 6KB, with parity
- Clock
  - External high speed oscillator: 6 MHz to 12 MHz (Ceramic, Crystal)
  - External high speed clock input: 1 to 10 MHz
  - Internal high speed oscillator (IHOSC1): 10 MHz (±1.3%: -30 to +85°C) User trimming function
  - PLL: 80MHz(System clock)
- Oscillation frequency detector (OFD): Abnormal system clock detection
- Voltage Detection (LVD): 8 level, Generate interrupts and reset outputs
- Interruption
  - External: 7 to 8 factors, with DNF
  - internal: 73 factors
- I/O ports: 33 to 37
  - Open-drain, pull-up/-down
- On-chip debug (JTAG/SW)
- Trigger Selector (TRGSEL)
  - Expand start factor of TSPI/UART/T32A
- CRC Calculation Circuit (CRC): 1 channel
  - CRC32、CRC16
- Asynchronous Serial Interface (UART): 3 channels
  - 5Mbps(Max),FIFO(Send 8-stage, Receive 8-stage)
- Serial Peripheral Interface (TSPI): 3 channels
  - SIO mode,20Mbps(MAX),FIFO(Send 16bitx8,Receive: 16bitx8)
- 12-bit Analog to Digital Converter (ADC): 6 to 7 channel inputs
  - Conversion time: 1.5μs at SCLK=40MHz
  - Self-diagnosis support function
- Programmable motor control circuit plus(PMD+): 1 channels
  - 3-phase complementary PWM output, Synchronized with 12-bit ADC
  - Emergency stop function by external inputs (EMG_N pin, OVV_N pin)
- Advanced vector engine (A-VE): 1 channel
  - Vector control coprocessor cooperates with ADC/PMD+
- Advanced Encoder input circuit(32bit) (A-ENC32): 1 channel
  - Encoder/sensor (3 types)/Timer /Phase counter mode
- 32-bit Timer Event Counter (T32A)
  - 4 channels as 32-bit Timers, 8 channels as 16-bit Timers
  - Interval Timer, Event counter, Input capture, Phase difference input, Pulse output, PPG output, Sync Start, Trigger start
- Watchdog Timer (SIWDT): 1 channel
  - Clock system other than the system clock can be selected
  - Clear window, interrupts and reset output

Start of commercial production
2019-03

Products Lists Categorized by Functions

Table 1.1 Products Lists

Built-in Functions		TMPM4L2FWDUG	TMPM4L1FWUG
Memory	Code Flash (KB)	128	128
	RAM (KB)	6	6
I/O port	PORT (pin)	37	33
External interrupt	INT (pin)	8	7
Timer function	T32A (ch)	4	4
Serial communication function	UART (ch)	3	3
	TSPI(SIO) (ch)	3	3
Analog function	12-bit ADC (AIN ch)	7	6
Motor control peripherals	A-VE (ch)	1	1
	PMD+ (ch)	1	1
	A-ENC32 (ch)	1	1
Other peripherals	CRC (ch)	1	1
	RAMP (ch)	1	1
System function	LVD (ch)	1	1
	WDT (ch)	1	1
	OFD (ch)	1	1
	POR (ch)	1	1
Debug interface	Debug	JTAG/SW	JTAG/SW
Package	Package type	LQFP48 (7 mm × 7 mm, 0.5 mm pitch)	LQFP44 (10 mm × 10 mm, 0.8 mm pitch)
	Package name	LQFP48-P-0707-0.50D	LQFP44-P-1010-0.80B

Note: JTAG can use 4pins (TMS,TCK,TDO,TDI).

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Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder Input Circuit (32-bit)
PMD+	Programmable Motor Control Circuit Plus
A-VE	Advanced Vector Engine
CRC	Cyclic Redundancy Check
DNF	Digital Noise Filter
EHOSC	External High speed Oscillator
IHOSC	Internal High speed Oscillator
INT	Interrupt
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RAMP	RAM parity
SIWDT	Clock Selective Watchdog timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Block Diagram

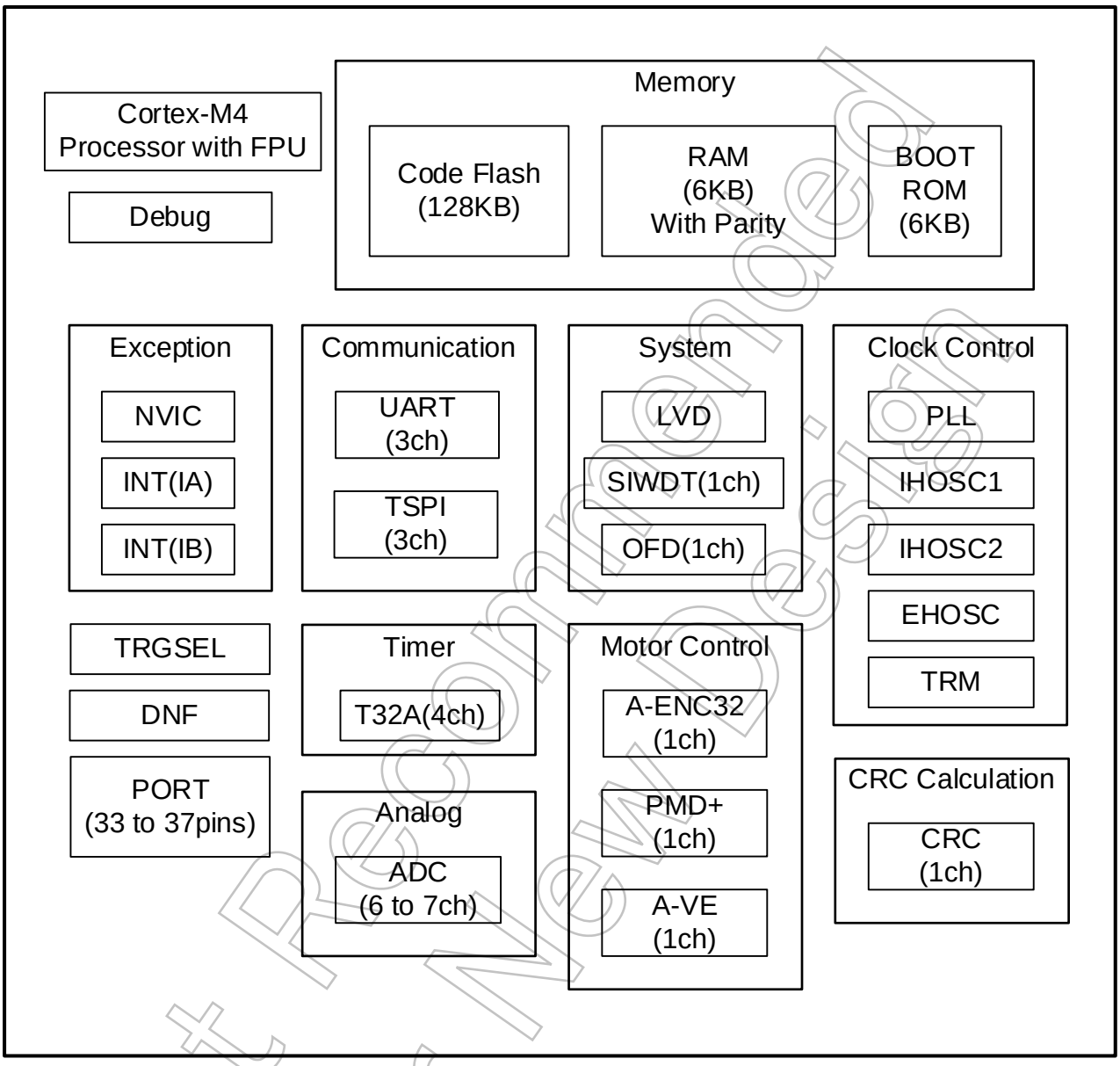
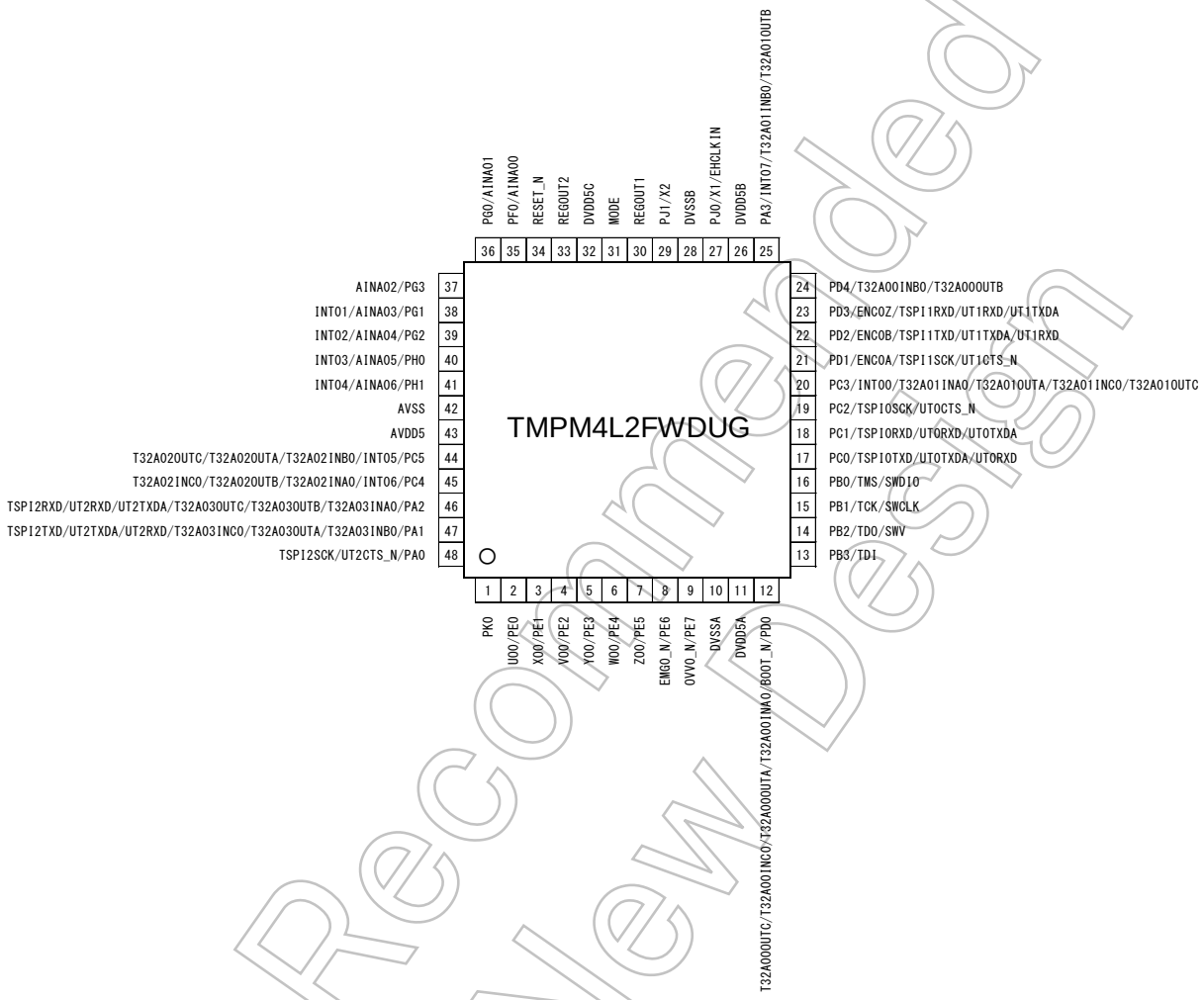


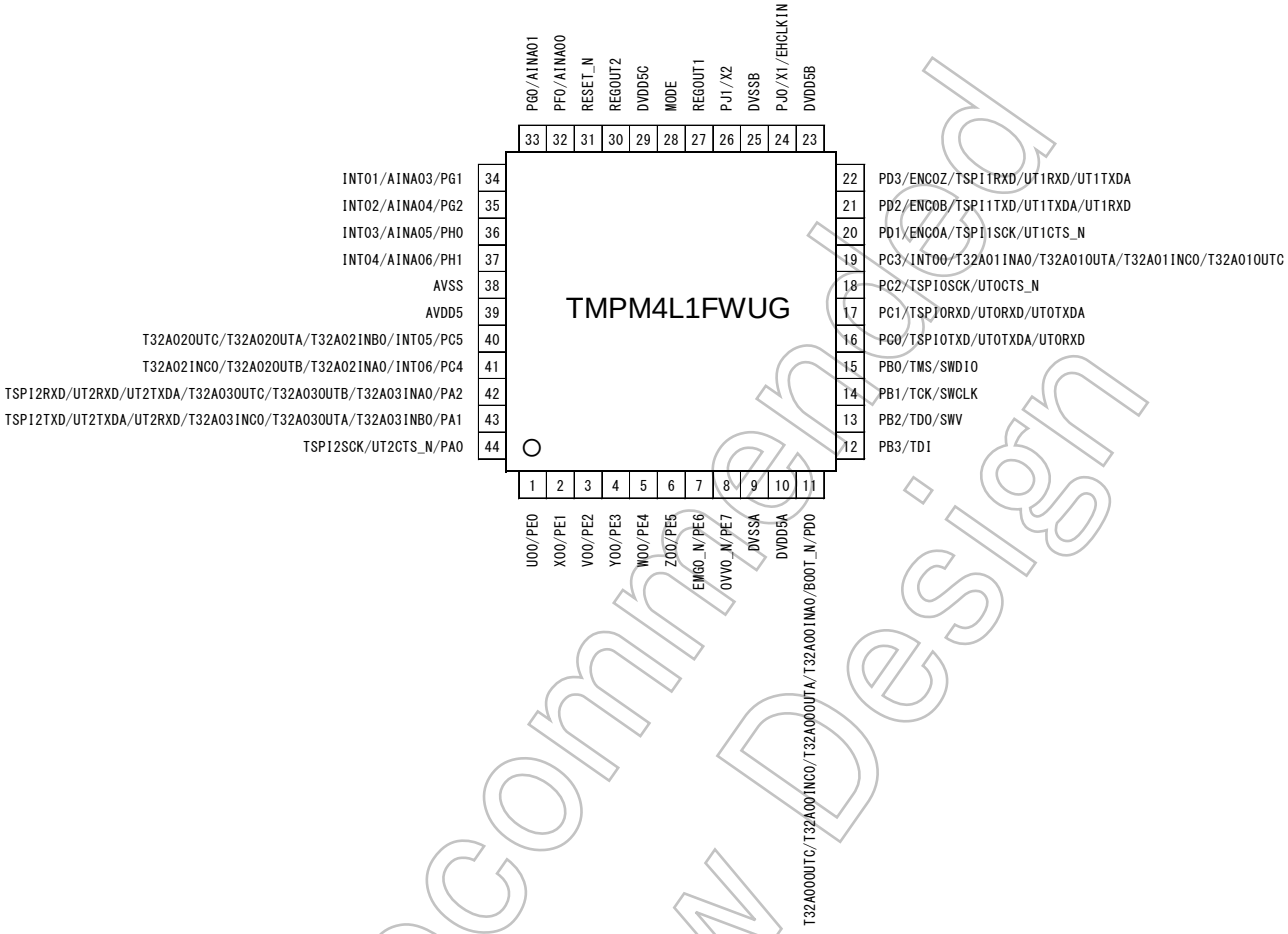
Figure 1.1 Block diagram of the TMPM4L Group(1)

2. Pin Assignment

2.1. LQFP48



2.2. LQFP44



3. Memory Map

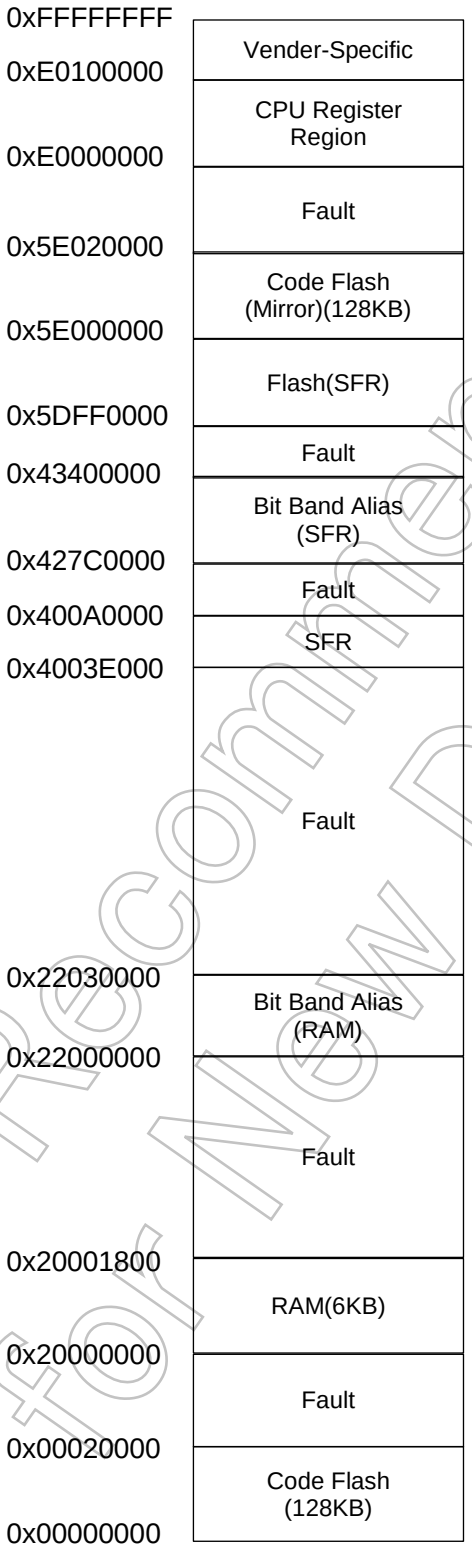


Figure 3.1 Example of the TMPM4LxFW

Note: Fault, Reserved: Please do not access their region.

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM4L2FWDUG TMPM4L1FWUG
Peripheral region	Code Flash (Mirror)	Size	128KB
		START	0x5E000000
		END	0x5E01FFFF
SRAM region	RAM	Size	6KB
		START	0x20000000
		END	0x200017FF
Code region	Code Flash	Size	128KB
		START	0x00000000
		END	0x0001FFFF

4. Pin Description

4.1. Functional Pin Name and Functions

4.1.1. Function Pins of Peripheral

Table 4.1 Pin names and functions of peripheral pins

Peripheral function	Pin name	Input or Output	Function
Interrupt control (IA/IB)	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: typ. 30 ns)
32-bit Timer event counter (T32A)	T32AxINA0	Input	16-bit timer A input capture input pin 0
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer input capture input pin 0
	T32AxOUTC	Output	32-bit timer output pin
Serial peripheral interface (TSPI)	TSPIxRXD	Input	Data input pin
	TSPIxTXD	Output	Data output pin
	TSPIxSCK	I/O	Clock input/output pin
Asynchronous serial communication circuit (UART)	UTxRXD	Input	Data input pin
	UTxTXDA	Output	Data output pin A
	UTxCTS_N	Input	Clear to send signal pin
Programmable Motor control circuit plus (PMD+)	EMGx_N	Input	Emergency state detection input pin
	OVVx_N	Input	Overvoltage detection input pin
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
Advanced Encoder input circuit (32bit) (A-ENC32)	ENCxA	Input	Encoder input pin A
	ENCxB	Input	Encoder input pin B
	ENCxZ	Input	Encoder input pin Z
Analog to Digital Converter (ADC)	AINAx	Input	Analog input pin

Note: "x" means channel number or unit number or interrupt number.

4.1.2. Debug Pins

Table 4.2 Debug pin names and their function

Debug PORT	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin

4.1.3. Control Pins

Table 4.3 Control pin names and their function

	Pin name	Input or Output	Function
Control Pin	X1	Input	High speed oscillator connection pin
	X2	Output	High speed oscillator connection pin
	EHCLKIN	Input	External Clock signal input pin
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled on the rising edge of the RESET_N input. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single boot mode. If it is "High", the MCU enters single chip mode. For details, refer to "Flash Memory" of Reference Manual.
	RESET_N	Input	Reset signal input pin
	MODE	Input	Mode Pin This pin must be fixed to "Low" level.

4.1.4. Power Supply Pins

Table 4.4 Power supply pin names and their function

	Pin name	Function
Power Supply	DVDD5A (Note1) DVDD5B (Note1) DVDD5C (Note1)	Power supply pin for digital DVDD5A/B/C supplies the power to the following pins: PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PJ0,PJ1, PK0, MODE, RESET_N A power supply is supplied to an oscillating circuit from a built-in regulator. X1, X2
	DVSSA (Note2) DVSSB (Note2)	GND pin for digital
	REGOUT1 (Note3)	Capacitor for a regulator connection pin (Note 4)
	REGOUT2 (Note3)	Capacitor for a regulator connection pin (Note 4)
	AVDD5	Power supply pin for analog and reference power pin for analog (VREFH) are combination pins. AVDD5 supplies the power to the following pins: PF0, PG0 to PG3, PH0, PH1
	AVSS	GND pin for analog, reference GND pin for analog (VREFL)

Note1: Apply the voltage to DVDD5A, DVDD5B, and DVDD5C at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA, DVSSB, and AVSS at the same potential except the case that the pins are not provided.

Note3: For REGOUT1 and REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B, or DVDD5C; or DVSSA, DVSSB, or AVSS.

Note4: For the capacitor value, refer to the "Electrical Characteristics"

4.1.5. Capacitors between power supply pins

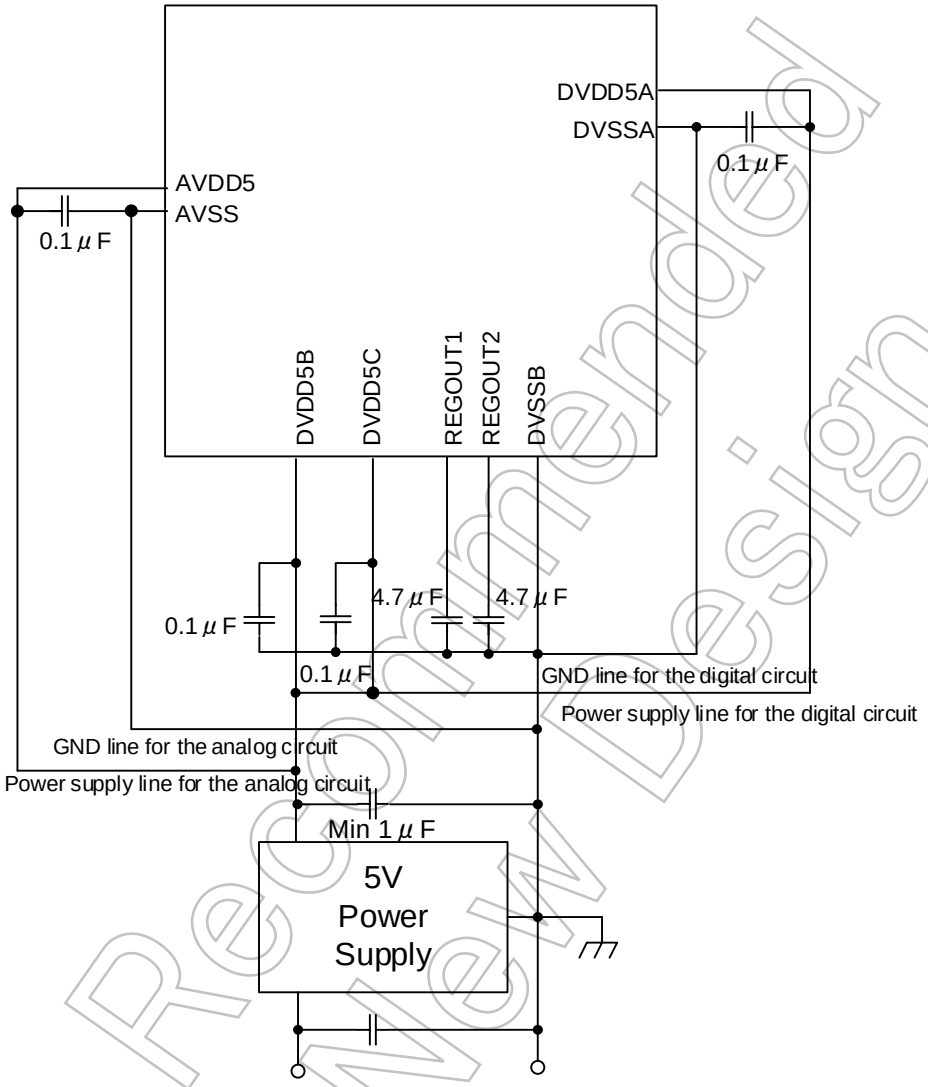


Figure 4.1 Capacitors for power supply pins connection circuit

Note1: 5V power supply output capacitor (min 1 µF) must be placed on the shortest distance from the DVDD5, DVSS.

Note2: 5V power supply and GND lines must be separated for the analog circuit and the digital circuit in near 5V power supply output capacitor (min 1 µF) between this capacitor and DVDD5, DVSS. When the distance to separation becomes long, digital power supply fluctuation is transmitted to the analog power supply due to the common impedance, which becomes noise of the analog circuit.

Note3: Power supply and GND lines must be bring close and be wired. When they are away, a power supply loop makes for power supply and GND lines through the capacitor of a power supply circuit, and they will be the antenna received high frequency noise.

Note4: Capacitors of REGOUT1 and REGOUT2 for regulators must be same capacity, and they must be placed on the shortest distance from DVSS.

Note5: Use multilayer ceramic capacitors for the power supply output capacitor (1 µF or more) and regulator capacitors (4.7 µF).

4.2. Functional Pin and Ports Assignment (Pin Number)

Following table shows a terminal number of the port assignment and each product which were seen from the functional pin.

"-" means that it does not have a pin or there is no assignment of a function.

Table 4.5 Signal connection List (1/4)

Function	Combination functional pin name	Port Name	M4L2 (LQFP48)	M4L1 (LQFP44)
UART ch 0	UT0RXD	PC0	17	16
		PC1	18	17
	UT0TXDA	PC0	17	16
		PC1	18	17
	UT0CTS_N	PC2	19	18
UART ch 1	UT1RXD	PD2	22	21
		PD3	23	22
	UT1TXDA	PD2	22	21
		PD3	23	22
	UT1CTS_N	PD1	21	20
UART ch 2	UT2RXD	PA1	47	43
		PA2	46	42
	UT2TXDA	PA1	47	43
		PA2	46	42
	UT2CTS_N	PA0	48	44
TSPI ch 0	TSPI0RXD	PC1	18	17
	TSPI0TXD	PC0	17	16
	TSPI0SCK	PC2	19	18
TSPI ch 1	TSPI1RXD	PD3	23	22
	TSPI1TXD	PD2	22	21
	TSPI1SCK	PD1	21	20
TSPI ch 2	TSPI2RXD	PA2	46	42
	TSPI2TXD	PA1	47	43
	TSPI2SCK	PA0	48	44

Table 4.6 Signal connection List (2/4)

Function	Combination functional pin name	Port Name	M4L2 (LQFP48)	M4L1 (LQFP44)
T32A ch 0	T32A00INA0	PD0	12	11
	T32A00OUTA	PD0	12	11
	T32A00INB0	PD4	24	-
	T32A00OUTB	PD4	24	-
	T32A00INC0	PD0	12	11
	T32A00OUTC	PD0	12	11
T32A ch 1	T32A01INA0	PC3	20	19
	T32A01OUTA	PC3	20	19
	T32A01INB0	PA3	25	-
	T32A01OUTB	PA3	25	-
	T32A01INC0	PC3	20	19
	T32A01OUTC	PC3	20	19
T32A ch 2	T32A02INA0	PC4	45	41
	T32A02OUTA	PC5	44	40
	T32A02INB0	PC5	44	40
	T32A02OUTB	PC4	45	41
	T32A02INC0	PC4	45	41
	T32A02OUTC	PC5	44	40
T32A ch 3	T32A03INA0	PA2	46	42
	T32A03OUTA	PA1	47	43
	T32A03INB0	PA1	47	43
	T32A03OUTB	PA2	46	42
	T32A03INC0	PA1	47	43
	T32A03OUTC	PA2	46	42

Table 4.7 Signal connection List (3/4)

Function	Combination functional pin name	Port Name	M4L2 (LQFP48)	M4L1 (LQFP44)
12-bit ADC unit A	AINA00	PF0	35	32
	AINA01	PG0	36	33
	AINA02	PG3	37	-
	AINA03	PG1	38	34
	AINA04	PG2	39	35
	AINA05	PH0	40	36
	AINA06	PH1	41	37
INT	INT00	PC3	20	19
	INT01	PG1	38	34
	INT02	PG2	39	35
	INT03	PH0	40	36
	INT04	PH1	41	37
	INT05	PC5	44	40
	INT06	PC4	45	41
	INT07	PA3	25	-
PMD+ ch 0	EMG0_N	PE6	8	7
	OVV0_N	PE7	9	8
	UO0	PE0	2	1
	VO0	PE2	4	3
	WO0	PE4	6	5
	XO0	PE1	3	2
	YO0	PE3	5	4
	ZO0	PE5	7	6
A-ENC32 ch 0	ENC0A	PD1	21	20
	ENC0B	PD2	22	21
	ENC0Z	PD3	23	22

Table 4.8 Signal connection List (4/4)

Function	Combination functional pin name	Port Name	M4L2 (LQFP48)	M4L1 (LQFP44)
JTAG/SW	TMS	PB0	16	15
	TCK	PB1	15	14
	TDO	PB2	14	13
	TDI	PB3	13	12
	SWDIO	PB0	16	15
	SWCLK	PB1	15	14
	SWV	PB2	14	13
Control pin	X1	PJ0	27	24
	X2	PJ1	29	26
	EHCLKIN	PJ0	27	24
	BOOT_N	PD0	12	11
	RESET_N		34	31
	MODE		31	28
Power supply pin	AVDD5		43	39
	AVSS		42	38
	DVDD5A		11	10
	DVDD5B		26	23
	DVDD5C		32	29
	DVSSA		10	9
	DVSSB		28	25
	REGOUT1		30	27
	REGOUT2		33	30

4.3. Ports

The symbols of each table of the port have the following meanings.

- Input/Output: Input or/and Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/Output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  YES: Support
  NO: Not available

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- Under Reset: Port state under Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

- After Reset: Port state after Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

4.3.1. Port Specification Table

Table 4.9 Pin numbers, and specifications of Port A,B,C,D,E,F,G

Port Name	Input/Output	PU/PD	OD	SMT/ CMOS	Under Reset	After Reset
PA0	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PA1	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PA2	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PA3	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PB0	Input/Output	PU/PD	YES	SMT	PU(Note2)	PU(Note2)
PB1	Input/Output	PU/PD	YES	SMT	PD(Note2)	PD(Note2)
PB2	Input/Output	PU/PD	YES	SMT	Hi-z(Note2)	Hi-z(Note2)
PB3	Input/Output	PU/PD	YES	SMT	PU(Note2)	PU(Note2)
PC0	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PC1	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PC2	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PC3	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PC4	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PC5	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PD0	Input/Output	PU/PD (Note1)	YES	SMT	Hi-z (Note1)	Hi-z
PD1	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PD2	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PD3	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PD4	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE0	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE1	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE2	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE3	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE4	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE5	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE6	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PE7	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PF0	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PG0	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PG1	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PG2	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PG3	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z

Note 1: Combination with BOOT_N. When RESET_N=0, Pull-up resistor is enabled. When RESET_N=1, the pin state is Hi-z with internal reset.

Note 2: It is assigned to a debugging pin in the state of the initial stage. (PB3: TDI, PB2: TDO/SWV, PB0: TMS/SWDIO, PB1: TCK/SWCLK) When receiving the command from TOOL, PB2: TDO/SWV becomes output.

Table 4.10 Pin numbers, and specifications of Port H,J,K

Port Name	Input/Output	PU/PD	OD	SMT/ CMOS	Under Reset	After Reset
PH0	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PH1	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z
PJ0	Input	PD	N/A	SMT	Hi-z	Hi-z
PJ1	Input	PD	N/A	SMT	Hi-z	Hi-z
PK0	Input/Output	PU/PD	YES	SMT	Hi-z	Hi-z

5. Functional Description and Operation Description

5.1. Reference Manuals

For more information on product of TMPM4L Group(1), please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM4L Group(1)

Reference Manual	IP Symbol	Category
Input/Output Ports (TMPM4L Group(1))	PORT-M4L(1)	System
Memory Map (TMPM4L Group (1))	MMAP-M4L(1)	System
Exception (TMPM4L Group (1))	EXCEPT-M4L(1)	System
Clock Control and Operation Mode (TMPM4L Group (1))	CG-M4L(1)-A	System
Product Information (TMPM4L Group (1))	PINFO-M4L(1)	System
Power supply and Reset operation (TMPM4L Group (1))	RESET-M4L(1)	System
Flash Memory	FLASH256-B	Peripheral
Trimming Circuit	TRM-A	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-B	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
Asynchronous Serial Communication Circuit	UART-D	Peripheral
Serial Peripheral Interface	TSPI-C	Peripheral
12-bit Analog to Digital Converter	ADC-D	Peripheral
Programmable Motor Control Circuit Plus	PMD+-B	Peripheral
Advanced Encoder Input Circuit (32-bit)	A-ENC32-A	Peripheral
Advanced Vector Engine	A-VE-A	Peripheral
32-bit Timer Event Counter	T32A-B	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
CRC Calculation Circuit	CRC-A	Peripheral
RAM Parity	RAMP-B	Peripheral

5.2. Processor Core

The TMPM4L Group(1) incorporates a high-performance 32-bit processor core (Arm Cortex-M4 processor with FPU).

For the operation of the processor core, refer to the Arm documentation set for "Cortex-M series processors". This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M4 processor with FPU revision used in the TMPM4L Group(1) is shown as below:

For details of the CPU core and the architecture, refer to the documentation of the Arm in the following URL:

http://infocenter.arm.com/help/index.jsp

Table 5.2 Core revision

Group name	Core revision
TMPM4L Group(1)	r0p1

5.2.2. Configurable Options

In the Cortex-M4 processor with FPU, some blocks can be selected to implement. The following table shows the configurations of the TMPM4L Group(1).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Not available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/Serial wire
Bit band	Available
Sequential control of AHB	Not available

5.3. Clock Control and Operation Mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The outline of the clock/mode control circuit is as follows:

- Internal high speed oscillator: 10MHz
- Selectable from the external high speed oscillator or internal high speed oscillator.
- PLL(Clock Multiplication Circuit):
  For System clock, Capable of 80 MHz output by changing the multiplication ratio according to the frequency of the high speed oscillation circuit.
- Clock gear:
  The high speed clock can be divided by 1/1, 1/2, 1/4, 1/8, or 1/16 and the clock is used as the system clock (fsys).
- Low-power consumption mode:
  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enable or disable operation in the IDLE mode.
  STOP1: The system clock is stopped in this mode.

5.4. Flash Memory (128KB Code FLASH)

The cord flash stores instruction code, and CPU reads instruction code and executes.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

5.5. Oscillator

External High Speed Oscillator (EHOSC):

Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.

Internal High Speed Oscillator 1 (IHOSC1):

The oscillation frequency is 10MHz. Use clock source for System clock.

Internal High Speed Oscillator 2 (IHOSC2):

The oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

	M4L2	M4L1
EHOSC	✓	✓
IHOSC1	✓	✓
IHOSC2	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust oscillation frequency of the internal high speed oscillator 1 (IHOSC1).

Table 5.5 Built-in TRM

	M4L2	M4L1
TRM	✓	✓

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detector (OFD) is a function that detects an abnormal state of the clock. It measures the external high speed oscillation (f_{EHOSC}) or high speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.

The upper limit and the lower limit of detection frequency ranges can be specified respectively.

Table 5.6 Built-in OFD

	M4L2	M4L1
OFD	✓	✓

Note: ✓: Available, -: N/A

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from eight kinds. LVD is set to enable from the Reset state at the Power on.

Table 5.7 Built-in LVD

	M4L2	M4L1
LVD	✓	✓

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter circuit (DNF)

The DNF can eliminate the noise of input signals from external interrupt pins at the certain range. The noise of the High level / Low level input of the external interrupt signal INTx is removed.

Table 5.8 Number of External Interrupt (Built-in DNF)

NFD	M4L2	M4L1
Number of External Interrupt	8	7

5.10. Debug Interface (DEBUG)

TMPM4L Group(1) contain Interface for connecting debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK). These are connected with the Debug tool and used for program development.

TMPM4L Group(1) products support serial wire debug ports, JTAG debug ports.

Table 5.9 Built-in Debug Interface

Debug Pin (Signal Name)	PORT	M4L2	M4L1
TMS/SWDIO	PB0	✓	✓
TCK/SWCLK	PB1	✓	✓
TDO/SWV	PB2	✓	✓
TDI	PB3	✓	✓

Note: ✓: Available, -: N/A

5.11. Asynchronous Serial Communication Circuit (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first / LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8-stage at transmission; and on 8-stage at reception.

Table 5.10 Built-in UART

UART	M4L2	M4L1
Channel 0	✓	✓
Channel 1	✓	✓
Channel 2	✓	✓

Note : ✓: Available, -: N/A

5.12. Serial Peripheral Interface (TSPI)

The TSPI supports SIO bus type, which does not use a CS signal at communications.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There is an 8-stage 16-bit FIFO for reception and transmission, each. The TSPI supports the master and slave communications.

Table 5.11 Built-in TSPI

TSPI(SIO)	M4L2	M4L1
Channel 0	✓	✓
Channel 1	✓	✓
Channel 2	✓	✓

Note : ✓: Available, -: N/A

5.13. 12-bit Analog to Digital Converter (ADC)

The ADC is a successive-approximation analog to digital converter. The combination of a conversion result register and analog input can be programmed in each startup trigger of AD conversion. A startup trigger for analog to digital conversion can be selected from software or peripheral functions (PMD trigger outputs, timer event counter outputs).

The monitor function of conversion result is also available and it can generate an interrupt request when the compare conditions are matched.

This ADC incorporates a selector to connect VREFH/VREFL with reference power supply. Controlling by software can support self-diagnosis function.

Table 5.12 Built-in ADC

ADC	M4L2	M4L1
Unit A	✓	✓
Analog Inputs Pin count	7	6

Note 1: ✓: Available, -: N/A

Note 2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

5.14. Programmable Motor Control Circuit Plus (PMD+)

The programmable motor control circuit plus (PMD+) enables users to control brushless DC motors easily. It incorporates the three-phase pulse modulation circuit and dead-time circuit, and easily generates waveforms for motor control by operating with the ADC in a coordinated fashion.

It also provides the over-voltage detection input and abnormal detection input to support safety measures.

Table 5.13 Built-in PMD+

A-PMD	M4L2	M4L1
Channel 0	✓	✓

Note : ✓: Available, -: N/A

5.15. Advanced Encoder Input Circuit (32-bit) (A-ENC32)

The advanced encoder input circuit (32-bit)(A-ENC32) supports an incremental encoder to acquire the motor position easily. The noise canceller is installed in the input pins, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC32 provides six operation modes: encoder mode, sensor modes (3 kinds), timer mode, and phase counter mode.

Table 5.14 Built-in A-ENC32

A-ENC	M4L2	M4L1
Channel 0	✓	✓

Note : ✓: Available, -: N/A

5.16. Advanced Vector Engine (A-VE)

The advanced vector engine executes vector control by hardware. In this vector operation, the ADC and PMD+ operate in a coordinated fashion without software involvement.

Table 5.15 Built-in A-VE

A-VE	M4L2	M4L1
Channel 0	✓	✓

Note : ✓: Available, -: N/A

5.17. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter respectively. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A have an interval timer, event counter, input capture, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.16 Built-in T32A

T32A	M4L2	M4L1
Channel 0	✓	✓
Channel 1	✓	✓
Channel 2	✓	✓
Channel 3	✓	✓

Note 1: ✓: Available, -: N/A

Note 2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

5.18. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys/4), internal oscillator 1 (f_{IHOSC1}), or internal oscillator 2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, change of a register can be forbidden until reset starts by setting to protected mode.(the count-clear function is possible)

Table 5.17 Built-in SIWDT

	M4L2	M4L1
SIWDT	✓	✓

Note : ✓: Available, -: N/A

5.19. CRC Calculation Circuit (CRC)

This product has the Hardware calculation circuit for CRC32 and CRC16.
It can be used for detecting a memory and communication data error.

Table 5.18 Built-in CRC

	M4L2	M4L1
CRC	✓	✓

Note : ✓: Available, -: N/A

5.20. RAM Parity (RAMP)

A RAM parity function generates and (8-bit unit) stores even parity data at the time of the writing to RAM, and performs a parity judging at the time of reading from RAM.
An interrupt is generated when it becomes an error by judgment. The Status and Address which the error generated are known.
A parity error is detectable in real time, since parity generating/ judgment is hardware.

Table 5.19 Built-in RAMP

	M4L2	M4L1
RAMP	✓	✓

Note : ✓: Available, -: N/A

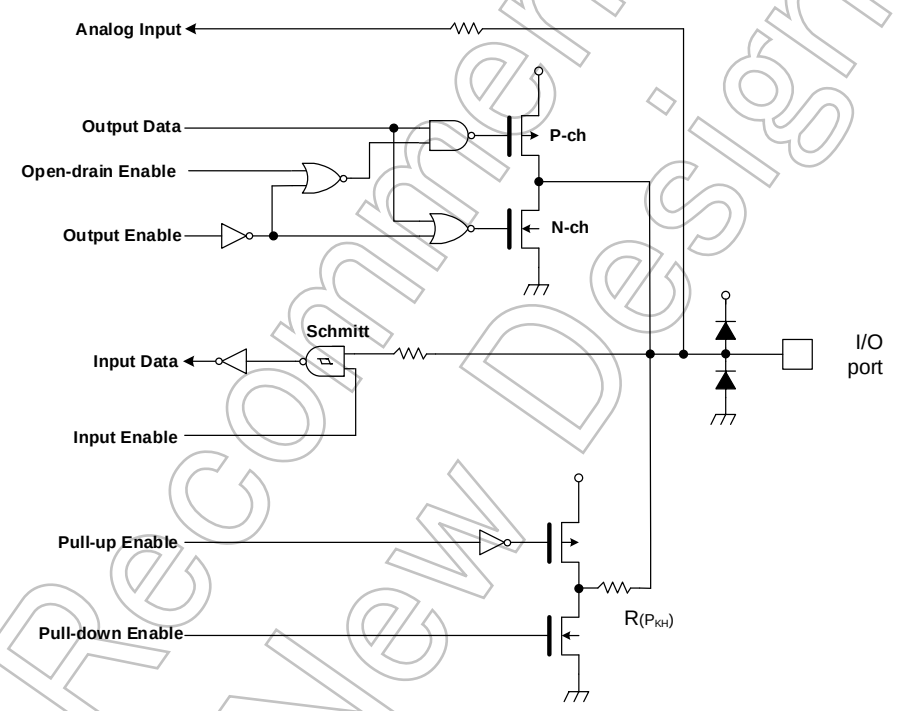
6. Equivalent Circuit

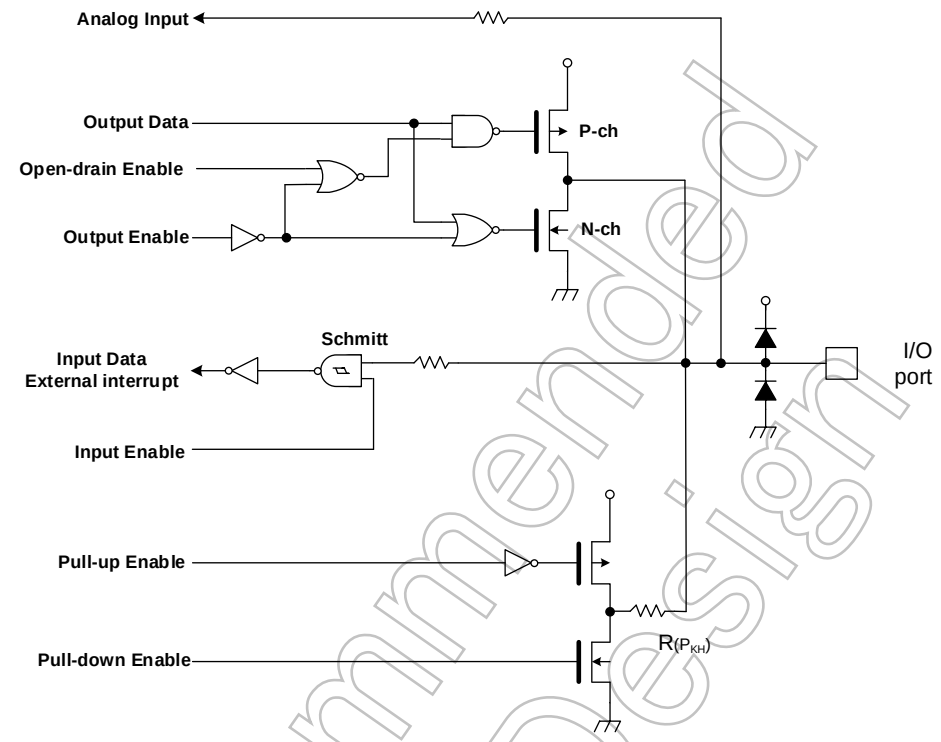
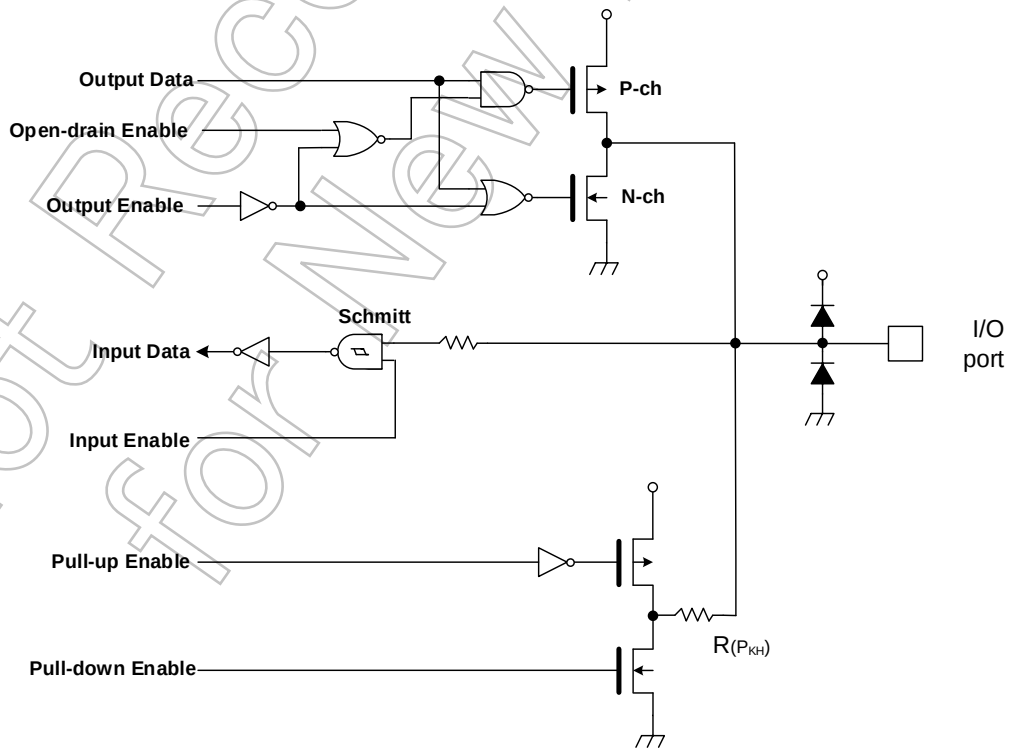
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCXX] series.

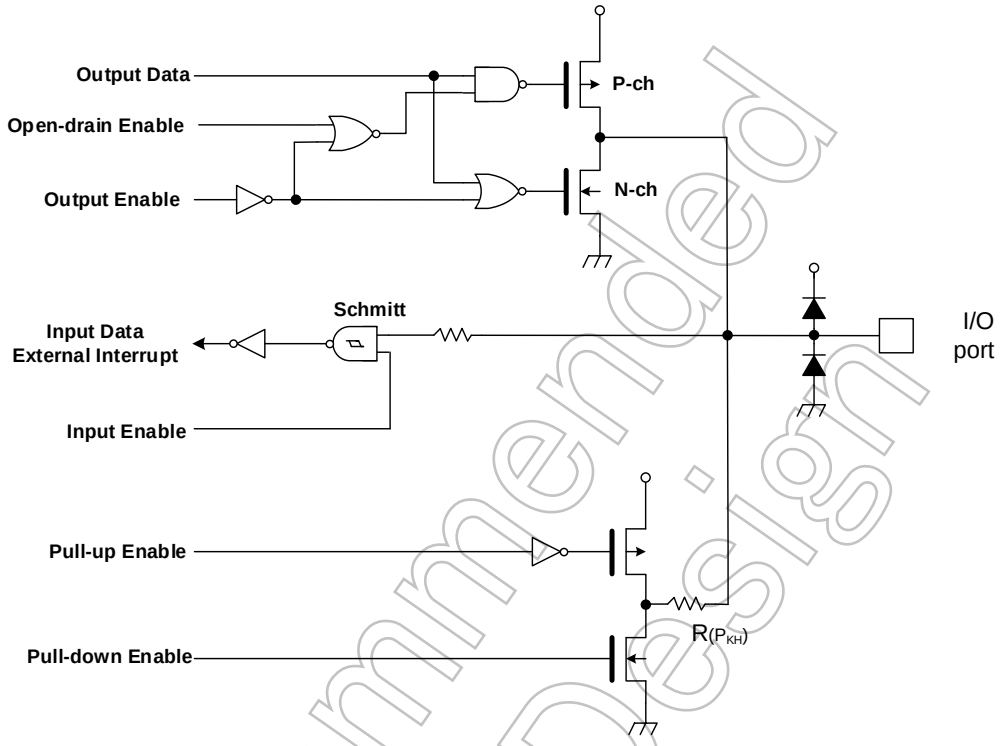
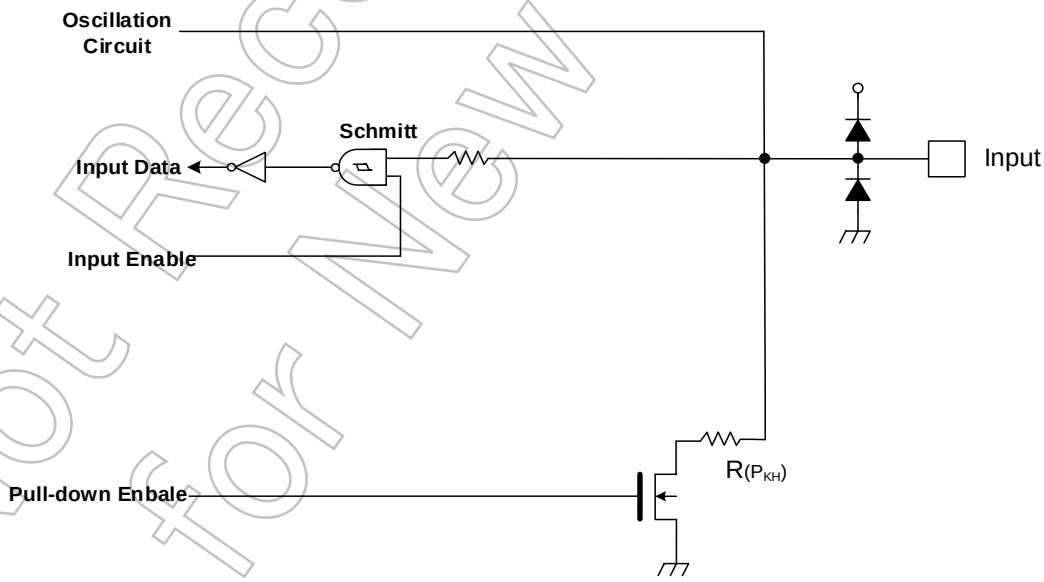
The input protection resistance ranges from several tens of Ω to several hundred Ω. Feedback resistor and Damping resistor are shown with a typical value.

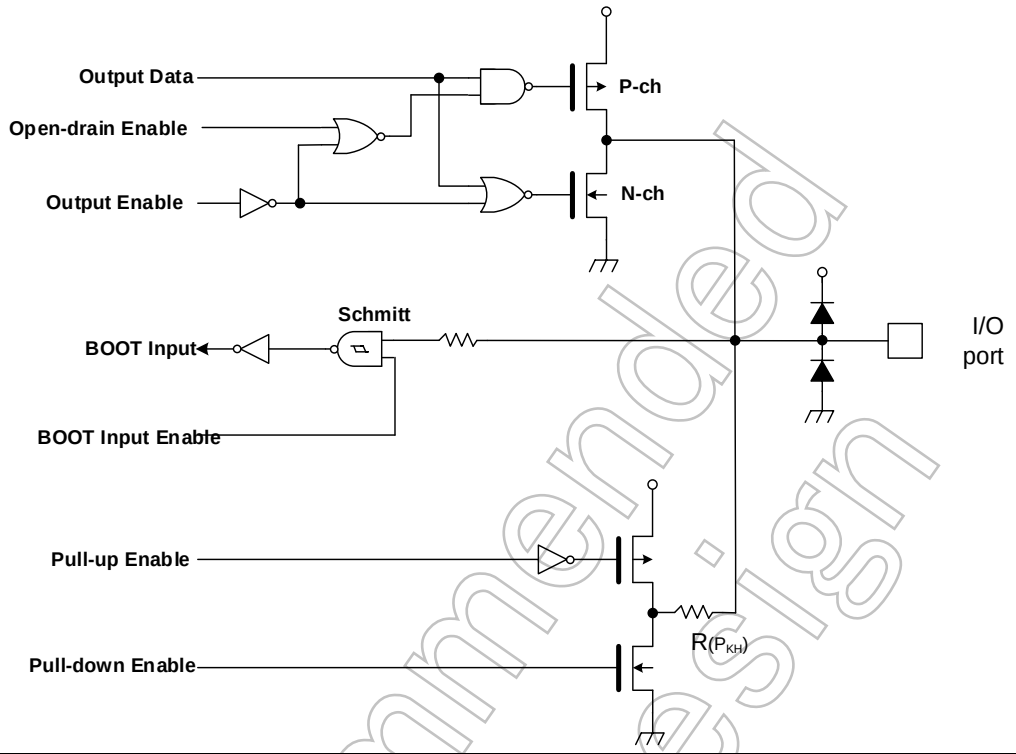
Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

6.1. Port

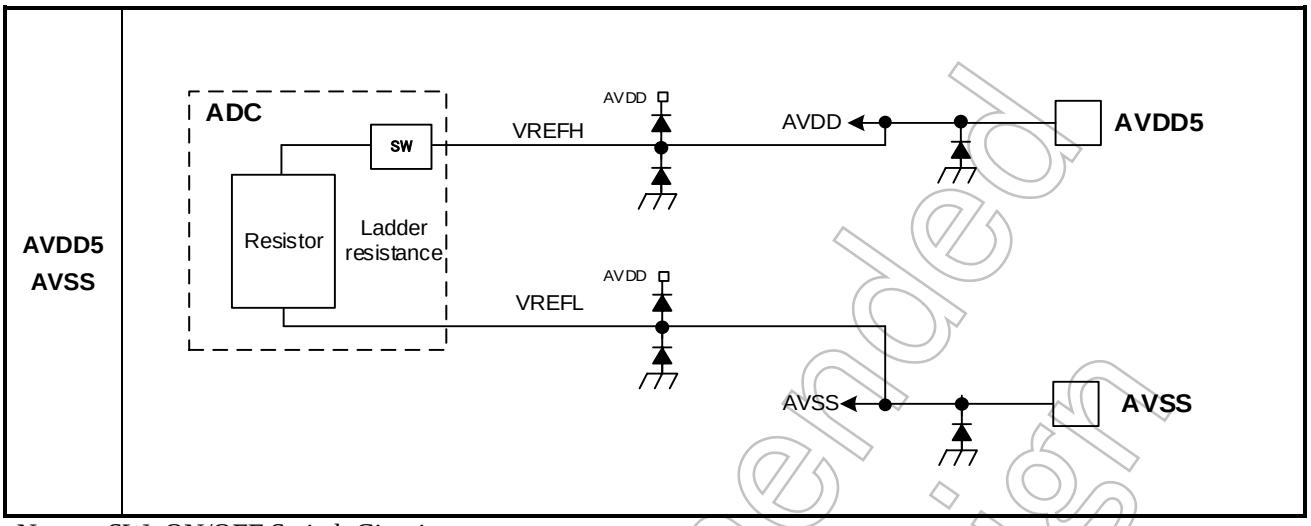
PF0, PG0,PG3,	**(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt input, Analog input)** 

PG1,PG2, PH0,PH1	(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt input, Analog input, External Interrupt Input) 
PA0 to PA2, PB0 to PB3, PC0 to PC2, PD0 to PD4, PE0 to PE7, PK0	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 

PA3, PC3 to PC5	**(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, External Interrupt Input)** 
PJ0,PJ1	**(Programmable Pull-down, Schmitt Input, Oscillation Circuit)** 

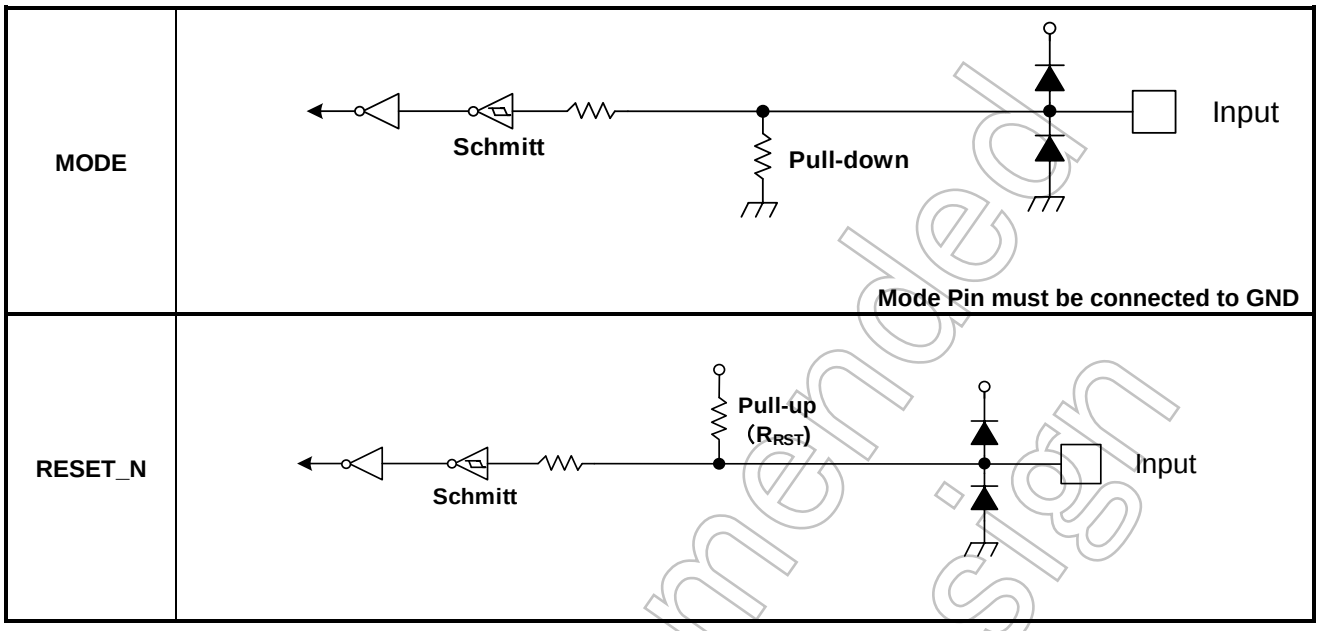
BOOT_N	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 

6.2. Analog Power pin

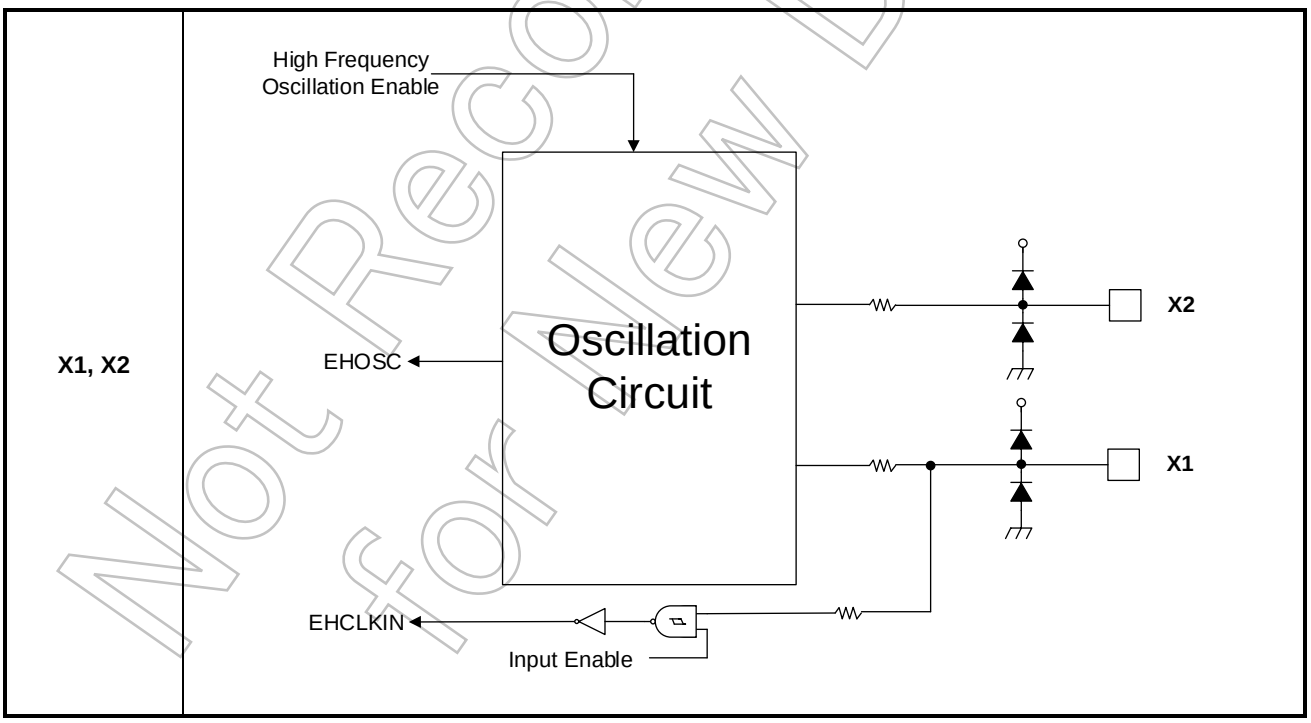


Note: SW: ON/OFF Switch Circuit

6.3. Control Pin



6.4. Clock control



7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5A DVDD5B DVDD5C	-0.3 to 6.0	V
		AVDD5	-0.3 to 6.0	
Capacitor pin voltage for voltage maintenance		REGOUT1	-0.3 to 1.7	V
		REGOUT2	-0.3 to 3.9	
Input voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PJ0, PJ1, PK0, MODE, RESET_N	V_{IN1} V_{IN2}	-0.3 to DVDD5+0.3(≦6.0V) (Note 1)	V
	PF0, PG0 to PG3, PH0, PH1	V_{IN3}	-0.3 to AVDD5+0.3(≦6.0V)	
Low level output current	Per pin PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PF0, PG0 to PG3, PH0, PH1,PK0	I_{OL}	5	mA
	Total of all pins	ΣI_{OL}	50	
High level output current	Per pin PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PF0, PG0 to PG3, PH0, PH1,PK0	I_{OH}	-5	
	Total of all pins	ΣI_{OH}	-50	
Power consumption		PD	470 (Ta=85℃) 230 (Ta=105℃)	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operational temperature		T_{OPR}	-40 to 105	°C

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

7.2. DC Electrical Characteristics (1/2)

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B,DVDD5C AVDD5	VDD	fosc = 6 to 12MHz fsys = 1 to 80MHz	4.5	–	5.5	V
Low level Input voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PJ0, PJ1, PK0, MODE, RESET_N	V_{IL1} V_{IL2}		-0.3	–	DVDD5×0.25	V
	PF0, PG0 to PG3, PH0, PH1	V_{IL3}				AVDD5×0.25	
High level Input voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PJ0, PJ1, PK0, MODE, RESET_N	V_{IH1} V_{IH2}		DVDD5×0.75	–	DVDD5+0.3	V
	PF0, PG0 to PG3, PH0, PH1	V_{IH3}		AVDD5×0.75		AVDD5+0.3	
Low level output voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7,PK0	V_{OL1} V_{OL2}	DVDD5=4.5V I_{OL}=1.6mA	–	–	0.4	V
	PF0, PG0 to PG3, PH0, PH1	V_{OL3}	AVDD5=4.5V I_{OL}=1.6mA	–	–	0.4	
High level output voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7,PK0	V_{OH1} V_{OH2}	DVDD5=4.5V I_{OH}= -1.6mA	DVDD5-0.4	–	–	
	PF0, PG0 to PG3, PH0, PH1	V_{OH3}	AVDD5=4.5V I_{OH}= -1.6mA	AVDD5-0.4	–	–	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note 3: Apply same voltage to DVDD5 and AVDD5.

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V≤VIN≤DVDD5 0.0V≤VIN≤AVDD5	-5	±0.05	5	µA
Output leak current		I_{LO}	0.2≤VIN≤DVDD5-0.2 0.2≤VIN≤AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		V_{TH}	DVDD5 =AVDD5= 5V	-	1.0	-	V
Reset pull-up resistor		R_{RST}		25	30	100	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	25	30	100	
			Pull-down	25	50	100	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin	I_{OL}	DVDD5=5V AVDD5=5V	-	-	2 (Note 4)	mA
	Total of PA3, PB0 to PB3, PC0 to PC3, PD0 to PD4	ΣI_{OL1}	DVDD5=5V	-	-	35 (Note 5)	
	Total of PA0 to PA2, PC4, PC5, PE0 to PE7,PK0	ΣI_{OL2}	DVDD5=5V	-	-	35 (Note 5)	
	Total of PF0, PG0 to PG3, PH0, PH1	ΣI_{OL3}	AVDD5=5V	-	-	20 (Note 5)	
High level output current	Per pin	I_{OH}	VDD5=5V	-2 (Note 4)	-	-	mA
	Total of PA3, PB0 to PB3, PC0 to PC3, PD0 to PD4	ΣI_{OH1}	DVDD5=5V	-35 (Note 5)	-	-	
	Total of PA0 to PA2, PC4 to PC5, PE0 to PE7,PK0	ΣI_{OH2}	DVDD5=5V	-35 (Note 5)	-	-	
	Total of PF0, PG0 to PG3, PH0, PH1	ΣI_{OH3}	AVDD5=5V	-20 (Note 5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note 3: Apply same voltage toDVDD5 and AVDD5.

Note 4: The sum of the pin currents in each group should not exceed the total current of each group.

Note 5: The sum of each group current should not exceed the absolute maximum rating.

2.7V ≤ DVDD5 = AVDD5 < 4.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B,DVDD5C AVDD5	VDD	fosc = 6 to 12MHz fsys = 1 to 40MHz	2.7	-	4.5	V
Low level Input voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PJ0, PJ1, PK0, MODE, RESET_N	V_{IL1} V_{IL2}		-0.3	-	DVDD5×0.25	V
	PF0, PG0 to PG3, PH0, PH1	V_{IL3}				AVDD5×0.25	
High level Input voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7, PJ0, PJ1, PK0, MODE, RESET_N	V_{IH1} V_{IH2}		DVDD5×0.75	-	DVDD5+0.3	V
	PF0, PG0 to PG3, PH0, PH1	V_{IH3}		AVDD5×0.75		AVDD5+0.3	
Low level output voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7,PK0	V_{OL1} V_{OL2}	DVDD5=2.7V I_{OL}=0.8mA	-	-	0.4	V
	PF0, PG0 to PG3, PH0, PH1	V_{OL3}	AVDD5=2.7V I_{OL}=0.8mA	-	-	0.4	
High level output voltage	PA0 to PA3, PB0 to PB3, PC0 to PC5, PD0 to PD4, PE0 to PE7,PK0	V_{OH1} V_{OH2}	DVDD5=2.7V I_{OH}= -0.8mA	DVDD5-0.4	-	-	
	PF0, PG0 to PG3, PH0, PH1	V_{OH3}	AVDD5=2.7V I_{OH}= -0.8mA	AVDD5-0.4	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note 3: Apply same voltage toDVDD5 and AVDD5.

2.7V ≤ DVDD5 = AVDD5 < 4.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V≤VIN≤DVDD5 0.0V≤VIN≤AVDD5	-5	±0.05	5	μA
Output leak current		I_{LO}	0.2≤VIN≤DVDD5-0.2 0.2≤VIN≤AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		V_{TH}	DVDD5 =AVDD5= 3V	-	0.5	-	V
Reset pull-up resistor		R_{RST}		25	100	200	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	25	100	200	
			Pull-down	25	100	200	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin	I_{OL}	DVDD5=3V AVDD5=3V	-	-	1 (Note 4)	mA
	Total of PA3, PB0 to PB3, PC0 to PC3, PD0 to PD4	ΣI_{OL1}	DVDD5=3V	-	-	18 (Note 5)	
	Total of PA0 to PA2,PC4, PC5, PE0 to PE7,PK0	ΣI_{OL2}	DVDD5=3V	-	-	18 (Note 5)	
	Total of PF0, PG0 to PG3, PH0, PH1	ΣI_{OL3}	AVDD5=3V	-	-	10 (Note 5)	
High level output current	Per pin	I_{OH}	DVDD5=3V AVDD5=3V	-1 (Note 4)	-	-	mA
	Total of PA3, PB0 to PB3, PC0 to PC3, PD0 to PD4	ΣI_{OH1}	DVDD5=3V	-18 (Note 5)	-	-	
	Total of PA0 to PA2,PC4, PC5, PE0 to PE7,PK0	ΣI_{OH2}	DVDD5=3V	-18 (Note 5)	-	-	
	Total of PF0, PG0 to PG3, PH0, PH1	ΣI_{OH3}	AVDD5=3V	-10 (Note 5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note 3: Apply same voltage toDVDD5 and AVDD5.

Note 4: The sum of the pin currents in each group should not exceed the total current of each group.

Note 5: The sum of each group current should not exceed the absolute maximum rating.

7.3. DC Electrical Characteristics (2/2) (Consumption current)

Ta = -40 to 105°C

Parameter	Symbol	Conditions			Min	Typ. (Note 2)	Max	Unit
		Supply voltage	High speed oscillator	Operating condition				
NORMAL	I_{DD}	DVDD5= AVDD5= 5.5V	Refer to the table 7.2 and 7.3 for detail		-	15.3	20.3	mA
			Oscillation	CPU only	-	7.2	11.5	
IDLE				Refer to the table 7.2 and 7.3 for detail	-	2.7	6.8	
STOP1			Stop		-	150	3300	μA

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note 3: Apply same voltage to DVDD5 and AVDD5.

Note 4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1
Pin setting	DVDD5= AVDD5=	5.0V(Typ.)、5.5V(max)		
	X1,X2	Oscillator connected (10MHz)		
	Input pins	Fixed		
	Output pins	Open		
Operation condition (Oscillation Circuit)	System clock (fsys)	80MHz		Stop
	External High speed frequency oscillator (EHOSC)	Oscillation		Stop
	Internal High speed frequency oscillator (IHOSC1)	Stop		
	PLL	Run(8 times)		Stop

Table 7.3 IDD measurement condition (CPU, Peripheral)

Peripheral circuit	unit number	NORMAL	IDLE	STOP1
CPU	1	Run (DhrystoneVer.2.1)	Stop	
ADC	1	Run (1.5µs, Repeated conversion)	Stop	
RAMP	1	Run	Stop	
T32A	4	All ch Run	Stop	
PMD+	1	All ch Run	Stop	
A-ENC32	1	Run	Stop	
A-VE	1	Run	Stop	
SIWDT	1	Run	Stop	
UART	3	2 ch: Transmission(5Mbps)	Stop	
TSPI	3	1 ch: Transmission(20MHz)	Stop	
CRC	1	Stop		
LVD	1	Stop		
OFD	1	Stop		
Debug	1	Stop		
Input/Output Port	—	Run	Stop	

fsys = 80MHz
Ta = -40 to 105°C

Item	Symbol	Condition	Min	Typ.	Max	Unit
Power consumption (ADC)	I_{AVDD}	AVDD5=5.0V、AVSS=0V	-	2.7	3.4	mA

7.4. 12-bit AD Converter Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH		AVDD5-0.3	-	AVDD5+0.3	V
Analog input voltage	VAIN		AVSS (VREFL)	-	AVDD5 (VREFH)	V
Integral nonlinear error (INL)	-	4.5V≤AVDD5≤5.5V AVSS=(VREFL)=0V AIN load resistor = 600Ω AIN load capacity ≥ 0.1μF Conversion time ≥ 1.5μs	-3	-	3	LSB
Differential nonlinear error (DNL)			-3	-	3	
Zero-scale error			-5	-	5	
Full-scale error			-5	-	5	
Total errors			-7	-	7	
Integral nonlinear error (INL)	-	2.7V≤AVDD5<4.5V AVSSA=(VREFL)=0V AIN load resistor = 600Ω AIN load capacity ≥0.1μF Conversion time =3.0μs	-4	-	4	LSB
Differential nonlinear error (DNL)			-3	-	3	
Zero-scale error			-6	-	6	
Full-scale error			-6	-	6	
Total errors			-7	-	7	
Stable time	t_{sta}	After ***[ADAMOD0]***<DACON> =1 is set.	3	-	-	μs
Conversion time	t_{conv}	4.5V≤AVDD5≤5.5V	1.5	-	5	
		2.7V≤AVDD5<4.5V	2.95	-	15	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note 3: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 4096 [V]

Note 4: The characteristic when single AD converter operates.

DVDD5 = AVDD5 = 2.7V to 5.5V
DVSS = AVSS = 0V
Ta= -40 to 105°C

Parameter	Conditions	Min	Typ.	Max	Unit
Reference power	ch9 select	1.1	-	1.3	V

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.5. Characteristics of Internal processing at RESET

DVSSA = DVSSB = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Initialized time	t_{IINIT}	Power On	-	-	2.15	ms
Internal processing time	t_{IRST}		0.13	-	0.20	
Waiting time till CPU running	t_{CPUWT}	Cold Reset	12	-	15	µs
		Warm Reset	55	-	72	
Power-on rising gradient	V_{PON}		0.01	-	100	mV/µs

7.6. Characteristics of Power on Reset

DVSSA = DVSSB = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power On	2.25	2.4	2.55	V
	V_{PDET}	Power Down	2.2	2.35	2.5	
Detection pulse width	T_{PDET}		200	-	-	µs

7.7. Characteristics of Voltage Detection Circuit

DVDD5 = AVDD5 = 2.7V to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power On	2.55	2.65	2.75	V
		Power Down	2.5	2.6	2.7	
	V_{LVL1}	Power On	2.65	2.75	2.85	V
		Power Down	2.6	2.7	2.8	
	V_{LVL2}	Power On	2.75	2.85	2.95	V
		Power Down	2.7	2.8	2.9	
	V_{LVL3}	Power On	2.85	2.95	3.05	V
		Power Down	2.8	2.9	3.0	
	V_{LVL4}	Power On	3.95	4.05	4.15	V
		Power Down	3.9	4.0	4.1	
	V_{LVL5}	Power On	4.15	4.25	4.35	V
		Power Down	4.1	4.2	4.3	
	V_{LVL6}	Power On	4.35	4.45	4.55	V
		Power Down	4.3	4.4	4.5	
	V_{LVL7}	Power On	4.55	4.65	4.75	V
		Power Down	4.5	4.6	4.7	
Detection response time	t_{VDDT1}	Power On	-	50	200	µs
Detection Release time	t_{VDDT2}	Power Down	-	250	-	
Setup time	t_{LVDEN}		-	-	100	
Detection Minimum pulse width	t_{LVDPW}		200	-	-	

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.8. AC Electrical Characteristics

7.8.1. Serial Peripheral Interface (TSPI)

7.8.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V, DVSS=AVSS=0V
- Ta = -40 to 105°C
- Output level: High = 0.8×DVDD5、Low = 0.2×DVDD5
- Input level: High = 0.75×DVDD5、Low = 0.25×DVDD5
- Load capacity: CL = 30pF

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.8.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

(1) SIO Master mode

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-12	-	13	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-12	-	13	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	31-(2×T) (Note 1)	-	6	-	
		31-T (Note 2)	-	18.5	-	
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	(2×T)-10 (Note 1)	-	15	-	
		T-10 (Note 2)	-	2.5	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-9	-	-9	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	9	-	9	

Note 1: When ***[TSPIxCR2]***<RXDLY>=1

Note 2: When ***[TSPIxCR2]***<RXDLY>=0

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	15	-	13.3 (Note1)	MHz
TSPIxSCK output cycle	t_{CYC}	66.7	-	75	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-17	-	21	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-17	-	21	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	41-(2×T) (Note 2)	-	16	-	
		41-T (Note 3)	-	28.5	-	
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	(2×T)-11 (Note 2)	-	14	-	
		T-11 (Note 3)	-	1.5	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-14	-	-14	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	12	-	12	

Note1: The output frequency is determined by the setting value of ***[TSPIxBR]***<BRCK><BRS>. When set the output frequency within the range not exceeding, it becomes 13.3MHz.

Note 2: When ***[TSPIxCR2]***<RXDLY>=1

Note 3: When ***[TSPIxCR2]***<RXDLY>=0

(2) SIO Slave mode

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	15	-	13.3 (Note)	MHz
TSPIxSCK Input cycle	t_{CYC}	66.7	-	75	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	10	-	10	-	
TSPIxSCK high level Input pulse width	t_{WH}	10	-	10	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	6	-	6	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	33	-	33	

Note: The output frequency is determined by the setting value of ***[TSPIxBR]***<BRCK><BRS>. When set the output frequency within the range not exceeding, it becomes 13.3MHz.

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	10	-	10	-	
TSPIxSCK high level Input pulse width	t_{WH}	10	-	10	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	6	-	6	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	45	-	45	

(1) 1st clock edge sampling (Master)

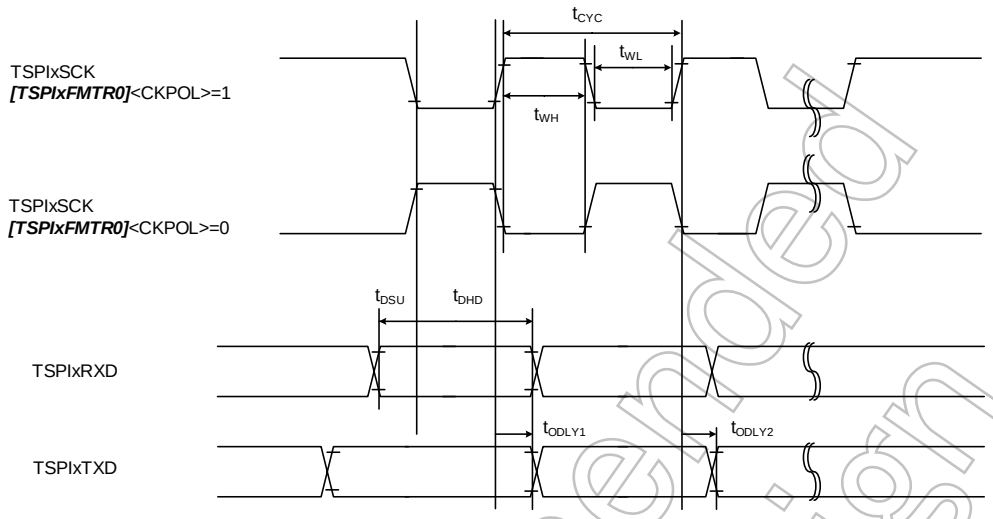


Figure 7.1 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

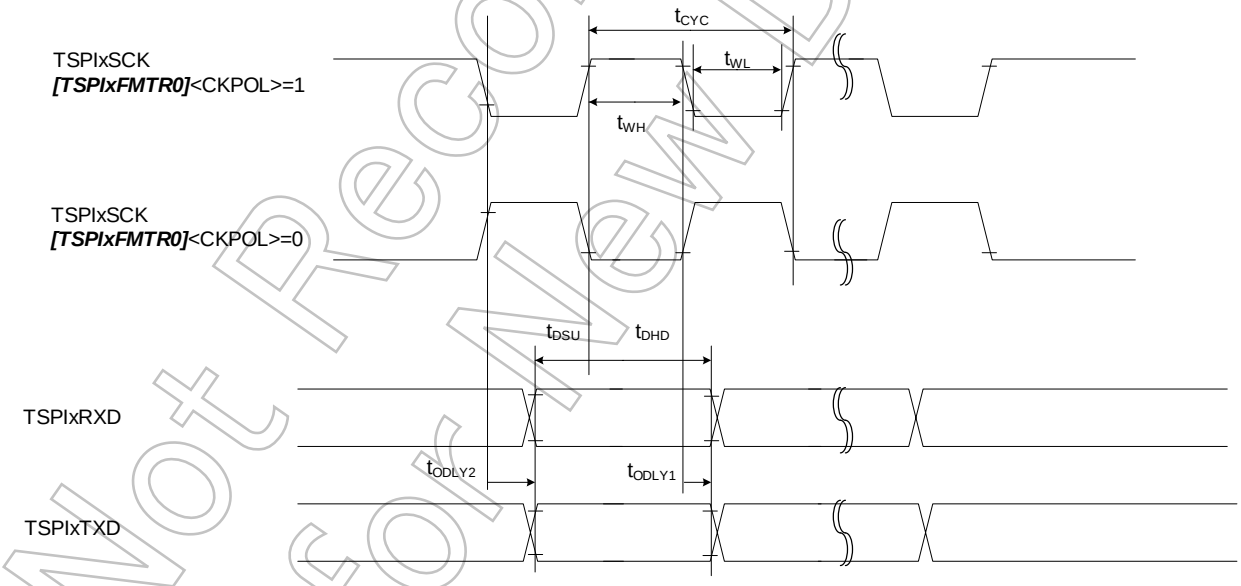


Figure 7.2 2nd clock edge sampling (Master)

(3) 2nd clock edge sampling (slave)

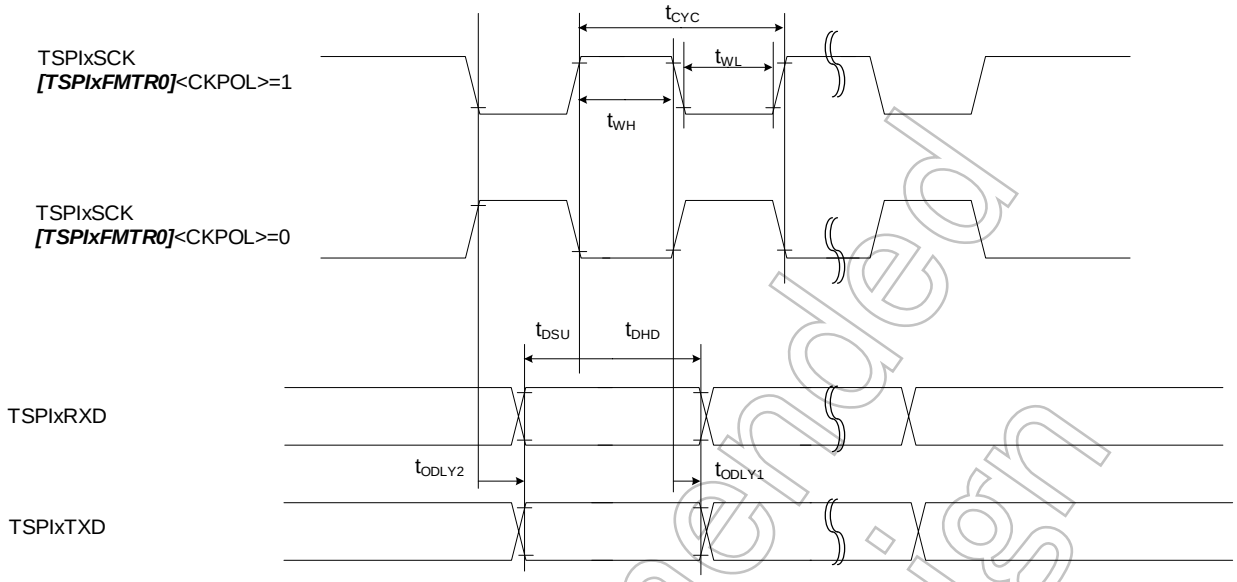


Figure 7.3 2nd clock edge sampling (Slave)

7.8.2. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0, T32AxINB0, and T32AxINC0.

7.8.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75×DVDD5、Low = 0.25×DVDD5
- Load capacity: CL = 30pF

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.8.2.2. AC Electrical Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0 clock. This cycle is depending on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Calculation		ΦT0=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	45	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	45	-	

(2) At the pulse count

Parameter	Symbol	Calculation		ΦT0=80MHz		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	

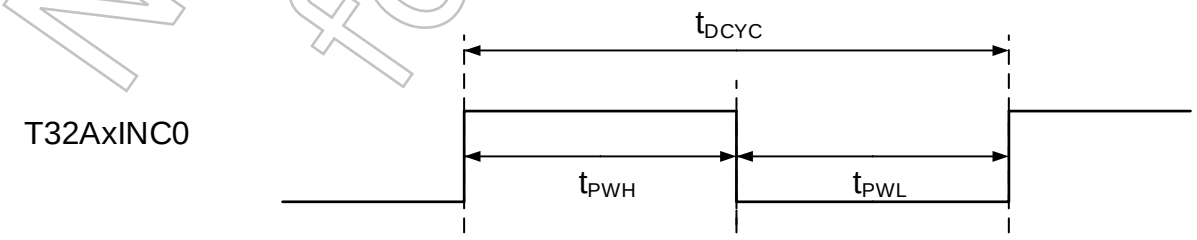


Figure 7.4 Count Pulse input

7.8.3. External Interrupt

7.8.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75×DVDD5、Low = 0.25×DVDD5
- Load capacity: CL = 30pF

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.8.3.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL,IDLE mode

Parameter	Symbol	Calculation		fsys=80MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	112.5	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	112.5	-	

(2) STOP1 mode

Parameter	Symbol	Calculation		fsys=80MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	125	-	125	-	ns
High level pulse width	t_{INTCH2}	125	-	125	-	

7.8.4. Debug Communication

7.8.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.8×DVDD5、Low = 0.2×DVDD5
- Input level: High = 0.75×DVDD5、Low = 0.25×DVDD5
- Load capacity: CL = 30pF

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.8.4.2. SWD Interface

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from rising edge of CLK	t_{d1}	4	-	
Output data valid from rising edge of CLK	t_{d2}	-	30	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from rising edge of CLK	t_{dh}	15	-	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from rising edge of CLK	t_{d1}	4	-	
Output data valid from rising edge of CLK	t_{d2}	-	45	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from rising edge of CLK	t_{dh}	15	-	

7.8.4.3. JTAG Interface

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	83.3	-	ns
Output data hold from rising edge of CLK	t_{d3}	4	-	
Output data valid from rising edge of CLK	t_{d4}	-	33	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from rising edge of CLK	t_{dh}	15	-	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	83.3	-	ns
Output data hold from rising edge of CLK	t_{d3}	4	-	
Output data valid from rising edge of CLK	t_{d4}	-	45	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from rising edge of CLK	t_{dh}	15	-	

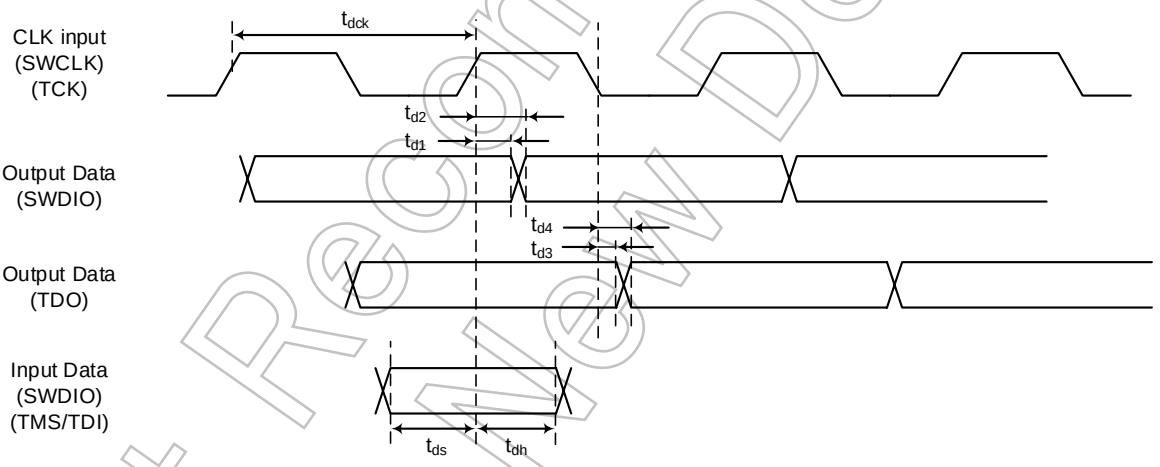


Figure 7.5 JTAG/SWD waveform

7.8.5. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	DVDD5 = 2.7 to 5.5V Ta = -40 to 105°C	15	30	60	ns

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.8.6. External Clock Input

7.8.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75×DVDD5、Low = 0.25×DVDD5
- Load capacity: CL = 30pF

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.8.6.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency ($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	12	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

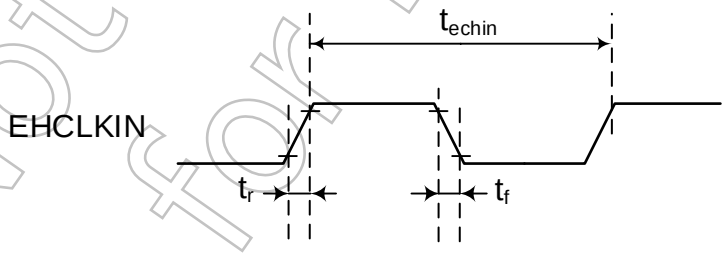


Figure 7.6 External clock input waveform

7.9. Flash Memory Characteristics

7.9.1. Code Flash

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	DVDD5=2.7V to 5.5V Ta= -40 to 105°C	-	-	10,000	cycles
Programming time	Word Program time	-	29.5	-	µs
Erase time	Page Erase time	1.1	-	4.3	ms
	Block Erase time	8.6	-	34	
	Area Erase time(Note2)	-	9.2	-	

Note1 : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note2: No block with effective protection.

7.9.2. Chip Erase

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Erasing of Code Flash, Protect Bits(Code), User Information Area and Security Bits	12.5	-	22.1	ms

Note1 : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note2: When Chip Erase command executes, no block with effective protection.

7.10. Regulator

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor	DVDD5=2.7V to 5.5V Ta=-40 to 105°C	-	4.7	-	µF
Capacitance of REGOUT2 capacitor		-	4.7	-	

Note : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

7.11. Oscillation Circuit

7.11.1. Internal Oscillation

DVDD5=2.7V to 5.5V
Ta= -30 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}		9.87	10	10.13	MHz

Note1 : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note2: Included the influence(package, reflow) depend on the variations after Factory shipping.

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	Factory out, IC data	-	10	-	MHz
	f_{IHOSC2}		-	10	-	

Note1 : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note2: Not included the influence(package, reflow) depend on the variations after Factory shipping. Please execute oscillator adjustment by the trimming register, if trimming of IHOSC1 is required. However, IHOSC2 cannot execute trimming.

7.11.2. External Oscillator

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}		6	-	12	MHz

Note1 : DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, and DVSSB.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

7.11.3. Oscillation Circuit

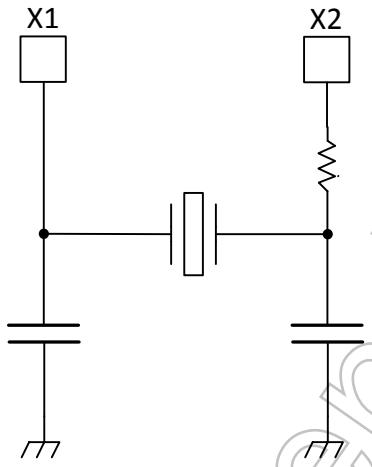


Figure 7.7 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

7.11.4. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.

Please refer to the company's website for details.

7.11.5. Crystal Oscillator

This product has been evaluated by the crystal oscillator by KYOCERA Corporation.

Please refer to the company's website for details.

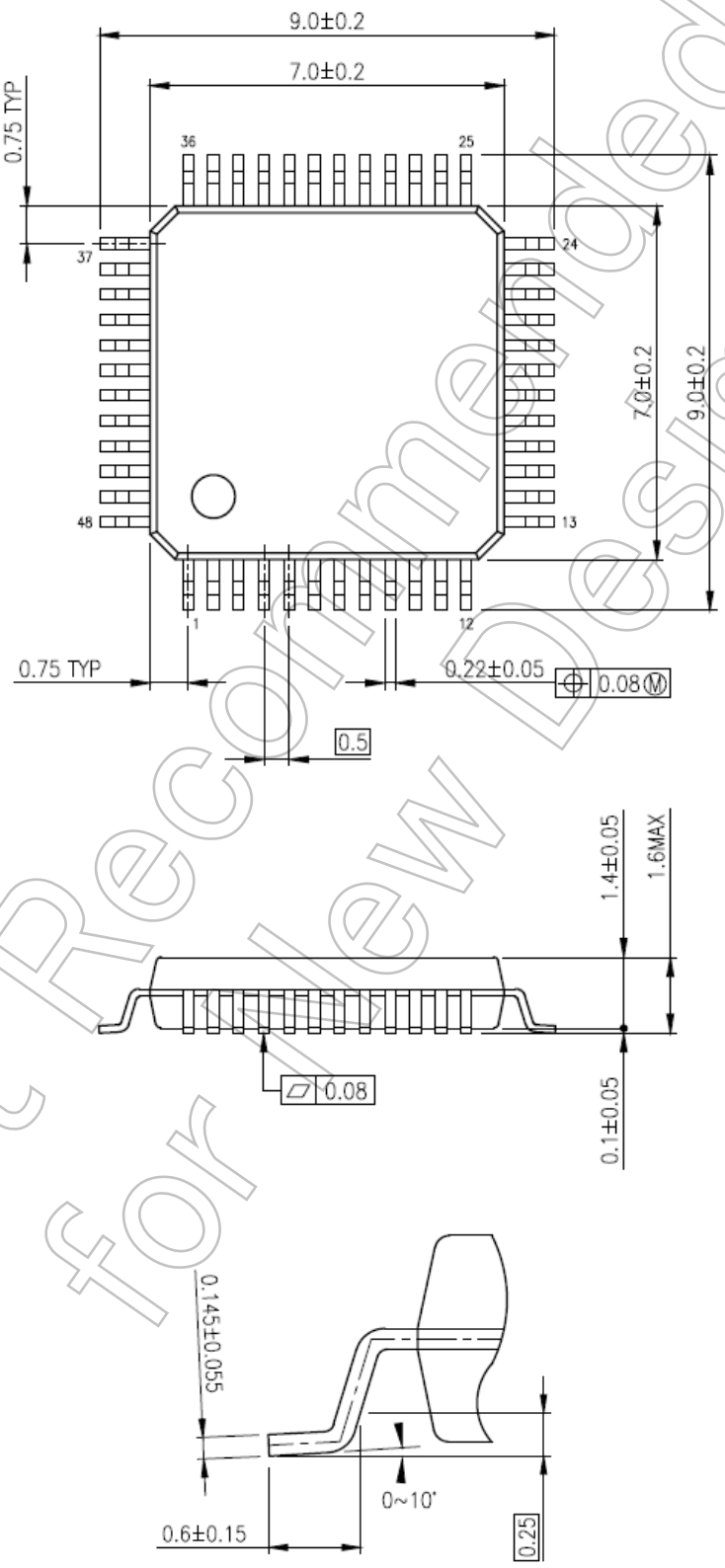
7.11.6. Precautions for designing printed circuit board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

8. Package Dimensions

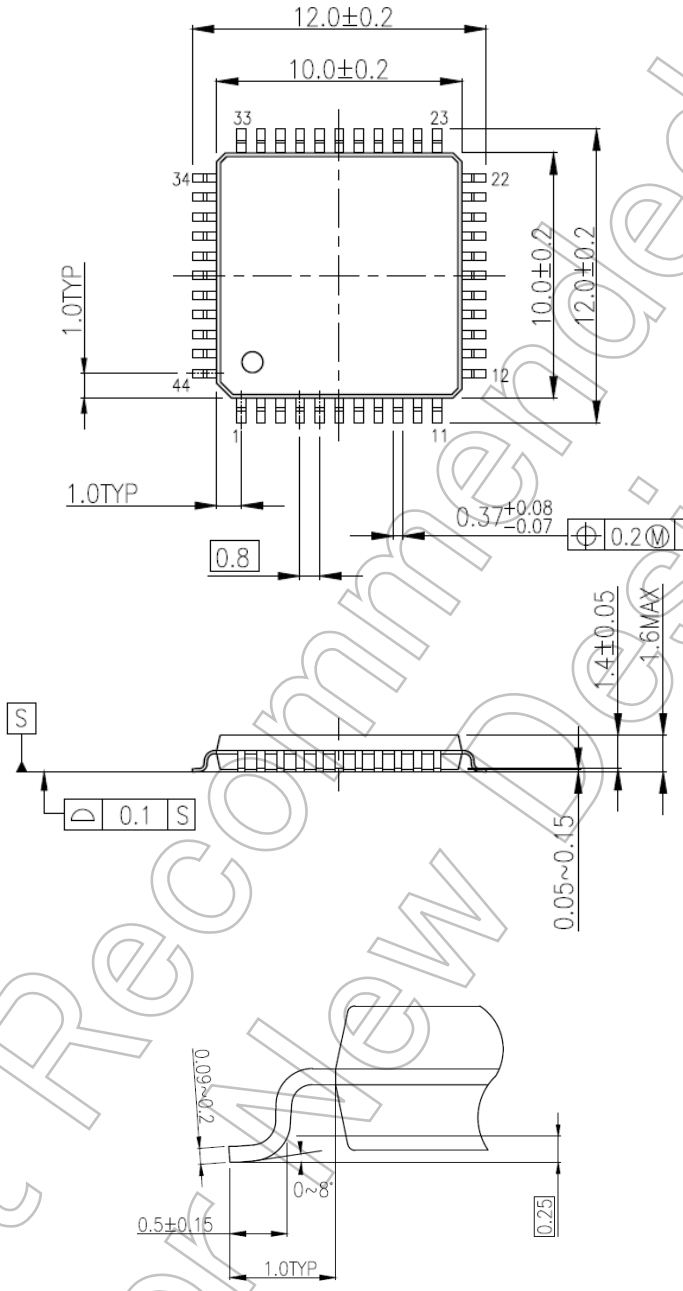
8.1. LQFP48-P-0707-0.50D

Unit: mm



8.2. LQFP44-P-1010-0.80B

Unit: mm



9. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power on

At power on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.
When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.
Also, when a reset is performed by the internal power on reset, pins of the MCUs that use the internal power on reset are undefined until power supply voltage reaches the voltage at which power on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.
Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.
We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
1.0	2018-12-18	-First release
1.1	2019-08-20	- Layout changed about the Date and the Copyright -Added “Start of commercial production” -6.3 Control Pin Added Pull-up symbol of RESET_N -7.4 12-bit AD Converter Characteristics Modified “Conversion time” 3 to 2.95 -7.7 Characteristics of Voltage Detection Circuit Corrected Min/Max value of V_{LVL4} to V_{LVL7} -7.8.1.2 AC Electrical Characteristics(TSPI) Deleted k1,k2 explanation -7.8.2.2 AC Electrical Characteristics(T32A) Modified fsys=80MHz to ΦT0=80MHz

Appendix
List of All pins

Combination Function A to B: These are the functions which become effective without setting up port function registers.

Combination Function 1 to 6: These are the functions which become effective with setting up port function registers.

M4L2 LQFP 48	M4L1 LQFP 44	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/ Output	PU/PD	OD	SMT/ CMOS	Under Reset	After Reset
1	-	PK0									I/O	PU/PD	YES	SMT	Hi-z	Hi-z
2	1	PE0			UO0						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
3	2	PE1			XO0						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
4	3	PE2			VO0						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
5	4	PE3			YO0						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
6	5	PE4			WO0						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
7	6	PE5			ZO0						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
8	7	PE6			EMG0_N						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
9	8	PE7			OVV0_N						I/O	PU/PD	YES	SMT	Hi-z	Hi-z
10	9	DVSSA									-	-	-	-	-	-
11	10	DVDD5A									-	-	-	-	-	-
12	11	PD0	BOOT_N		T32A00INA0	T32A00OUTA	T32A00INC0	T32A00OUTC			I/O	PU/PD	YES	SMT	Hi-z (Note1)	Hi-z
13	12	PB3			TDI						I/O	PU/PD	YES	SMT	PU (Note2)	PU (Note 2)
14	13	PB2			TDO/SWV						I/O	PU/PD	YES	SMT	Hi-z (Note2)	Hi-z (Note2)
15	14	PB1			TCK/SWCLK						I/O	PU/PD	YES	SMT	PD (Note 2)	PD (Note 2)
16	15	PB0			TMS/SWDIO						I/O	PU/PD	YES	SMT	PU (Note 2)	PU (Note 2)
17	16	PC0			TSPI0TXD	UT0TXDA	UT0RXD				I/O	PU/PD	YES	SMT	Hi-z	Hi-z
18	17	PC1			TSPI0RXD	UT0RXD	UT0TXDA				I/O	PU/PD	YES	SMT	Hi-z	Hi-z
19	18	PC2			TSPI0SCK	UT0CTS_N					I/O	PU/PD	YES	SMT	Hi-z	Hi-z
20	19	PC3		INT00	T32A01INA0	T32A01OUTA	T32A01INC0	T32A01OUTC			I/O	PU/PD	YES	SMT	Hi-z	Hi-z
21	20	PD1			ENC0A	TSPI1SCK	UT1CTS_N				I/O	PU/PD	YES	SMT	Hi-z	Hi-z
22	21	PD2			ENC0B	TSPI1TXD	UT1TXDA	UT1RXD			I/O	PU/PD	YES	SMT	Hi-z	Hi-z
23	22	PD3			ENC0Z	TSPI1RXD	UT1RXD	UT1TXDA			I/O	PU/PD	YES	SMT	Hi-z	Hi-z
24	-	PD4			T32A00INB0	T32A00OUTB					I/O	PU/PD	YES	SMT	Hi-z	Hi-z
25	-	PA3		INT07	T32A01INB0	T32A01OUTB					I/O	PU/PD	YES	SMT	Hi-z	Hi-z
26	23	DVDD5B									-	-	-	-	-	-
27	24	PJ0	X1	EHCLKIN							Input	PD	N/A	SMT	Hi-z	Hi-z
28	25	DVSSB									-	-	-	-	-	-
29	26	PJ1	X2								Input	PD	N/A	SMT	Hi-z	Hi-z
30	27	REGOUT1									-	-	-	-	-	-
31	28	MODE									-	PD	YES	SMT	-	-
32	29	DVDD5C									-	-	-	-	-	-
33	30	REGOUT2									-	-	-	-	-	-
34	31	RESET_N									-	PU	YES	SMT	-	-
35	32	PF0	AINA00								I/O	PU/PD	YES	SMT	Hi-z	Hi-z
36	33	PG0	AINA01								I/O	PU/PD	YES	SMT	Hi-z	Hi-z
37	-	PG3	AINA02								I/O	PU/PD	YES	SMT	Hi-z	Hi-z
38	34	PG1	AINA03	INT01							I/O	PU/PD	YES	SMT	Hi-z	Hi-z
39	35	PG2	AINA04	INT02							I/O	PU/PD	YES	SMT	Hi-z	Hi-z
40	36	PH0	AINA05	INT03							I/O	PU/PD	YES	SMT	Hi-z	Hi-z
41	37	PH1	AINA06	INT04							I/O	PU/PD	YES	SMT	Hi-z	Hi-z
42	38	AVSS									-	-	-	-	-	-
43	39	AVDD5									-	-	-	-	-	-
44	40	PC5		INT05	T32A02INB0	T32A02OUTA	T32A02OUTC				I/O	PU/PD	YES	SMT	Hi-z	Hi-z

M4L2 LQFP 48	M4L1 LQFP 44	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/ Output	PU/PD	OD	SMT/ CMOS	Under Reset	After Reset
45	41	PC4		INT06	T32A02INA0	T32A02OUTB	T32A02INC0				I/O	PU/PD	YES	SMT	Hi-z	Hi-z
46	42	PA2			T32A03INA0	T32A03OUTB	T32A03OUTC	UT2TXDA	UT2RXD	TSPI2RXD	I/O	PU/PD	YES	SMT	Hi-z	Hi-z
47	43	PA1			T32A03INB0	T32A03OUTA	T32A03INC0	UT2RXD	UT2TXDA	TSPI2TXD	I/O	PU/PD	YES	SMT	Hi-z	Hi-z
48	44	PA0			UT2CTS_N	TSPI2SCK					I/O	PU/PD	YES	SMT	Hi-z	Hi-z

Note 1: Combination with BOOT_N. When RESET_N=0, Pull-up resistor is enabled. When RESET_N=1, the pin state is Hi-z with internal reset.

Note 2: It is assigned to a debugging pin in the state of the initial stage. (PB3: TDI, PB2: TDO/SWV, PB0: TMS/SWDIO, PB1: TCK/SWCLK) When receiving the command from TOOL, PB2: TDO/SWV becomes output.

Part Naming Conventions

TMP M4L 2 F W x UG

Toshiba microcontrollers

Revision

Package

Symbol	Package
QG	Plastic shrink quad outline non-leaded package; dry-packed
UG.DUG,FG, DFG	Plastic quad flat package; dry-packed
MG,DMG	Plastic small-outline package; dry-packed
XBG	Plastic ball grid array; dry-packed

Core

Symbol	Core
M4	Arm Cortex-M4 processor with FPU
M3	Arm Cortex-M3
M0	Arm Cortex-M0

Product Group

Family	Group	Application
TXZ	H	For General-purpose/Consumer electronic equipment
	G	For OA/Digital equipment/industrial equipment
	K	For Motor/Inverter control industrial equipment(MCU+AMP/COMP)
	L	For Motor/Inverter control industrial equipment
	P	For Healthcare/ Battery equipment

ROM size

Symbol	Size[KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
10	1,023
15	1,536
20	2,048
40	4,096
80	8,192

Pin Count

Symbol	Pin count	Symbol	Pin count
0, G	Under 32 pin	8, Q	129 pin to 144 pin
1, H	33 pin to 44 pin	9, R	145 pin to 176 pin
2, J	45 pin to 48 pin	A, S	177 pin to 200 pin
3, K	49 pin to 52 pin	B, T	201 pin to 220 pin
4, L	53 pin to 64 pin	C, U	221 pin to 240 pin
5, M	65 pin to 80 pin	D, V	241 pin to 260 pin
6, N	81 pin to 100 pin	E, W	261pin to 280 pin
7, P	101 pin to 128 pin	F, Y	281 pin to 300 pin

ROM type

Symbol	Type
F	Flash
C	Mask

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