32-bit RISC Microcontroller

TXZ Family

Reference Manual
Programmable Motor Control Circuit plus
(PMD+-B)

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder Input Circuit (32bit)
A-VE	Advanced Vector Engine
PMD	Programmable Motor Control Circuit Plus
PWM	Pulse Width Modulation

1. Outlines

The programmable motor control circuit plus (PMD) can operate as a motor control circuit of 1 channel per unit. The following is a list of functions. The following is a list of functions.

Function Classification	Function	Operation
Output waveform generation	Resolution	The count resolution of PWM carrier: 1/fsys or 4/fsys. Resolution of PWM period and Duty Saw-tooth wave carrier: 1/fsys or 4/fsys Triangular wave carrier: 2/fsys or 8/fsys
	PWM generation	PWM carrier waveform: Saw-tooth wave or Triangular wave 3-phase PWM can be generated with three comparators. 3-phase mode: 3-phase common duty or 3-phase independent duty
	Output waveform (Conduction control)	Each of the U/X, V/Y and W/Z phases can be selected PWM or High/Low output. Upper-phase output or lower-phase output respectively can be set to low-active or high-active. This function has the common PWM carrier waveform and generates independent 3-phase complementary PWM.
Trigger generation	Synchronous trigger generation	It generates a synchronous sampling signal that starts AD conversion at an arbitrary timing synchronized with the PWM carrier.
Buffer function	—	PWM period, Duty, Synchronous trigger timing, and 6 port output setting are double-buffered. These setting can be changed during operation. Update timing can be selected by Asynchronous, Carrier bottom, Carrier peak and Carrier peak/bottom.
Protection function	Protection control	This function stop output by protection signal input (OFF output or output disabled) Two types of protection function: EMG and OVV. OVV can be selected monitor function of ADC for protection input.
	Dead time control	The dead time control inserts the dead time for preventing short-circuit at switching between the upper-phase and lower-phase (U/X, V/Y, W/Z). The complementary PWM is output.
Interrupt request	PWM interrupt	PWM interrupt request is generated at a synchronous timing with the PWM period. - Interrupt timing: PWM carrier bottom or PWM carrier peak - Interrupt frequency: Half PWM period, one PWM period, two PWM period, or four PWM period.
	EMG interrupt	This interrupt request is generated by the EMG protection of EMGx_N input
	OVV interrupt	This interrupt request is generated by the OVV protection of OVV input

The PMD realizes 3-phase motor control including Vector control when it cooperates with an advanced vector engine (hereafter, abbreviated as VE), an analog to digital converter (hereafter, abbreviated as ADC), and an advanced encoder input circuit (32-bit) (hereafter, abbreviated as A-ENC).

The pulse width modulation circuit, the conduction control circuit, and the synchronous trigger generation circuit can be controlled by the VE. The synchronous trigger generation circuit can start operating ADC. The conduction control circuit can perform commutation control by trigger input signal from the A-ENC.

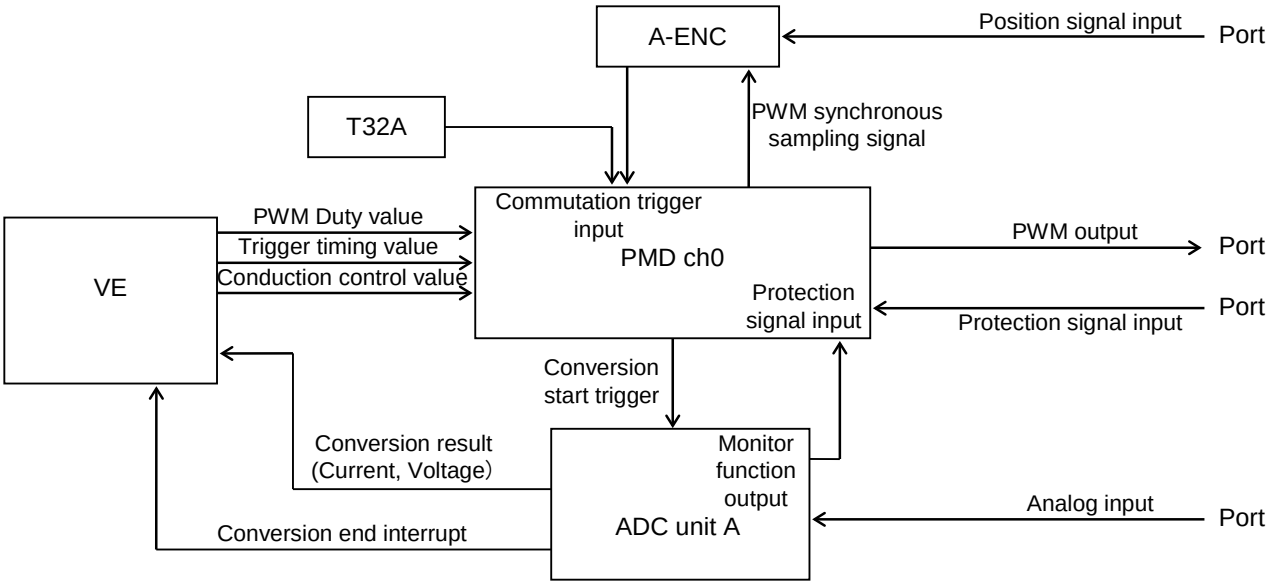


Figure 1.1 Functions related to PMD

2. Configuration

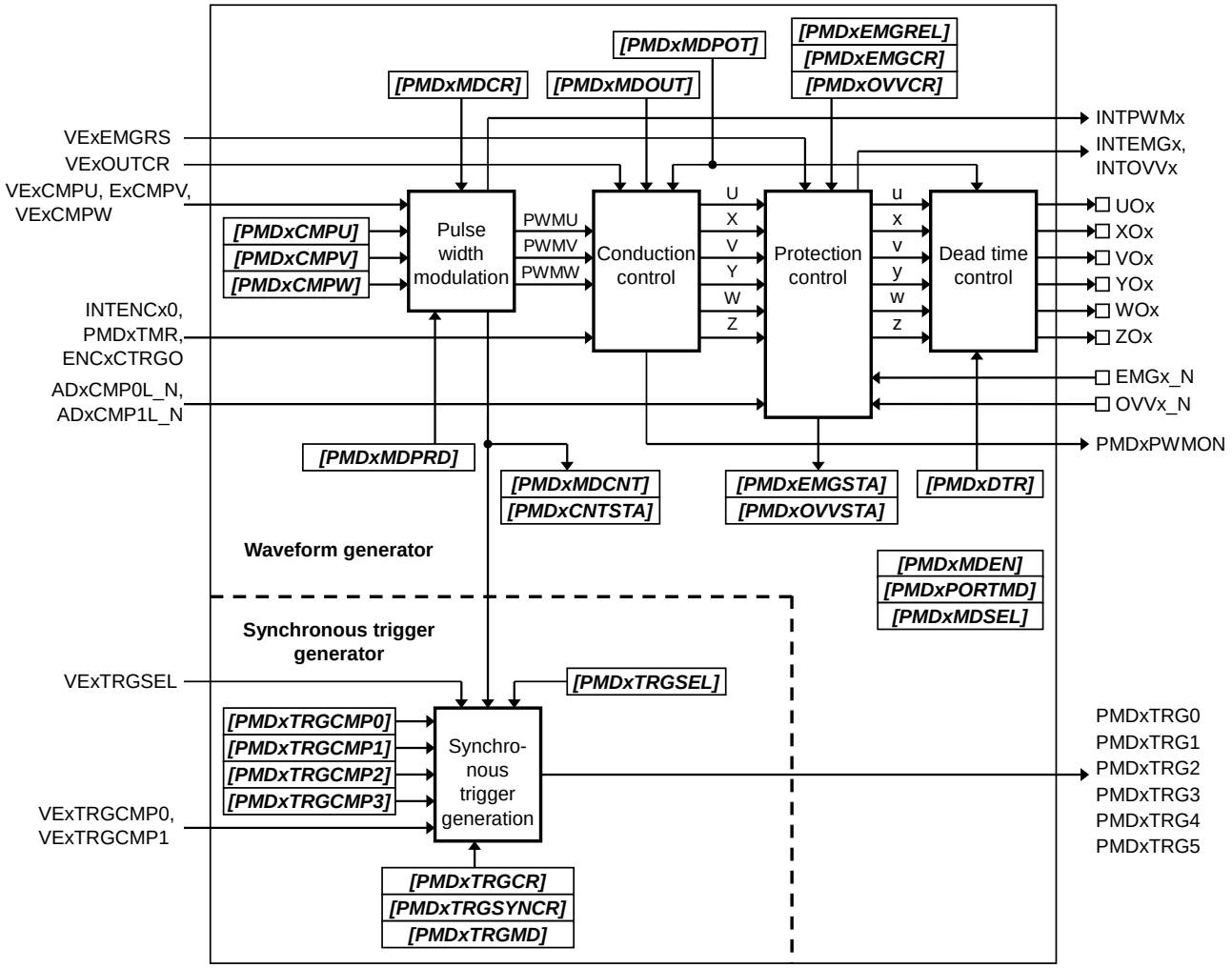


Figure 2.1 PMD Block diagram

Table 2.1 List of signals

No	Signal name		I/O	Related Reference manual
1	UOx	U-phase output pin	Output	Product Information
2	XOx	X-phase output pin	Output	Product Information
3	VOx	V-phase output pin	Output	Product Information
4	YOx	Y-phase output pin	Output	Product Information
5	WOx	W-phase output pin	Output	Product Information
6	ZOx	Z-phase output pin	Output	Product Information
7	EMGx_N	EMG detection input pin	Input	Product Information
8	OVVx_N	OVV detection input pin	Input	Product Information
9	PMDxPWMON	PWM signal for the encoder input	Output	Product Information
10	INTENCx0	Commutation trigger (A-ENC position detection synchronization)	Input	Product Information
11	PMDxTMR	Commutation trigger (General-purpose timer synchronization)	Input	Product Information
12	ENCxCTRGO	Commutation trigger (A-ENC MCMP completion synchronization)	Input	Product Information
13	ADxCMP0L_N	OVV state signal (AD monitor function 0)	Input	Product Information
14	ADxCMP1L_N	OVV state signal (AD monitor function 1)	Input	Product Information
15	PMDxTRG0	ADC synchronous sampling output 0	Output	Product Information
16	PMDxTRG1	ADC synchronous sampling output 1	Output	Product Information
17	PMDxTRG2	ADC synchronous sampling output 2	Output	Product Information
18	PMDxTRG3	ADC synchronous sampling output 3	Output	Product Information
19	PMDxTRG4	ADC synchronous sampling output 4	Output	Product Information
20	PMDxTRG5	ADC synchronous sampling output 5	Output	Product Information
21	INTPWMx	PWM interrupt	Output	Exception, Product Information
22	INTEMGx	EMG interrupt	Output	Exception
23	INTOVVx	OVV interrupt	Output	Exception
24	VExCMPU	VE U-phase PWM duty	Input	Product Information
25	VExCMPV	VE V-phase PWM duty	Input	Product Information
26	VExCMPW	VE W-phase PWM duty	Input	Product Information
27	VExTRGCMP0	VE Trigger compare 0	Input	Product Information
28	VExTRGCMP1	VE Trigger compare 1	Input	Product Information
29	VExTRGSEL	VE Synchronous trigger output selection	Input	Product Information
30	VExOUTCR	VE Conduction control / output control	Input	Product Information
31	VExEMGRS	VE EMG return	Input	Product Information

3. Function and Operation

The PMD circuit consists of two blocks of a wave generation circuit and a synchronous trigger generation circuit. The wave generation circuit includes a pulse width modulation circuit, a conduction control circuit, a protection control circuit, and a dead time control circuit.

- The pulse width modulation circuit has the common PWM carrier waveform and generates independent 3-phase PWM waveforms.
- The conduction control circuit determines the output pattern for each of the upper and lower sides of the U-, V-, and W-phases.
- The protection control circuit controls emergency output stop by EMG input and OVV input.
- The dead time control circuit prevents a short circuit which may occur when the upper side and lower side are switched.
- The synchronous trigger generation circuit generates synchronous trigger signals to the ADC for starting AD conversion.

3.1. Clock Supply

When using PMD, set an applicable clock enable bit to "1" (clock supply) in Clock supply and stop register A for fsys (***[CGFSYSENA]***, ***[CGFSYSMENA]***), Clock supply and stop register B for fsys (***[CGFSYSENB]***, ***[CGFSYSMENB]***), and Clock supply and stop register for fc (***[CGFCEN]***). An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

3.2. Pulse Width Modulation Circuit

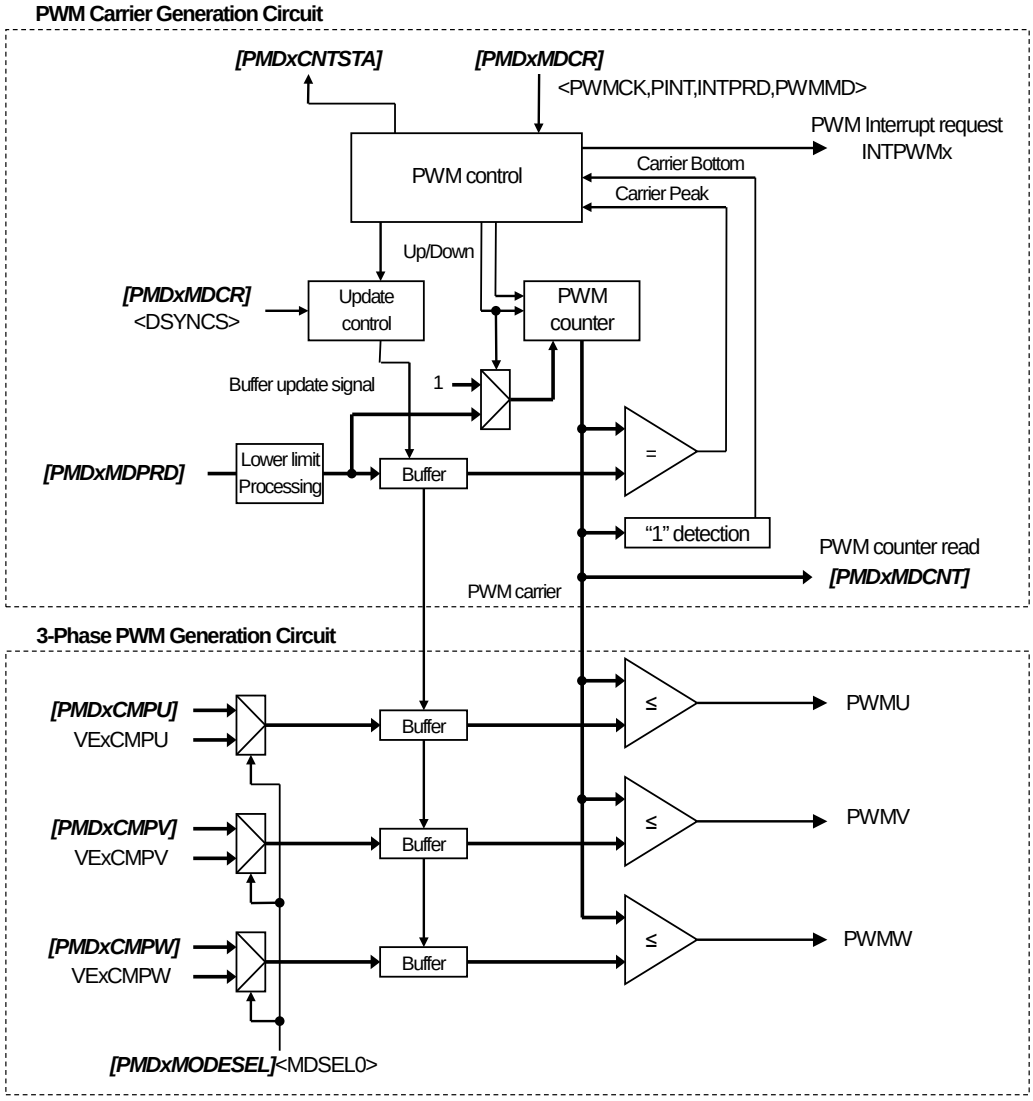


Figure 3.1 Pulse Width Modulation Circuit

The pulse width modulation circuit has a 16-bit PWM up/down-counter and generates PWM carrier waveforms with a resolution of 1/fsys. The PWM period extension mode (***[PMDxMDCR]***<PWMCK>=1) is also available. When this mode is selected, the PWM counter generates PWM carrier waveforms with a resolution of 4/fsys.

The PWM carrier waveform mode can be selected from mode 0 (edge-aligned PWM, saw-tooth waveform) and mode 1 (center-aligned PWM, triangular waveform). (Refer to "Figure 3.2 PWM Waveforms".)

3.2.1. Setting the PWM period

The PWM period is determined by the ***[PMDxMDPRD]*** register. This register is double-buffered.

The subsequent stage buffer is updated at every PWM period. It is also possible to update at every half PWM period. (Refer to "Table 4.1 ***[PMDxMDPRD]***, ***[PMDxCMPU/V/W]*** buffer Update Timing".)

Sawtooth wave PWM : ***[PMDxMDPRD]*** value = $\frac{\text{System clock fsys [Hz]}}{\text{PWM frequency [Hz]}}$

Triangular wave PWM : ***[PMDxMDPRD]*** value = $\frac{\text{System clock fsys [Hz]}}{\text{PWM frequency [Hz]} \times 2}$

3.2.2. Compare function

The pulse width modulation circuit generates PWM waveforms of the desired duty by comparing the magnitude of the 3 phase PWM compare registers (***[PMDxCMPU]***, ***[PMDxCMPV]***, ***[PMDxCMPW]***) and the PWM carrier which is generated by the PWM counter (***[PMDxMDCNT]***).

The PWM compare register of each phase has a double-buffered register. The PWM compare register value is loaded into the subsequent stage buffer at every PWM period. It is also possible to update at every half a PWM period. (Refer to "Table 4.1 ***[PMDxMDPRD]***, ***[PMDxCMPU/V/W]*** buffer Update Timing".)

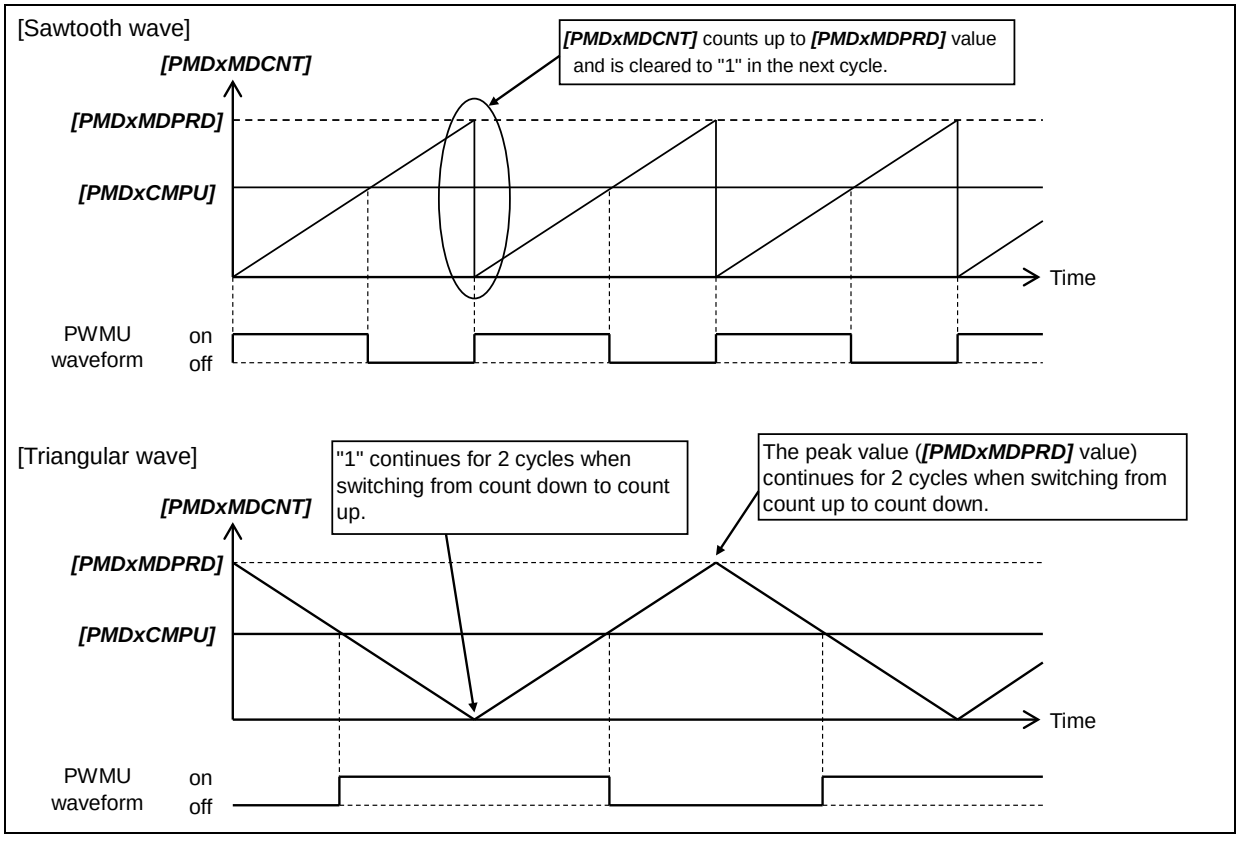


Figure 3.2 PWM Waveforms

When triangular wave carrier, the PWM waveform of each phase is selected from the center-aligned PWM, the falling edge fixed PWM and the rising edge fixed PWM by ***[PMDxMDCR]***<nPWMES>(n = U,V,W) setting. (Refer to "Figure 3.3 Waveforms of PWM triangular wave carrier using fixed edge").

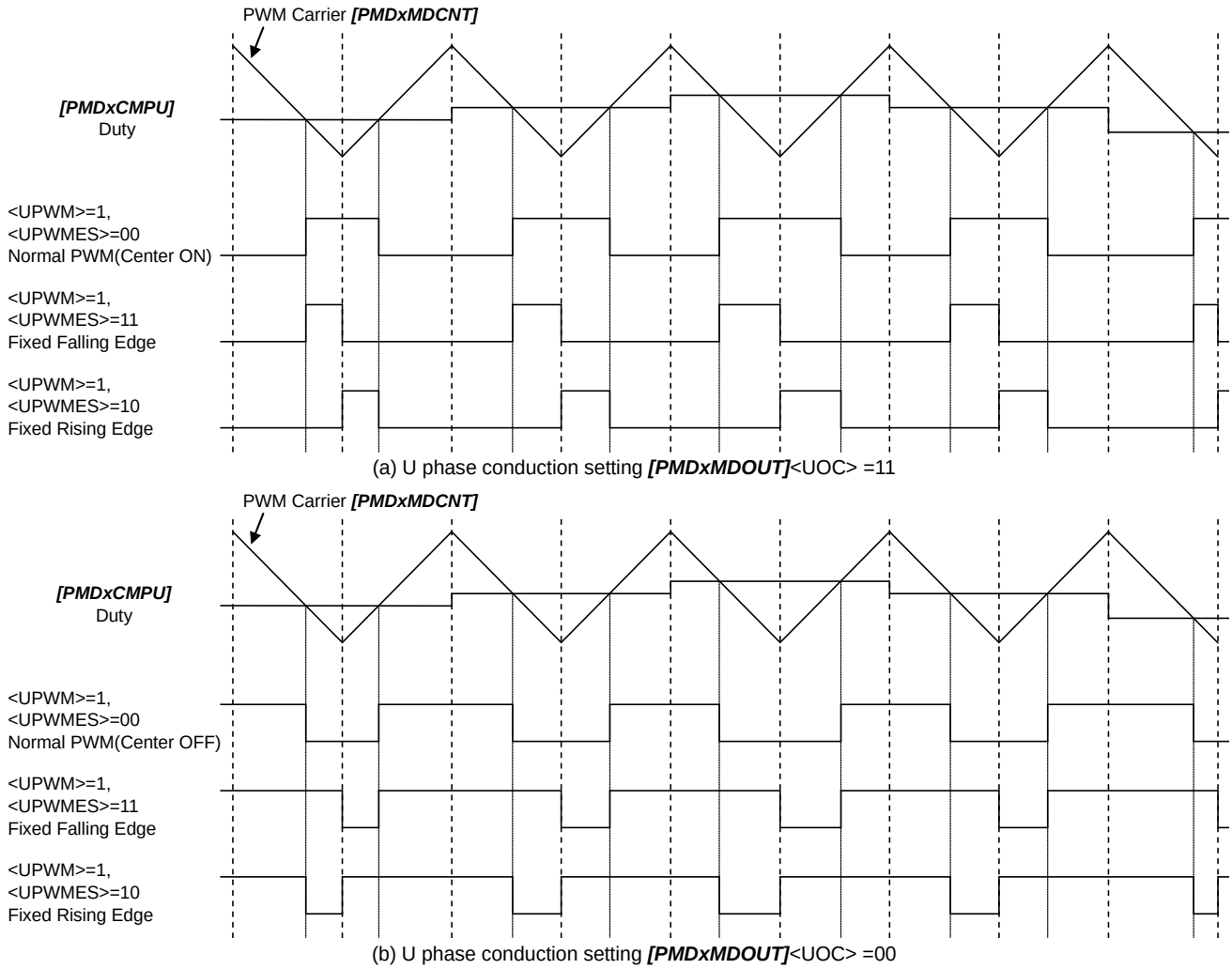


Figure 3.3 Waveforms of PWM triangular wave carrier using fixed edge

Also, PWM output of each phase of 3 phase PWM, can be switched between the center-on PWM and the center-off PWM with combination of ***[PMDxMDOUT]***<nOC>, <nPWM>(n=U, V, W), and ***[PMDxMDCR]***<SYNTMD> (Refer to "3.3 Conduction Control Circuit").

3.2.3. Waveform mode

3-phase PWM waveforms can be generated in the following two modes by ***[PMDxMDCR]***<DTYMD> setting:

- 3-phase independent mode:

  Each of the PWM compare registers for the three phases is set independently to generate independent PWM waveforms for each phase. This mode is used to generate drive waveforms such as sinusoidal waves.

- 3-phase common mode:

  Only the U-phase PWM compare register is set to generate identical PWM waveforms for all the three phases. This mode is used for rectangular wave drive of brushless DC motors.

3.2.4. Interrupt processing

The pulse width modulation circuit generates PWM interrupt requests in synchronization with PWM waveforms. Interrupt request timing can be selected either at PWM carrier peak or at PWM carrier bottom.

The frequency of PWM interrupts can be set to half a PWM period, one PWM period, two PWM periods or four PWM periods.

3.3. Conduction Control Circuit

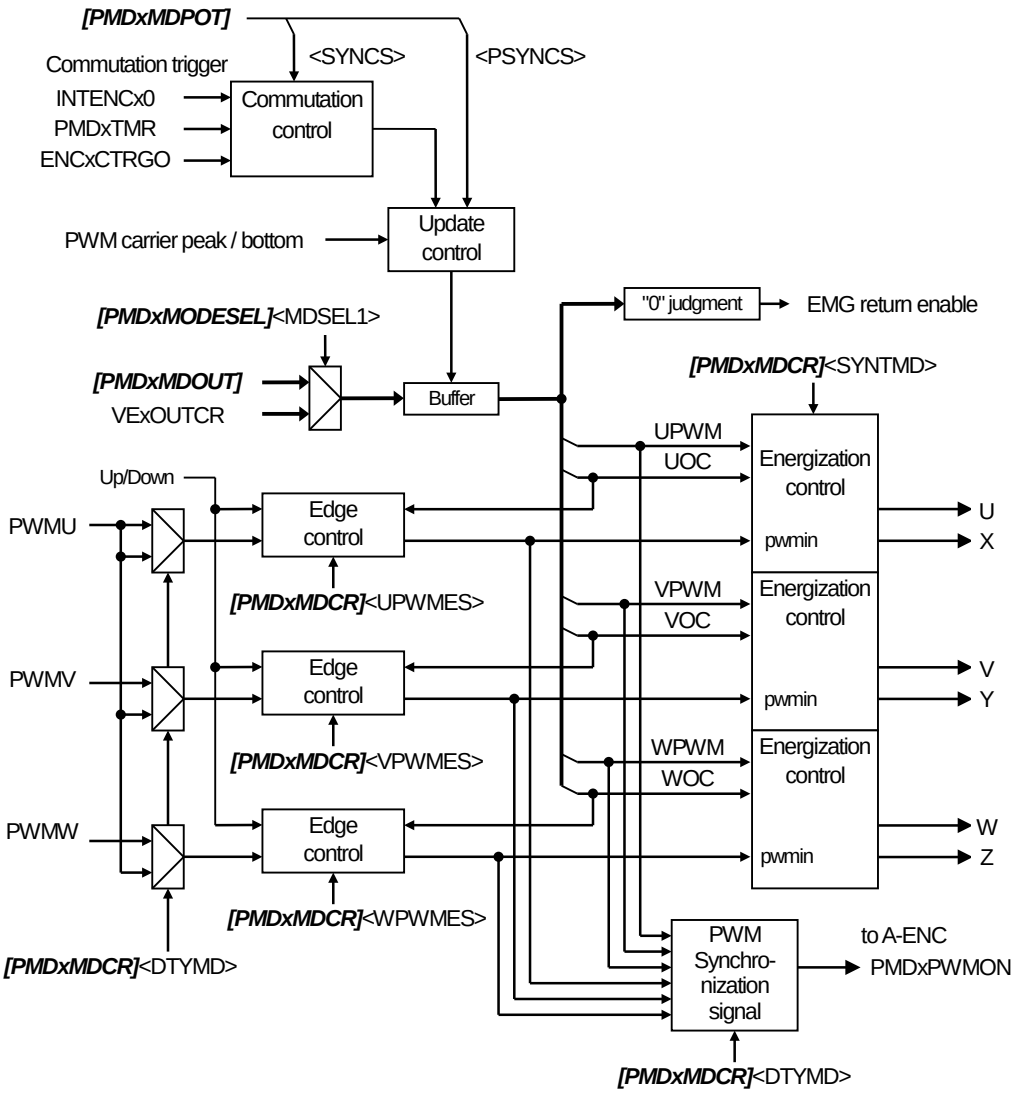


Figure 3.4 Conduction Control Circuit

The conduction control circuit performs the six phase outputs (U/X, V/Y, W/Z) control according to the settings made in the output control register ***[PMDxMDOUT]*** / VExOUTCR and the output setting register ***[PMDxMDPOT]***. ***[PMDxMDOUT]*** / VExOUTCR register is double-buffered and update timing can be select as synchronous or asynchronous to PWM. Update timing synchronizing with trigger input from another peripheral function can also be selected. (For details of update timing, refer to "Table 3.1 ***[PMDxMDOUT]*** / VExOUTCR buffer Update Timing".)

<UPWM>, <VPWM>, <WPWM> of the ***[PMDxMDOUT]*** register selects PWM or High/Low output for each of the U/X, V/Y and W/Z phases. When PWM output is selected, PWM waveforms are output. When High/Low output is selected, output is fixed to either a High level or Low level. Each output is set to "High" or "Low" by <UOC>, <VOC>, <WOC> of the register ***[PMDxMDOUT]*** / VExOUTCR.

Refer to "Table 3.2 Decode circuit outputs according to ***[PMDxMDOUT]*** / VExOUTCR and [PMDxMDCR]<SYNTMD> setting" for six phase outputs control with the output control setting (***[PMDxMDOUT]*** / VExOUTCR and ***[PMDxMDPOT]***), and the port output setting (***[PMDxMDCR]***<SYNTMD>).

In addition, using ***[PMDxMDPOT]***<POLH>,<POLL>, six output ports can be set to low-active or high-active on upper-phase outputs (UOx,VOx,WOx) or lower-phase outputs (XOx,YOx,ZOx) respectively.

The conduction control circuit outputs a PWM signal (PWMON) to the encoder input circuit (A-ENC). The external input signal in the A-ENC is sampled synchronously with the PWMON.

Table 3.1 *[PMDxMDOUT]* / VExOUTCR buffer Update Timing

		***[PMDxMDPOT]*<PSYNCS> setting**			
		00	**01**	**10**	**11**
***[PMDxMDPOT]* <SYNCS> setting**	**00**	Constant update	PWM carrier bottom	PWM carrier peak	PWM carrier peak and PWM carrier bottom
	01	When INTENCx0 (Note2) is arisen	The first PWM carrier bottom every time when INTENCx0 (Note2) is arisen.	The first PWM carrier peak every time when INTENCx0 (Note2) is arisen.	Either the first PWM carrier peak or the first carrier bottom every time when INTENCx0(Note2) is arisen.
	10	When PMDxTMR (Note2) is arisen.	The first PWM carrier bottom every time when PMDxTMR (Note2) is arisen.	The first PWM carrier peak every time when PMDxTMR (Note2) is arisen.	Either the first PWM carrier peak or the first carrier bottom every time when PMDxTMR(Note2) is arisen.
	11	When ENCxCTRGO (Note2) (MCMP compare established) is arisen.	The first PWM carrier bottom every time when ENCxCTRGO (Note2) is arisen.	The first PWM carrier peak every time when ENCxCTRGO (Note2) is arisen.	Either the first PWM carrier peak or the first carrier bottom every time when ENCxCTRGO (Note2) is arisen.

Note1: If PMD is disabled (***[PMDxMDEN]***<PWMEN>=0), the retained trigger condition is cleared.

Note2: The connection destination depend on the product. For details, refer to "Product Information" of the reference manual.

Table 3.2 Decode circuit outputs according to *[PMDxMDOUT]* / VExOUTCR and *[PMDxMDCR]*<SYNTMD> setting

[PMDxMDCR]<SYNTMD>=0

		PWM output setting *[PMDxMDOUT]*<nPWM>			
		0: H/L output		1: PWM output	
		Upper-phase	Lower-phase	Upper-phase	Lower-phase
Conduction setting *[PMDxMDOUT]* <nOC>	00	Low	Low	PWM_N	PWM
	01	Low	High	Low	PWM
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

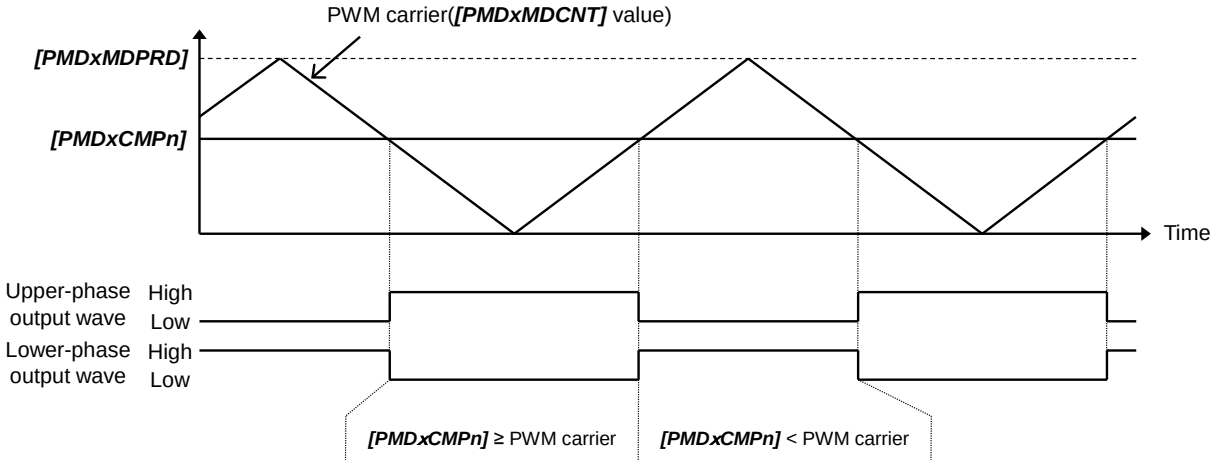
[PMDxMDCR]<SYNTMD>=1

		PWM output setting *[PMDxMDOUT]*<nPWM>			
		0: H/L output		1: PWM output	
		Upper-phase	Lower-phase	Upper-phase	Lower-phase
Conduction setting *[PMDxMDOUT]* <nOC>	00	Low	Low	PWM_N	PWM
	01	Low	High	Low	PWM_N
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

Note: n = U,V,W

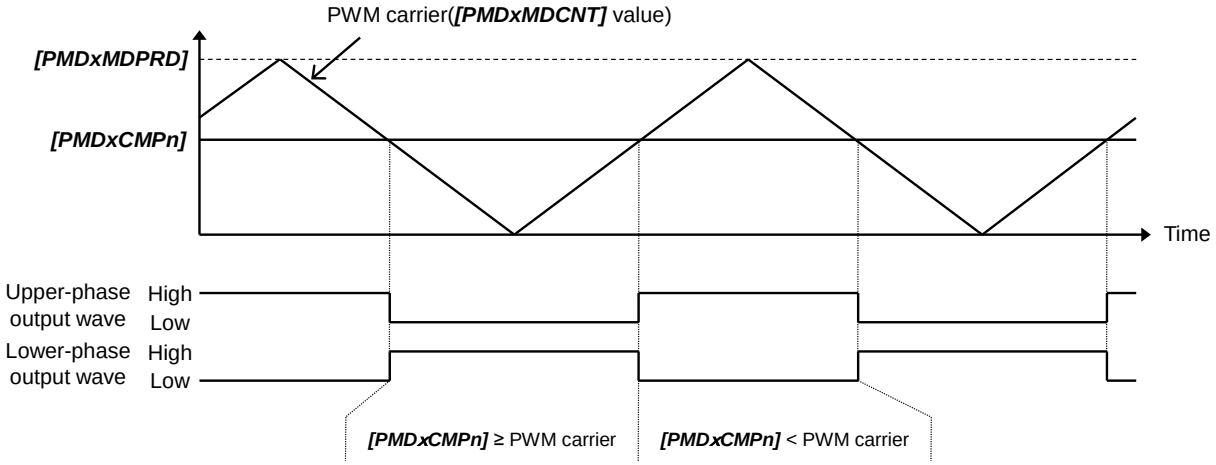
- Center-ON PWM

[PMDxMDCR]<PWMMD>=1
[PMDxMDOUT]<nPWM>=1
[PMDxMDOUT]<nOC>=11



- Center-OFF PWM

[PMDxMDCR]<PWMMD>=1
[PMDxMDOUT]<nPWM>=1
[PMDxMDOUT]<nOC>=00



3.4. Protection Control Circuit

The protection control circuit consists of a protection control unit and a protect output control unit.
The protection control unit consists of the EMG protection control circuit and the OVV protection control circuit.

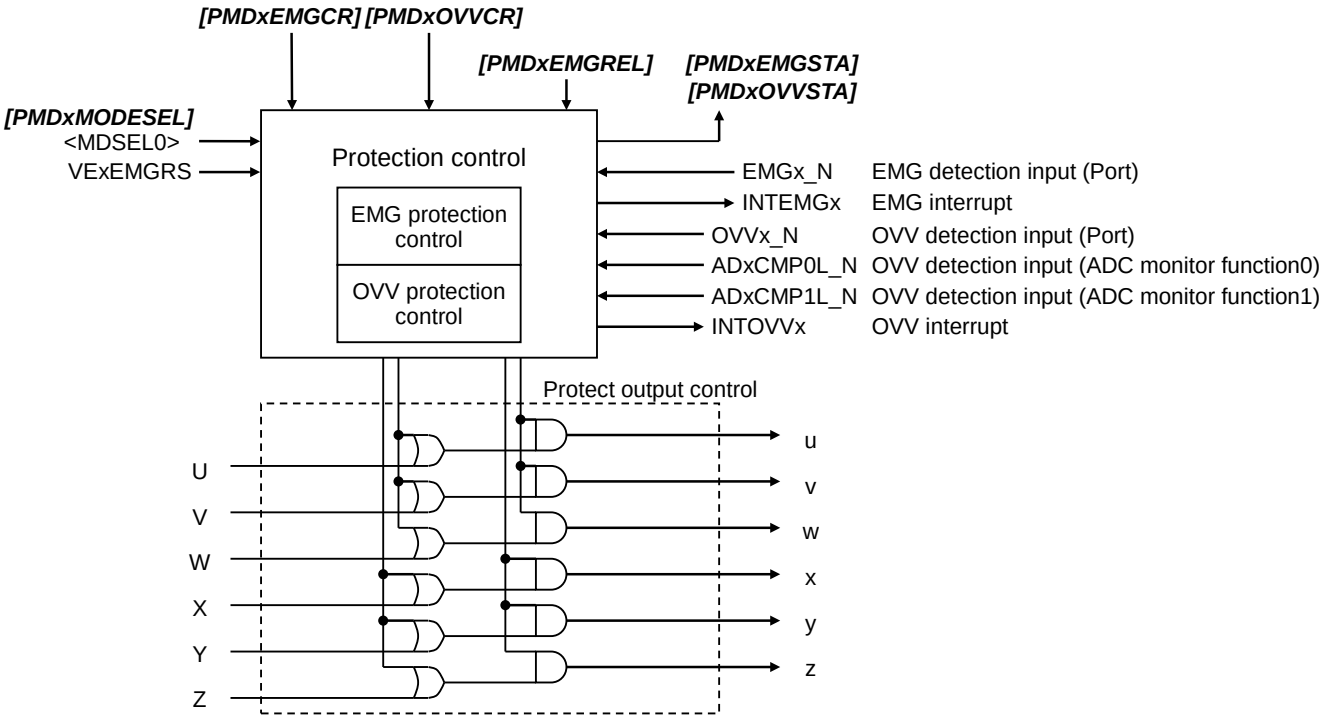


Figure 3.5 Protection Control Circuit

3.4.1. EMG Protection Circuit

The EMG protection circuit is an emergency stop protection circuit and operates when the EMGx_N input goes "Low ". EMG protection is set through the EMG Control Register (***[PMDxEMGCR]***).

Note: After reset, the EMG protection circuit is enabled.

- EMG input

  The noise filter is inserted in the EMGx_N input. The noise detection time is selected with the EMG input detection time setting (***[PMDxEMGCR]***<EMGCNT>).

- EMG protection operation

  The EMG protection circuit offers an emergency stop mechanism: when the EMGx_N input is asserted (H→L), all six port outputs are immediately disabled (depending on the ***[PMDxEMGCR]***<EMGMD> setting) and an EMG interrupt (INTEMGx) is generated. ***[PMDxEMGCR]*** <EMGMD> can be set to output a control signal that sets external output ports to High-impedance in case of an emergency.
  A read value of "1" in ***[PMDxEMGSTA]***<EMGST> indicates that the EMG protection circuit is active.

- Return from the EMG protection

  In the EMG protection state, it can be released by setting all the port output lines inactive (Set "0" to <UPWM>,<VPWM>,<WPWM>,<UOC>,<VOC>,<WOC> of ***[PMDxMDOUT]*** / VExOUTCR.) (Note1) and then setting either <EMGRS> of ***[PMDxEMGCR]*** / VExEMGRS to "1". While the EMGx_N input is "Low", any attempt to return from the EMG protection state is ignored. The EMG protection state can return after that confirming the status flag of ***[PMDxEMGSTA]***<EMGI> is "1".

  Note1: The data of ***[PMDxMDOUT]*** / VExOUTCR is necessary to be reflected in the subsequent stage buffer.

  Note2: EMG return procedure after the reset deassertion.

  After reset, the EMG function is enabled but EMGx_N pin is configured as a normal port. Therefore, as the EMG protection might be valid, release the EMG protection by the following procedure at the initial sequence.

  (1) Selects EMG function by the Port function register(***[PxFRn]***).
  (2) Reads ***[PMDxEMGSTA]***<EMGI> to confirm it as "1".
  (3) Sets <UPWM>,<VPWM>,<WPWM>,<UOC>,<VOC>,<WOC> of ***[PMDxMDOUT]*** / VExOUTCR to "0" to make all ports in-active.
  (4) Return EMG protection by setting <EMGRS> of ***[PMDxEMGCR]*** / VExEMGRS to "1".

- Disable of the EMG protection function

  To disable the EMG protection function, write "0x5A" and "0xA5" in this order to the EMG release register ***[PMDxEMGREL]*** and then clear ***[PMDxEMGCR]***<EMGEN> to "0". These 3 instructions must be executed consecutively to prevent the EMG protection function from being inadvertently disabled.

3.4.2. OVV Protection Circuit

The OVV protection circuit is activated when the OVV input becomes "Low". This protection control is set by OVV control register (***[PMDxOVVCR]***).

- OVV input

  The OVV input can be selected from the OVVx_N pin and the OVV status signal (ADxCMP0L_N, ADxCMP1L_N) of the AD monitor function by ***[PMDxOVVCR]*** <OVVISEL>, <ADIN0EN>, and <ADIN1EN>.

  The noise filter is inserted in the OVV input. The noise detection time is selected with the OVV input detection time setting (***[PMDxOVVCR]***<OVVCNT>).

- OVV protection operation

  OVV protection circuit fixes 6 port outputs in the port output disable unit to High level or Low level, when OVV signal input is active continuously for a predetermined interval time (set by <OVVCNT>). And OVV interrupt (INTOVVx) is generated. ***[PMDxOVVCR]***<OVVMD> setting selects from among Lower-phases OFF/Upper-phases ON, Upper-phases OFF/Lower-phases ON, and all phases OFF.

  A read value of "1" in ***[PMDxOVVSTA]***<OVVST> indicates that the OVV protection circuit is active.

- Return from the OVV protection

  The return from the OVV protection state is enabled by setting ***[PMDxOVVCR]***<OVVRS> to "1". And after the OVV input becomes inactive, the OVV protection is automatically returned at a predetermined timing. (While the OVV protection input is "Low", any attempt to return from the OVV protection state is ignored. The state of the port can be checked by reading ***[PMDxOVVSTA]***<OVVI>)

  The OVV protection state is returned in synchronization with the PWM period (at the timing when PWM count (***[PMDxMDCNT]***) matches ***[PMDxMDPRD]***. However if an interrupt on a half period of PWM is set, the protection state is returned when PWM count is "0x0001" or matches ***[PMDxMDPRD]***.).

- Disable of the OVV protection function

  In order to disable OVV function, EMG release register ***[PMDxEMGREL]*** should be set to "0x5A" and next, "0xA5". Then ***[PMDxOVVCR]***<OVVEN> should be set to "0". These 3 instructions should be executed continuously to prevent the OVV protection function from being inadvertently disabled.

3.4.3. Protection control when using the debug tool

When using the debug tool, PMD output ports can be disabled when PMD is stopped by the debug halt.

In the debug halt, whether the port output becomes High-impedance or PMD output is selected by ***[PMDxPORTMD]***<PORTMD> setting.

3.5. Dead time Control Circuit

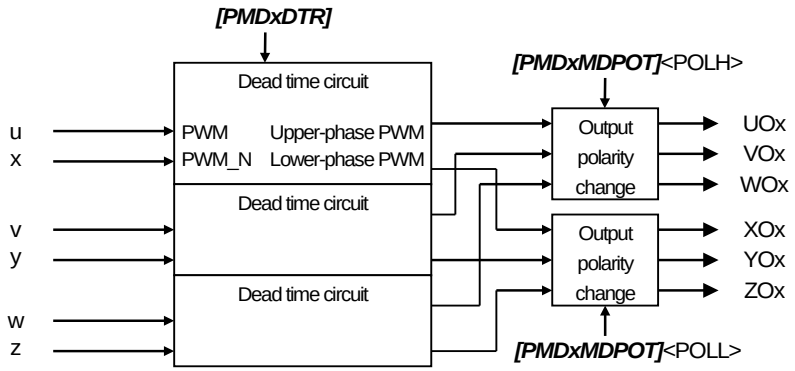


Figure 3.6 Dead time Control Circuit

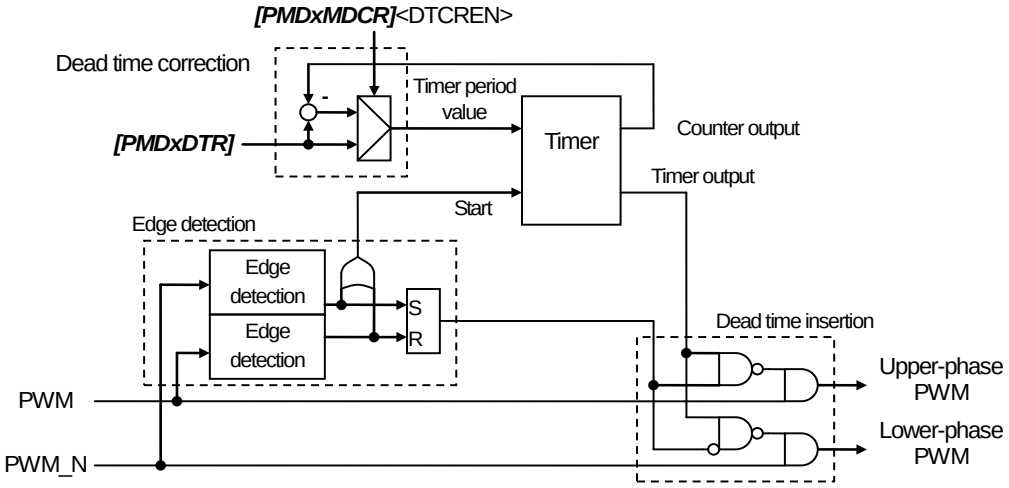


Figure 3.7 Dead Time Circuit

The dead time control circuit consists of a dead time unit and an output polarity switching unit. The dead time unit consists of the edge detection block, timer block, dead time insert block, and dead time correction block. (Refer to "Figure 3.7 Dead Time Circuit")

For each of the U-, V-, and W-phases, the dead -time units delay the ON-timing of each phase when the upper-phase and lower-phase are switched to prevent a short circuit. The dead time is set to the Dead Time Register (***[PMDxDTR]*** <DTR[7:0]>) as an 8-bit value with a resolution of 8/fsys can be set.

The output polarity switching circuit allows the polarity (active high or active low) of the upper-output (UOx, VOx, WOx) and lower-output (XOx,YOx, ZOx) phases to be independently set through PMD output setting register ***[PMDxMDPOT]***<POLH> and <POLL>.

In the dead time correction block, when one of the on-period of the upper PWM or the lower PWM is 0 width, if ***[PMDxMDCR]***<DTCREN> is set to "1", the other PWM delay time is corrected to be shortened. If the PWM signal is OFF during the dead time period, the delay time of the counter phase is shortened in the rest of dead time (dead time register setting time - ON time). When the upper PWM becomes OFF during the dead time period, the delay time of the lower PWM should be corrected to be shortened. When the lower PWM becomes OFF during the dead time period, the delay time of the upper PWM should be corrected to be shortened. Figure 3.8 shows dead time correction. A delay time is corrected in the vicinity of duty of 100% of the upper PWM and it also is corrected in the vicinity of duty of 0%.

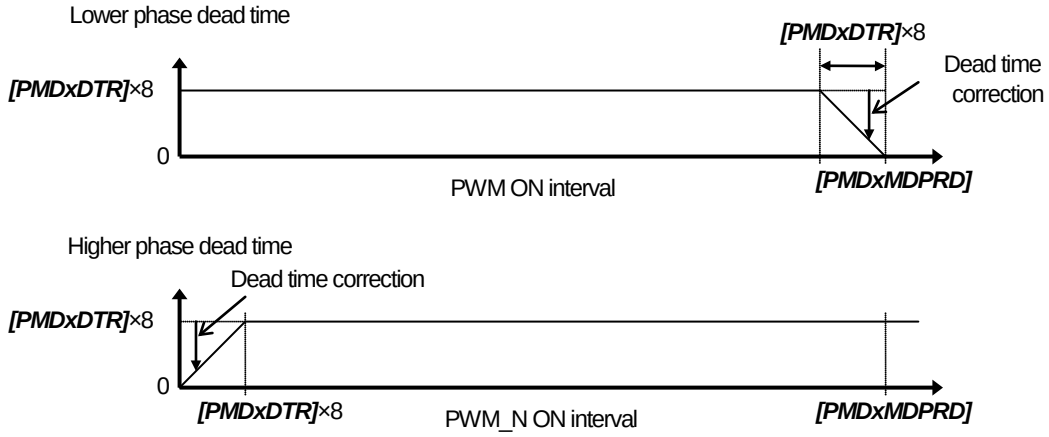


Figure 3.8 Dead Time Correction

3.6. Synchronous Trigger Generation Circuit

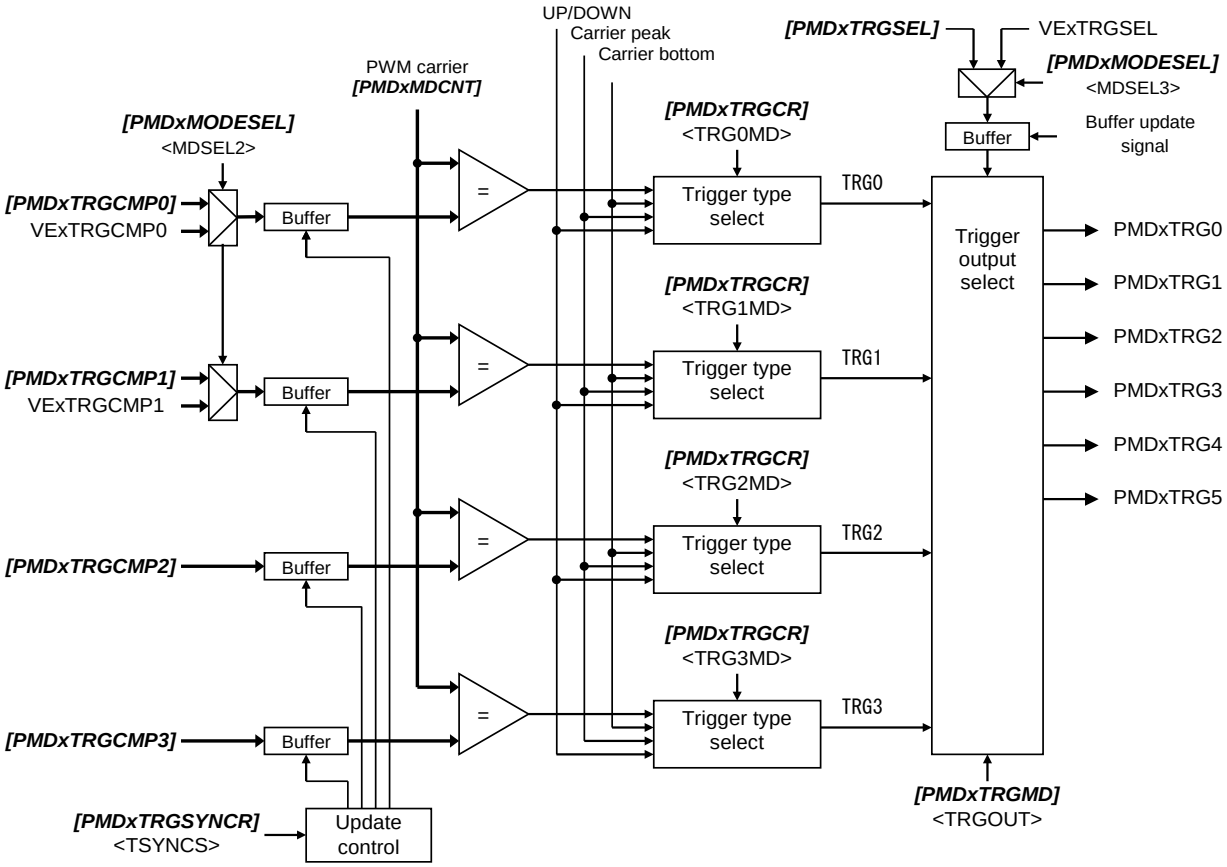


Figure 3.9 Synchronous Trigger Generation Circuit

The synchronous trigger generation circuit generates four trigger signals (TRG0 to TRG3) for starting ADC sampling in synchronization with PWM. When VE mode is selected in ***[PMDxMODESEL]***<MDSEL2>, ***[PMDxTRGCMP0]*** and ***[PMDxTRGCMP1]*** are switched to VExTRGCMP0 and VExTRGCMP1 in the VE register output.

The trigger timing can be selected following 6 types.

(1) At up count operation compare-match (Note1)(Note2)
(2) At down count operation compare-match (Note1)(Note3)
(3) At up/down count operation compare-match (Note1)(Note3)(Note4)
(4) PWM carrier peak
(5) PWM carrier bottom(Note3)
(6) PWM carrier peak and PWM carrier bottom(Note3)

Note1: The compare-match is between PWM counter (***[PMDxMDCNT]***) and (***[PMDxTRGCMPn]***(n=0 to 3))
Note2: If PWM is started while ***[PMDxTRGCMPn]***(n=0 to 3) is set to "0x0001" with saw-tooth wave carrier(<PWMMD>=0), there is no trigger output in the first PWM cycle.
Note3: When saw-tooth wave carrier(<PWMMD>=0) is selected, it cannot be selected.
Note4: When trigger output at up/down-count match, ***[PMDxTRGCMPn](n=0 to 3)***=0x0001 and triangular wave (<PWMMD>=1),one trigger output is made per period.

During in trigger select output mode: ***[PMDxTRGMD]***<TRGOUT>=1. The TRG0 signal is output from ADC synchronous trigger (***[PMDxTRG0]*** to ***[PMDxTRG5]***) selected by the trigger output select register ***[PMDxTRGSEL]*** / VExTRGSEL. The TRG0 setting is set by ***[PMDxTRGCMP0]*** / VExTRGCMP0 and ***[PMDxTRGCR]***<TRG0MD>. (Refer to "Table 4.4 Trigger Output Patterns".)

When ***[PMDxTRGMD]***<EMGTGE>=1, this circuit outputs trigger signals in EMG protection state.

An example of using the synchronization trigger generation circuit is shown below.

- In the case of 3-shunt

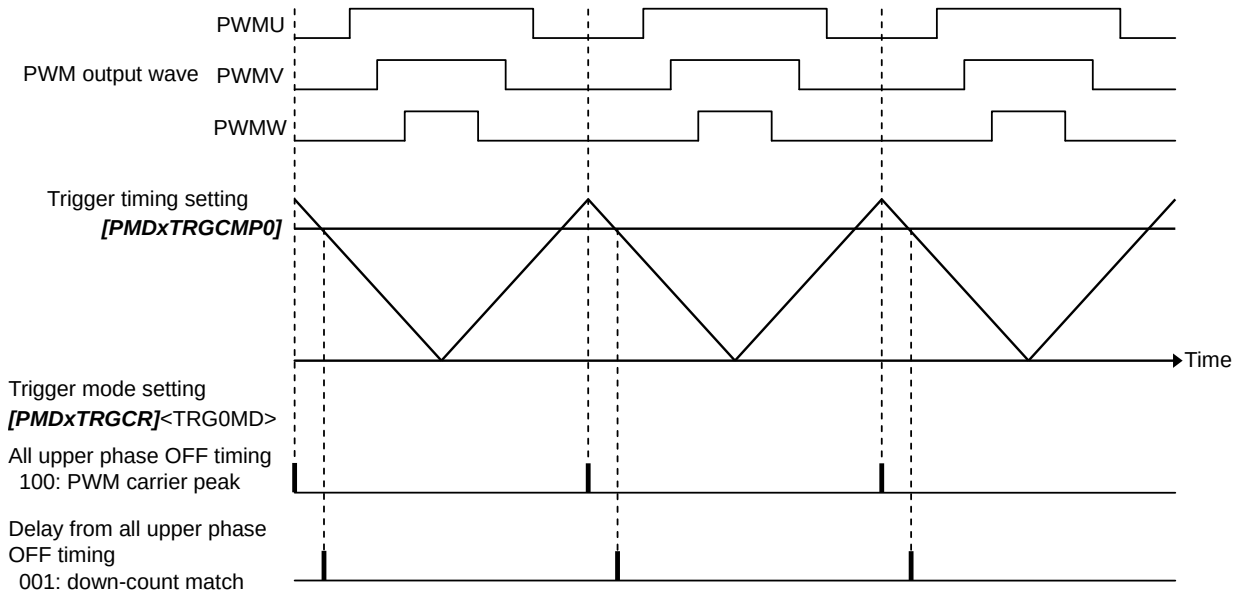


Figure 3.10 Example of using the PMD trigger at 3-shunt

Trigger output mode setting (***[PMDxTRGMD]***<TRGOUT>) is set to "1"(Trigger selection output).

Trigger mode setting 0 (***[PMDxTRGCR]***<TRG0MD>) is set to "100"(Trigger output at PWM carrier peak), when trigger is generated at the timing of all upper-phases OFF. Trigger mode setting 1 (***[PMDxTRGCR]***<TRG1MD>) is set to "001"(Trigger output at down-count match) and ***[PMDxTRGCMP0]*** is set to delay timing, when delayed trigger is generated at the timing of all upper-phases OFF.

By setting trigger output select (***[PMDxTRGSEL]***<TRGSEL>) according to the position (sector) of the motor, it is possible to generate six kinds of triggers for each sector.

- In the case of 1-shunt

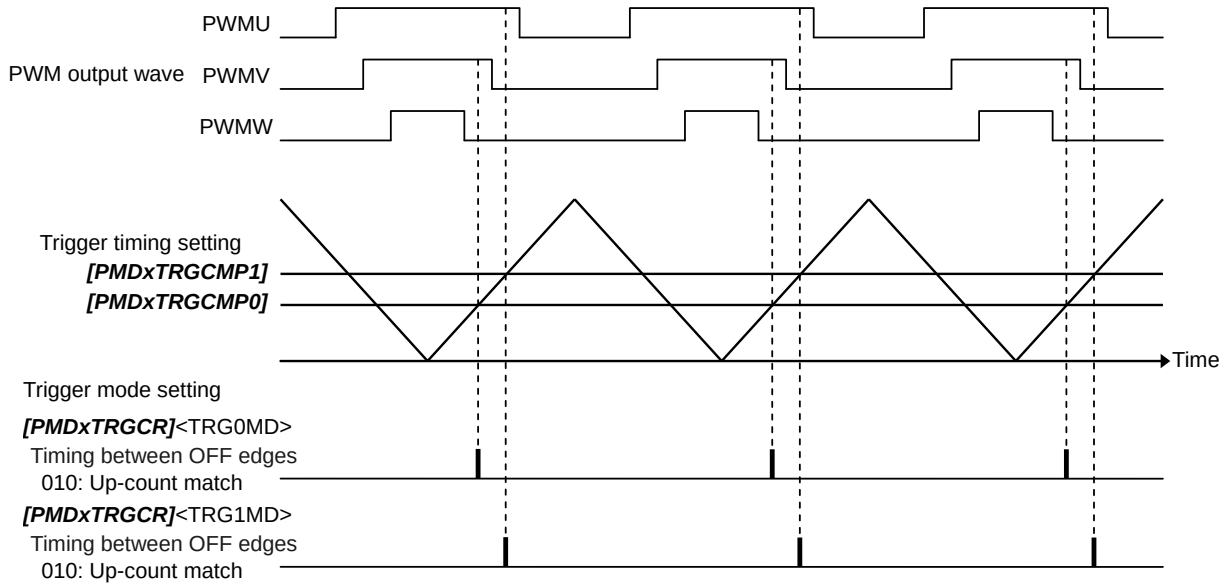


Figure 3.11 Example of using the PMD trigger at 1-shunt

Trigger output mode setting (***[PMDxTRGMD]***<TRGOUT>) is set to "0"(Fixed trigger output).

Trigger mode setting 0 and 1(***[PMDxTRGCR]***<TRG0MD>,<TRG1MD>) is set to "010"(Trigger output at up-count match), when trigger is generated at the timing between OFF edges. Or trigger mode setting 0 and 1(<TRG0MD>, <TRG1MD>) is set to "001"(Trigger output at down-count match), when trigger is generated at the timing between ON edges.

The previous trigger is set to ***[PMDxTRGCMP0]***, and the subsequent trigger is set to ***[PMDxTRGCMP1]***.

4. Registers

4.1. List of Registers

The following table lists the control registers and their addresses:

Peripheral Function Name		Channel/Unit	Base Address		
			TYPE1	TYPE2	TYPE3
Programmable Motor Control Circuit Plus	PMD+	ch0	0x400F6000	0x400E9000	0x40089000
		ch1	0x400F6100	0x400E9400	0x40089400
		ch2	0x400F6200	0x400E9800	0x40089800
		ch3	—	0x400E9C00	0x40089C00

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register Name		Address(Base+)
PMD Enable Register	***[PMDxMDEN]***	0x0000
Port Output Mode Register	***[PMDxPORTMD]***	0x0004
PMD Control Register	***[PMDxMDCR]***	0x0008
PWM Counter Status Register	***[PMDxCNTSTA]***	0x000C
PWM Counter Register	***[PMDxMDCNT]***	0x0010
PWM Period Register	***[PMDxMDPRD]***	0x0014
PMD Compare U Register	***[PMDxCMPU]***	0x0018
PMD Compare V Register	***[PMDxCMPV]***	0x001C
PMD Compare W Register	***[PMDxCMPW]***	0x0020
Mode Selection Register	***[PMDxMODESEL]***	0x0024
PMD Conduction Control Register	***[PMDxMDOUT]***	0x0028
PMD Output Setting Register	***[PMDxMDPOT]***	0x002C
EMG Release Register	***[PMDxEMGREL]***	0x0030
EMG Control Register	***[PMDxEMGCR]***	0x0034
EMG Status Register	***[PMDxEMGSTA]***	0x0038
OVV Control Register	***[PMDxOVVCR]***	0x003C
OVV Status Register	***[PMDxOVVSTA]***	0x0040
Dead time Register	***[PMDxDTR]***	0x0044
Trigger Compare 0 Register	***[PMDxTRGCMP0]***	0x0048
Trigger Compare 1 Register	***[PMDxTRGCMP1]***	0x004C
Trigger Compare 2 Register	***[PMDxTRGCMP2]***	0x0050
Trigger Compare 3 Register	***[PMDxTRGCMP3]***	0x0054
Trigger Control Register	***[PMDxTRGCR]***	0x0058
Trigger Output Mode Setting Register	***[PMDxTRGMD]***	0x005C
Trigger Output Select Register	***[PMDxTRGSEL]***	0x0060
Trigger Update Timing Setting Register	***[PMDxTRGSYNCR]***	0x0064

4.2. Details of Registers

4.2.1. *[PMDxMDEN]* (PMD Enable Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	—	0	R	Read as "0".
0	PWMEN	0	R/W	Enables or disables waveform synthesis.(Note1), (Note2) 0: Disable 1: Enable

Note1: When the port is set to a function output (PMD output), the port disables output (High-impedance) by setting <PWMEN>=0. For details of a port setting, refer to "Input/Output Ports" of the reference manual.

Note2: <PWMEN>=1 should be set after initial settings other than <PWMEN> like an output polarity are set.

4.2.2. *[PMDxPORTMD]* (Port Output Mode Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	—	0	R	Read as "0".
1:0	PORTMD[1:0]	00	R/W	Port control setting when a debug halt occurs (Note1)(Note2)(Note3) 00: Upper-phases High-impedance / lower-phases High-impedance 01: Upper-phases High-impedance / lower-phases PMD output 10: Upper-phases PMD output / lower-phases High-impedance 11: Upper-phases PMD output / lower-phases PMD output Sets the port output for both upper-phases (UOx/VOx/WOx) and the lower-phases (XOx/YOx/ZOx) when a debug halt occurs in the use of ports for function output (PMD output). When a debug halt occurs while High-impedance is selected, the ports are disabled to output (High-impedance). In other cases, external port outputs depend on PMD outputs.

Note1: When ***[PMDxMDEN]***<PWMEN>=0, output ports are disabled to output (High-impedance) regardless of the <PORTMD[1:0]> setting.

Note2: Depending on the setting of ***[PMDxEMGCR]***<EMGMD[1: 0]>, port output control is also performed during EMG protection.

Note3: For details of a port setting, refer to "Input/Output Ports" of the reference manual.

4.2.3. *[PMDxMODESEL]* (Mode Selection Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	—	0	R	Read as "0".
7	DCMPEN	0	R/W	Enables auto switching between VE register and PMD register (Note1) 0: Two register switching disable (only uses <MDSEL0> setting register) 1: Two register switching enabled (switches between the first half and last half of PWM period) This bit is enabled in case of <MDSEL0>=1. This bit is enabled when a triangular wave carrier is selected (***[PMDxMDCR]***<PWMMD>=1).
6:4	—	0	R	Read as "0".
3	MDSEL3	0	R/W	Mode selection 3 0: Bus mode (uses PMD register: ***[PMDxTRGSEL]***) 1: VE mode (uses VE register: ***[VExTRGSEL]***) ***[PMDxTRGSEL]*** / VExTRGSEL register selection
2	MDSEL2	0	R/W	Mode selection 2 0: Bus mode (uses PMD register: ***[PMDxTRGCMP0]*** and ***[PMDxTRGCMP1]***) 1: VE mode (uses VE registers: ***[VExTRGCMP0]*** and ***[VExTRGCMP1]***) ***[PMDxTRGCMP0]*** / VExTRGCMP0 and ***[PMDxTRGCMP1]*** / VExTRGCMP1 registers selection
1	MDSEL1	0	R/W	Mode selection 1 0: Bus mode (uses PMD register: ***[PMDxMDOUT]***) 1:VE mode (uses VE register: ***[VExOUTCR]***) ***[PMDxMDOUT]*** / VExOUTCR register selection
0	MDSEL0	0	R/W	Mode selection 0 0: Bus mode (uses PMD registers: ***[PMDxCMPU]***/***[PMDxCMPV]*** and ***[PMDxCMPW]***) 1: VE mode (uses VE registers: ***[VExCMPU]*** / ***[VExCMPV]*** / ***[VExCMPW]*** registers selection and ***[VExEMGRS]*** register enable setting)

Note1: When auto switching to VE register is enabled, set "1" to ***[VExEN]*** and ***[VExREPTIME]***, to use VE register (***[VExCMPU]***, ***[VExCMPV]***, and ***[VExCMPW]***).

Note2: For details of VE, refer to the reference manual, "Advanced Vector Engine".

4.2.4. *[PMDxMDCR]* (PMD Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:14	WPWMES[1:0]	00	R/W	W-phase edge setting (Note1) 00: Edge unfixed (center-aligned PWM) 01: Reserved 10: PWM rising-edge fixed (to the PWM carrier bottom) 11: PWM falling-edge fixed (to the PWM carrier bottom)
13:12	VPWMES[1:0]	00	R/W	V-phase edge setting (Note1) 00: Edge unfixed (center-aligned PWM) 01: Reserved 10: PWM rising-edge fixed (to the PWM carrier bottom) 11: PWM falling-edge fixed (to the PWM carrier bottom)
11:10	UPWMES[1:0]	00	R/W	U-phase edge setting (Note1) 00: Edge unfixed (center-aligned PWM) 01: Reserved 10: PWM rising-edge fixed (to the PWM carrier bottom) 11: PWM falling-edge fixed (to the PWM carrier bottom)
9:8	DSYNCS[1:0]	00	R/W	Double-buffer update timing for the PWM compare register and PWM period register. (Note2)(Note3) 00: Depends on interrupt period setting (refer to the Table 4.1) Updates at the carrier peak and carrier bottom when 0.5 PWM period is selected (<INTPRD>=00). Otherwise, updates at the carrier peak. 01: Updates at PWM carrier bottom 10: Updates at PWM carrier peak 11: Updates at both PWM carrier peak and bottom
7	DTCREN	0	R/W	Set a dead time correction. 0: Disable 1: Enable
6	PWMCK	0	R/W	PWM period extension mode 0: Normal period 1: 4 × period Sets the counting period of the PWM counter. Normal period setting: Saw-tooth wave 1/fsys / Triangular wave 2/fsys 4 × period setting: Saw-tooth wave 4/fsys / Triangular wave 8/fsys
5	SYNTMD	0	R/W	Port output mode setting Port outputs are controlled by a combination of ***[PMDxMDOUT]*** <nOC>,<nPWM>, ***[PMDxMDPOT]***<POLH>, <POLL> and <SYNTMD> (refer to Table 4.2).
4	DTYMD	0	R/W	Duty mode selection 0: 3-phase common mode 1: 3-phase independent mode Select whether to set the duty setting independently for each phase of ***[PMDxCMPU/V/W]***, or to use the ***[PMDxCMPU]*** register as common 3 phases.
3	PINT	0	R/W	PWM interrupt request timing selection (Note4)(Note5) 0: Interrupt request occurs at PWM carrier bottom (***[PMDxMDCNT]*** =0x0001). 1: Interrupt request occurs at PWM carrier peak (***[PMDxMDCNT]*** = ***[PMDxMDPRD]***).

Bit	Bit Symbol	After reset	Type	Function
2:1	INTPRD[1:0]	00	R/W	PWM interrupt request period selection 00: Interrupt request at every 0.5 PWM period (Note6)(Note7) 01: Interrupt request at every PWM period 10: Interrupt request at every two PWM periods 11: Interrupt request at every four PWM periods This field selects the PWM interrupt request period from 0.5 PWM period, one PWM period, two PWM periods and four PWM periods.
0	PWMMD	0	R/W	PWM carrier waveform selection 0: PWM mode 0 (edge-aligned PWM and saw-tooth wave) 1: PWM mode 1(center-aligned PWM and triangular wave)

Note1: Valid when triangular carrier PWM is selected (<PWMMD>=1).

Note2: Updates at carrier peak when saw-tooth wave carrier is selected (<PWMMD>=0) regardless of the setting.

Note3: When ***[PMDxMDEN]***<PWMEN>=0, updates asynchronously regardless of setting.

Note4: Interrupt request occurs at carrier peak when the PWM carrier is saw-tooth wave (<PWMMD>=0).

Note5: Interrupt request occurs both at carrier peak and carrier bottom when the interrupt period is 0.5 period (<INTPRD>=00).

Note6: PWM interrupt request period can be configured only when the PWM carrier is triangular wave (<PWMMD>=1)

Note7: The subsequent stage of the double-buffer of the compare registers (***[PMDxCMPU/V/W]***) and the period register (***[PMDxMDPRD]***) are updated by peak and bottom of the PWM carrier.

Table 4.1 *[PMDxMDPRD]*, *[PMDxCMPU/V/W]* buffer Update Timing

Settings		Update Timing
<DSYNCS>	<INTPRD>	
00	1x	Updates at PWM carrier peak
	x1	Updates at PWM carrier peak
	00	Updates at PWM carrier peak and PWM carrier bottom
01	xx	Updates at PWM carrier bottom
10	xx	Updates at PWM carrier peak
11	xx	Updates at PWM carrier peak and PWM carrier bottom

Note: x: Don't care

4.2.5. *[PMDxCNTSTA]* (PWM Counter Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	—	0	R	Read as "0".
0	UPDWN	0	R	PWM counter flag (Note) 0: Up-counting 1: Down-counting This bit indicates whether the PWM counter is up-counting or down-counting.

Note: The PWM carrier is a saw-tooth wave (***[PMDxMDCR]***<PWMMD>=0), a zero is always read.

4.2.6. *[PMDxMDCNT]* (PWM Counter Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	MDCNT[15:0]	0x0000	R	PWM counter(Note) A value can be read from the up-down counter generating a PWM carrier wave. Counter resolution: 1/fsys When a 4 × period mode is selected (***[PMDxMDCR]***<PWMCK>=1), time resolution of the counter is 4/fsys.

Note: Depending on the setting of the PWM carrier (***[PMDxMDCR]***<PWMMD>), the PWM counter values when PMD is disabled (***[PMDxMDEN]***<PWMEN>=0) are as follows:
In case of ***[PMDxMDCR]***<PWMMD>=0: 0x0001
In case of ***[PMDxMDCR]***<PWMMD>=1: the value of ***[PMDxMDPRD]***

4.2.7. *[PMDxMDPRD]* (PWM Period Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	MDPRD[15:0]	0x0000	R/W	PWM period ***[PMDxMDPRD]*** ≥ 0x0010 (Note1) By the combination of the PWM period extension mode (***[PMDxMDCR]***<PWMCK>) and the PWM carrier waveform ***[PMDxMDCR]***<PWMMD>, the PWM period can be calculated as follows: When <PWMCK>=0, <PWMMD>=0: ***[PMDxMDPRD]*** × 1/fsys <PWMMD>=1: ***[PMDxMDPRD]*** × 2/fsys When <PWMCK>=1, <PWMMD>=0: ***[PMDxMDPRD]*** × 4/fsys <PWMMD>=1: ***[PMDxMDPRD]*** × 8/fsys

Note1: If ***[PMDxMDPRD]*** is set to a value less than "0x0010", it is automatically assumed to be "0x0010". (The register retains the actual value that is written.)

Note2: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note3: Since the ***[PMDxMDPRD]*** register is double-buffered, the PWM period can be changed during the operation of the PWM counter.

Note4: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.1 ***[PMDxMDPRD]***, ***[PMDxCMPU/V/W]*** buffer Update Timing".

Note5: Read value is the first buffer value (the latest data set via a bus).

4.2.8. *[PMDxCMPU]* (PWM Compare U Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	CMPU[15:0]	0x0000	R/W	PWM pulse width of U Phase (Note1) 0x0000 through 0xFFFF <CMPU> are compare registers for determining the output pulse width of the U-phase. These registers are double-buffered. Pulse width is determined by comparing the subsequent stage buffer and the PWM counter to evaluate which is small or large. By the combination of the PWM period extension mode (***[PMDxMDCR]***<PWMCK>) and the PWM carrier waveform (***[PMDxMDCR]***<PWMMD>), the pulse width can be calculated as follows: When <PWMCK>=0, <PWMMD>=0: ***[PMDxCMPU]*** × 1/fsys <PWMMD>=1: ***[PMDxCMPU]*** × 2/fsys When <PWMCK>=1, <PWMMD>=0: ***[PMDxCMPU]*** × 4/fsys <PWMMD>=1: ***[PMDxCMPU]*** × 8/fsys

Note1: When ***[PMDxCMPU]*** > ***[PMDxMDPRD]***, the duty is 100%.

Note2: When the compare register updated by the bus is loaded to the subsequent stage buffer, set the bus mode (default) by writing "0" to ***[PMDxMODESEL]***<MDSEL0>.

Note3: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note4: Since the ***[PMDxCMPU]*** register is double-buffered, the PWM pulse width can be changed during the operation of the PWM counter.

Note5: For detailed update timing of the subsequent stage buffer,
refer to the "Table 4.1 ***[PMDxMDPRD]***, ***[PMDxCMPU/V/W]*** buffer Update Timing".

Note6: Read value is the first buffer value (the latest data set via a bus).

4.2.9. *[PMDxCMPV]* (PWM Compare V Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	CMPV[15:0]	0x0000	R/W	PWM pulse width of V Phase (Note1) 0x0000 through 0xFFFF <CMPV> are compare registers for determining the output pulse width of the V-phase. These registers are double-buffered. Pulse width is determined by comparing the subsequent stage buffer and the PWM counter to evaluate which is small or large. By the combination of the PWM period extension mode (***[PMDxMDCR]***<PWMCK>) and the PWM carrier waveform (***[PMDxMDCR]***<PWMMD>), the pulse width can be calculated as follows: When <PWMCK>=0, <PWMMD>=0: ***[PMDxCMPV]*** × 1/fsys <PWMMD>=1: ***[PMDxCMPV]*** × 2/fsys When <PWMCK>=1, <PWMMD>=0: ***[PMDxCMPV]*** × 4/fsys <PWMMD>=1: ***[PMDxCMPV]*** × 8/fsys

Note1: When ***[PMDxCMPV]*** > ***[PMDxMDPRD]***, the duty is 100%.

Note2: When the compare register updated by the bus is loaded to the subsequent stage buffer, set the bus mode (default) by writing "0" to ***[PMDxMODESEL]***<MDSEL0>.

Note3: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note4: Since the ***[PMDxCMPV]*** register is double-buffered, the PWM pulse width can be changed during the operation of the PWM counter.

Note5: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.1 ***[PMDxMDPRD]***, ***[PMDxCMPU/V/W]*** buffer Update Timing".

Note6: Read value is the first buffer value (the latest data set via a bus).

4.2.10. *[PMDxCMPW]* (PWM Compare W Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	CMPW[15:0]	0x0000	R/W	PWM pulse width of W Phase (Note1) 0x0000 through 0xFFFF <CMPW> are compare registers for determining the output pulse width of the W-phase. These registers are double-buffered. Pulse width is determined by comparing the subsequent stage buffer and the PWM counter to evaluate which is small or large. By the combination of the PWM period extension mode (***[PMDxMDCR]***<PWMCK>) and the PWM carrier waveform (***[PMDxMDCR]***<PWMMD>), the pulse width can be calculated as follows: When <PWMCK>=0, <PWMMD>=0: ***[PMDxCMPW]*** × 1/fsys <PWMMD>=1: ***[PMDxCMPW]*** × 2/fsys When <PWMCK>=1, <PWMMD>=0: ***[PMDxCMPW]*** × 4/fsys <PWMMD>=1: ***[PMDxCMPW]*** × 8/fsys

Note1: When ***[PMDxCMPW]*** > ***[PMDxMDPRD]***, the duty is 100%.

Note2: When the compare register updated by the bus is loaded to the subsequent stage buffer, set the bus mode (default) by writing "0" to ***[PMDxMODESEL]*** <MDSEL0>.

Note3: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note4: Since the ***[PMDxCMPW]*** register is double-buffered, the PWM pulse width can be changed during the operation of the PWM counter.

Note5: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.1 ***[PMDxMDPRD]***, ***[PMDxCMPU/V/W]*** buffer Update Timing".

Note6: Read value is the first buffer value (the latest data set via a bus).

4.2.11. *[PMDxMDPOT]* (PMD Output Setting Register)

Bit	Bit Symbol	After reset	Type	Function
31:10	—	0	R	Read as "0".
9:8	SYNCS[1:0]	00	R/W	Selects ***[PMDxMDOUT]*** / VExOUTCR transfer timing (trigger synchronous setting). 00: asynchronous(Note4) 01: when INTENCx0 (A-ENCx interrupt request)(Note6) occurs 10: when PMDxTMR (Timer interrupt request)(Note6) occurs 11: when ENCxCTRGO (A-ENCx MCMP completed)(Note6) occurs Selects the subsequent stage buffer update timing of the conduction control register. (Note2)(Note3)
7:4	—	0	R	Read as "0".
3	POLH	0	R/W	Selects the output polarity of the upper-phase outputs (UOx, VOx, WOx). 0: Active low 1: Active high
2	POLL	0	R/W	Selects the output polarity of the lower-phase outputs (XOx, YOx, ZOx). 0: Active low 1: Active high
1:0	PSYNCS[1:0]	00	R/W	Selects ***[PMDxMDOUT]*** / VExOUTCR transfer timing (PWM synchronous setting). 00: asynchronous to PWM (Note4) 01: Carrier bottom (when ***[PMDxMDCNT]*** =0x0001) 10: Carrier peak (***[PMDxMDCNT]*** = ***[PMDxMDPRD]***) 11: Carrier peak and carrier bottom Selects the subsequent stage buffer update timing of the conduction control register. (Note2)(Note3)(Note5)

Note1: This register must be set while ***[PMDxMDEN]***<PWMEN>=0.

Note2: By the combination of the settings for <PSYNCS> and <SYNCS>, the buffer update timing can be determined (refer to the "Table 3.2 Decode circuit outputs according to ***[PMDxMDOUT]*** / VExOUTCR and ***[PMDxMDCR]***<SYNTMD> setting").

Note3: When PMD is disabled (***[PMDxMDEN]***<PWMEN>=0), the timing is asynchronous regardless of settings.

Note4: When <SYNCS> and <PSYNCS> are set to "0", the setting is applied to the port output at the same time that the ***[PMDxMDOUT]*** / VExOUTCR registers.

Note5: When the PWM carrier is saw-tooth wave, the buffer update timing is the carrier peak, except <PSYNCS>=00

Note6: The connection destination depend on the product. For details, refer to "Product Information" of the reference manual.

4.2.12. *[PMDxMDOUT]* (PMD Conduction Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:11	—	0	R	Read as "0".
10	WPWM	0	R/W	W-phase PWM output setting 0: High/Low Output 1: PWM Output Port output is controlled by the combination of <WOC>, <WPWM>, ***[PMDxMDPOT]***<POLH>, <POLL> and ***[PMDxMDCR]*** <SYNTMD> (refer to the Table 4.2).
9	VPWM	0	R/W	V-phase PWM output setting 0: High/Low Output 1: PWM Output Port output is controlled by the combination of <VOC>, <VPWM>, ***[PMDxMDPOT]***<POLH>, <POLL> and ***[PMDxMDCR]*** <SYNTMD> (refer to the Table 4.2).
8	UPWM	0	R/W	U-phase PWM output setting 0: High/Low Output 1: PWM Output Port output is controlled by the combination of <UOC>, <UPWM>,***[PMDxMDPOT]***<POLH>,<POLL> and ***[PMDxMDCR]*** <SYNTMD> (refer to the Table 4.2)
7:6	—	0	R	Read as "0".
5:4	WOC[1:0]	00	R/W	W-phase conduction control setting Port output is controlled by the combination of <WOC>, <WPWM>, ***[PMDxMDPOT]***<POLH>, <POLL> and ***[PMDxMDCR]*** <SYNTMD> (refer to the Table 4.2).
3:2	VOC[1:0]	00	R/W	V-phase conduction control setting Port output is controlled by the combination of <VOC>, <VPWM>, ***[PMDxMDPOT]***<POLH>, <POLL> and ***[PMDxMDCR]*** <SYNTMD> (refer to the Table 4.2).
1:0	UOC[1:0]	00	R/W	U-phase conduction control setting Port output is controlled by the combination of <UOC>, <UPWM>, ***[PMDxMDPOT]***<POLH>, <POLL> and ***[PMDxMDCR]*** <SYNTMD> (refer to the Table 4.2).

Note1: When the ***[PMDxMDOUT]*** / VExOUTCR register updated by the bus is loaded to the subsequent stage buffer, set the bus mode (default) by writing "0" to ***[PMDxMODESEL]*** <MDSEL1>.

Note2: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note3: Since the conduction control register is double-buffered, the setting value can be changed during the operation of the PWM counter.

Note4: For detailed update timing of the subsequent stage buffer, refer to the "Table 3.1 ***[PMDxMDOUT]*** / VExOUTCR buffer Update Timing".

Note5: Read value is the first buffer value (the latest data set via a bus).

Table 4.2 Port Outputs according to <nOC>, <nPWM>, <POLH>,<POLL>and <SYNTMD> settings

[PMDxMDCR]<SYNTMD>=0
Polarity: Active high (***[PMDxMDPOT]***<POLH><POLL>=11)

Conduction control setting		PWM output setting <nPWM>			
Upper	Lower				
		0: H/L output		1: PWM output	
<nOC[1]>	<nOC[0]>	Upper phase	Lower phase	Upper phase	Lower phase
0	0	L	L	/PWMn	PWMn
0	1	L	H	L	PWMn
1	0	H	L	PWMn	L
1	1	H	H	PWMn	/PWMn

[PMDxMDCR]<SYNTMD>=0
Polarity: Active low (***[PMDxMDPOT]***<POLH><POLL>=00)

Conduction control setting		PWM output setting <nPWM>			
Upper	Lower				
		0: H/L output		1: PWM output	
<nOC[1]>	<nOC[0]>	Upper phase	Lower phase	Upper phase	Lower phase
0	0	H	H	PWMn	/PWMn
0	1	H	L	H	/PWMn
1	0	L	H	/PWMn	H
1	1	L	L	/PWMn	PWMn

[PMDxMDCR]<SYNTMD>=1
Polarity: Active high (***[PMDxMDPOT]***<POLH><POLL>=11)

Conduction control setting		PWM output setting <nPWM>			
Upper	Lower				
		0: H/L output		1: PWM output	
<nOC[1]>	<nOC[0]>	Upper phase	Lower phase	Upper phase	Lower phase
0	0	L	L	/PWMn	PWMn
0	1	L	H	L	/PWMn
1	0	H	L	PWMn	L
1	1	H	H	PWMn	/PWMn

[PMDxMDCR]<SYNTMD>=1
Polarity: Active low (***[PMDxMDPOT]***<POLH><POLL>=00)

Conduction control setting		PWM output setting <nPWM>			
Upper	Lower				
		0: H/L output		1: PWM output	
<nOC[1]>	<nOC[0]>	Upper phase	Lower phase	Upper phase	Lower phase
0	0	H	H	PWMn	/PWMn
0	1	H	L	H	PWMn
1	0	L	H	/PWMn	H
1	1	L	L	/PWMn	PWMn

Note1: n = U, V, W

Note2: PWMn: PWM signal of PWM compare setting /PWMn: Inversion signal of PWMn

4.2.13. *[PMDxEMGREL]* (EMG Release Register)

Bit	Bit Symbol	After reset	Type	Function
31:8	—	0	R	Read as "0".
7:0	EMGREL[7:0]	0x00	W	EMG/OVV disable code By setting "0x5A" → "0xA5", EMG function and OVV function can be disabled. After writing the disable code, set ***[PMDxEMGCR]***<EMGEN>=0 or ***[PMDxOVVCR]***<OVVEN>=0 continuously.

Note: Write a disable code each at disabling EMG and OVV.

4.2.14. *[PMDxEMGCR]* (EMG Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:12	—	0	R	Read as "0".
11:8	EMGCNT[3:0]	0x0	R/W	EMGx_N input detection time 0x0 to 0xF (When <EMGCNT>=0x0, the noise filter is bypassed.) The noise filtering length of anomaly detection input set to these bits. And this value can be calculated by following formula. <EMGCNT[3:0]> × 16/fsys Please set it while EMG protection is prohibited (<EMGEN>=0). (Note1)
7:6	—	0	R	Read as "0".
5	INHEN	1	R/W	Debug halt enable/disable 0: Disable 1: Enable (Enabled in the initial status) This bit selects whether or not to stop the PMD when the debug halt signal is input.
4:3	EMGMD[1:0]	11	R/W	EMG protection mode select (Note2) 00: All phases High-impedance 01: All upper-phases ON / all lower-phases High-impedance 10: All upper-phases High-impedance / all lower-phases ON 11: All phases High-impedance ON indicates that PWM output continues. Sets the port output both the upper (UOx, VOx, WOx) and the lower (XOx, YOx, ZOx) for the case when EMG occurs.
2	—	0	R/W	Always write "0".
1	EMGRS	0	W	EMG protection release 0: Don't care 1: Release protection After setting "0x000" in the ***[PMDxMDOUT]*** / VExOUTCR register (Note3), confirm that ***[PMDxEMGSTA]***<EMGI> becomes "1", then set "1" to <EMGRS>. It returns from the EMG protection state. Always reads as "0".
0	EMGEN	1	R/W	EMG protection circuit enable/disable 0: Disable 1: Enable (Enabled in the initial status) To disable the function, write "0x5A" and then write "0xA5" to the EMG release register (***[PMDxEMGREL]***). Then, set "0" to <EMGEN> (These three instructions must be executed consecutively.).

Note1: If <EMGCNT> is changed while EMG protection circuit is enabled, it may become the protection state. Therefore, when <EMGCNT> is changed, please release the protection state by the following procedure:

(1) ***[PMDxEMGSTA]***<EMGI> should be read to confirm its value is "1".
(2) ***[PMDxMDOUT]*** / VExOUTCR <UPWM>, <VPWM>, <WPWM>, <UOC>, <VOC>, and <WOC> should be set to "0" to set all port outputs to inactive state.
(3) <EMGRS> of ***[PMDxEMGCR]*** / VExEMGRS should be set to "1" to exit EMG protection state.

Note2: <EMGMD> protection mode setting is prioritized when OVV and EMG occur at the same time.

Note3: EMG protection cannot be released if the subsequent stage buffer of ***[PMDxMDOUT]*** / VExOUTCR is not updated to "0x000".

4.2.15. *[PMDxEMGSTA]* (EMG Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	—	0	R	Read as "0".
1	EMGI	Undefined	R	EMGx_N input state 0: Active input. 1: Inactive input. EMGx_N input status can be checked by reading this bit.
0	EMGST	0	R	EMG protection state 0: Normal operation 1: Protected EMG protection status can be checked by reading this bit.

4.2.16. *[PMDxOVVCR]* (OVV Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:12	—	0	R	Read as "0".
11:8	OVVCNT[3:0]	0x0	R/W	OVV input detection time 0x1 to 0xF (If 0x0 is set, it is handled as 0x1.) The noise filtering length of OVV input set to these bits. And this value can be calculated by following formula. <OVVCNT[3:0]> × 16/fsys Please set it while OVV protection is prohibited(<OVVEN>=0).
7	—	0	R	Read as "0".
6	ADIN1EN	0	R/W	AD monitor function 1 input enable (Note1) 0: Disable input 1: Enable input Selects enable/disable signals from AD monitor function 1 of the ADC. If you enable it and select AD monitor function signal for input (<OVVISEL>=1), the results of the AD monitor function 1 as OVV inputs (if OVV protection is enabled).
5	ADIN0EN	0	R/W	AD monitoring function 0 input enable (Note1) 0: Disable input 1: Enable input Selects enable/disable signals from AD monitor function 0 of the ADC. If you enable it and select AD monitor function signal for input (<OVVISEL>=1), the results of the AD monitor function 0 as OVV inputs (if OVV protection is enabled).
4:3	OVVMD[1:0]	00	R/W	Selects OVV protection mode (Note2) 00: No output control 01: All upper-phases ON, all lower-phases OFF 10: All upper-phases OFF, all lower-phases ON 11: All phases OFF This field controls the outputs of the upper (UOx, VOx, WOx) and lower(XOx, YOx, ZOx) phases when an OVV condition occurs. ON indicates that it's fixed to active output. OFF indicates that it's fixed inactive output. Active and inactive are depends on the settings of <POLL> and <POLH>.

Bit	Bit Symbol	After reset	Type	Function
2	OVVISEL	0	R/W	Selects OVV input 0: OVVx_N pin input 1: AD monitor function signal This bit selects whether to use port input or the monitor signal from the ADC as the OVV signal to be input to the protection circuit. When the AD monitor function signal is selected, the setting of OVV input detection time <OVVCNT[3:0]> becomes invalid.(Direct input)
1	OVVRS	0	R/W	Selects OVV protection state release 0: Disable automatic release of OVV protection state 1: Enable automatic release of OVV protection state If automatic release of OVV protection is enabled, when the state changes to OVV protection after detecting anomaly (OVV input makes a high-to-low transition), the OVV protection state can be automatically released when updating the buffer of PWM period register ***[PMDxMDPRD]*** after the OVV input transition to high. (Refer to the "Table 4.1 ***[PMDxMDPRD]***, ***[PMDxCMPU/V/W]*** buffer Update Timing".)
0	OVVEN	0	R/W	OVV protection circuit enable/disable 0: Disable 1: Enable To disable the function, write "0x5A" and then write "0xA5" to the EMG release register (***[PMDxEMGREL]***). Then, set "0" to <OVVEN>. (These three instructions must be executed consecutively.)

Note1: Refer to the chapter "AD Monitor Function" in the Reference Manual of "12-bit Analog to Digital Converter" for detailed information about AD monitor function.

Note2: If OVV and EMG conditions occur simultaneously, the protection mode settings in the bits of <EMGMD[1:0]> become effective.

4.2.17. *[PMDxOVVSTA]* (OVV Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	—	0	R	Read as "0".
1	OVVI	Undefined	R	OVVI input state 0: Active input. 1: Inactive input. OVVI input status can be checked by reading this bit.
0	OVVST	0	R	OVV protection state 0: Normal operation 1: In protected OVV protection status can be checked by reading this bit.

4.2.18. *[PMDxDTR]* (Dead time Register)

Bit	Bit Symbol	After reset	Type	Function
31:8	—	0	R	Read as "0".
7:0	DTR[7:0]	0x00	R/W	Sets dead time 0x00 to 0xFF The dead time value can be calculated by following formula. ***[PMDxDTR]*** × 8/fsys

Note: Do not change ***[PMDxDTR]*** register while ***[PMDxMDEN]***<PWMEN> =1.

4.2.19. *[PMDxTRGCMP0]* (Trigger Compare 0 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	TRGCMP0[15:0]	0x0000	R/W	Trigger output compare register Range: 0x0001 to [***[PMDxMDPRD]*** value - 1]. When the PWM counter value ***[PMDxMDCNT]*** matches the value set in ***[PMDxTRGCMP0]***, TRG0 is output. Note: It is prohibited to set ***[PMDxTRGCMP0]*** to "0x0000" and ***[PMDxTRGCMP0]*** ≥ ***[PMDxMDPRD]***.

Note1: When the compare register updated by the bus is loaded to the subsequent stage buffer, set the bus mode (default) by writing "0" to ***[PMDxMODESEL]*** <MDSEL2>.

Note2: Do not write to this register in byte unit. If the upper 8 bits[15:8] and the lower 8 bits[7:0] are written separately, operation cannot be guaranteed.

Note3: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.

Note4: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 ***[PMDxTRGCMPn]*** buffer Update Timing".

Note5: Read value is the first buffer value (the latest data set via a bus).

Note6: If PWM(<PWMEN>=1) is started while ***[PMDxTRGCMPn]***(n=0 to 3) is set to "0x0001" with saw-tooth wave carrier(<PWMMD>=0), there is no trigger output in the first PWM cycle.

Table 4.3 *[PMDxTRGCMPn]* buffer Update Timing

[PMDxTRGSYNCR] <TSYNCS>setting	*[PMDxTRGCR]* <TRGnMD>setting	*[PMDxTRGCMPn]* Buffer update timing
00	000	Updates immediately
	001	Update when PWM carrier peak
	010	Update when PWM carrier bottom
	011	Update when PWM carrier peak or PWM carrier bottom (Note1)
	1xx	Updates immediately
01	xxx	Update when PWM carrier bottom
10	xxx	Update when PWM carrier peak
11	xxx	Update when PWM carrier peak or PWM carrier bottom (Note1)

Note1: Updates at carrier peak when saw-tooth wave carrier is selected (***[PMDxMDCR]***<PWMMD>=0).

Note2: x: Don't care

Note3: When ***[PMDxMDEN]***<PWMEN>=0, the immediate update is done regardless of the setting.

4.2.20. *[PMDxTRGCMP1]* (Trigger Compare 1 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	TRGCMP1[15:0]	0x0000	R/W	Trigger output compare register Range: 0x0001 to [***[PMDxMDPRD]*** value - 1]. When the PWM counter value ***[PMDxMDCNT]*** matches the value set in ***[PMDxTRGCMP1]***, TRG1 is output. Note: It is prohibited to set ***[PMDxTRGCMP1]*** to "0x0000" and ***[PMDxTRGCMP1]*** ≥ ***[PMDxMDPRD]***.

Note1: When the compare register updated by the bus is loaded to the subsequent stage buffer, set the bus mode (default) by writing "0" to ***[PMDxMODESEL]*** <MDSEL2>.

Note2: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note3: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.

Note4: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 ***[PMDxTRGCMPn]*** buffer Update Timing".

Note5: Read value is the first buffer value (the latest data set via a bus).

Note6: If PWM is started(<PWMEN>=1) while ***[PMDxTRGCMPn]***(n=0 to 3) is set to "0x0001" with saw-tooth wave carrier(<PWMMD>=0), there is no trigger output in the first PWM cycle.

4.2.21. *[PMDxTRGCMP2]* (Trigger Compare 2 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	TRGCMP2[15:0]	0x0000	R/W	Trigger output compare register Range: 0x0001 to [***[PMDxMDPRD]*** value - 1]. When the PWM counter value ***[PMDxMDCNT]*** matches the value set in ***[PMDxTRGCMP2]***, TRG2 is output. Note: It is prohibited to set ***[PMDxTRGCMP2]*** to" 0x0000" and ***[PMDxTRGCMP2]*** ≥ ***[PMDxMDPRD]***.

Note1: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note2: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.

Note3: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 ***[PMDxTRGCMPn]*** buffer Update Timing".

Note4: Read value is the first buffer value (the latest data set via a bus).

Note5: If PWM is started(<PWMEN>=1) while ***[PMDxTRGCMPn]***(n=0 to 3) is set to "0x0001" with saw-tooth wave carrier(<PWMMD>=0), there is no trigger output in the first PWM cycle.

4.2.22. *[PMDxTRGCMP3]* (Trigger Compare 3 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15:0	TRGCMP3[15:0]	0x0000	R/W	Trigger output compare register Range: 0x0001 to [***[PMDxMDPRD]*** value- 1]. When the PWM counter value ***[PMDxMDCNT]*** matches the value set in ***[PMDxTRGCMP3]***, TRG3 is output. Note: It is prohibited to set ***[PMDxTRGCMP3]*** to "0x0000" and ***[PMDxTRGCMP3]*** ≥ ***[PMDxMDPRD]***.

Note1: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note2: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.

Note3: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 ***[PMDxTRGCMPn]*** buffer Update Timing".

Note4: Read value is the first buffer value (the latest data set via a bus).

Note5: If PWM is started(<PWMEN>=1) while ***[PMDxTRGCMPn]***(n=0 to 3) is set to "0x0001" with saw-tooth wave carrier(<PWMMD>=0), there is no trigger output in the first PWM cycle.

4.2.23. *[PMDxTRGCR]* (Trigger Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	—	0	R	Read as "0".
15	TRG3BE	0	R/W	Asynchronous update of the ***[PMDxTRGCMP3]*** buffer This bit enables asynchronous updating to the subsequent stage buffer from ***[PMDxTRGCMP3]***. (Note1) (Note2) 0: Synchronous update 1: Asynchronous update (The value written to ***[PMDxTRGCMP3]*** is immediately reflected.)
14:12	TRG3MD[2:0]	000	R/W	***[PMDxTRGCMP3]*** mode setting This register selects a match-mode of trigger output(TRG3). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled
11	TRG2BE	0	R/W	Asynchronous update of the ***[PMDxTRGCMP2]*** buffer This bit enables asynchronous updating to the subsequent stage buffer from ***[PMDxTRGCMP2]***. (Note1) (Note2) 0: Synchronous update 1: Asynchronous update (The value written to ***[PMDxTRGCMP2]*** is immediately reflected.)
10:8	TRG2MD[2:0]	000	R/W	***[PMDxTRGCMP2]*** mode setting This register selects a match-mode of trigger output(TRG2). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled
7	TRG1BE	0	R/W	Asynchronous update of the ***[PMDxTRGCMP1]*** / VExTRGCMP1 buffer This bit enables asynchronous updating to the subsequent stage buffer from ***[PMDxTRGCMP1]***. (Note1) (Note2) 0: Synchronous update 1: Asynchronous update (The value written to ***[PMDxTRGCMP1]*** is immediately reflected.)
6:4	TRG1MD[2:0]	000	R/W	***[PMDxTRGCMP1]*** / VExTRGCMP1 mode setting This register selects a match-mode of trigger output(TRG1). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled

Bit	Bit Symbol	After reset	Type	Function
3	TRG0BE	0	R/W	Asynchronous update of the ***[PMDxTRGCMP0]*** / VExTRGCMP0 buffer This bit enables asynchronous updating to the subsequent stage buffer from ***[PMDxTRGCMP0]***. (Note1)(Note2) 0: Synchronous update 1: Asynchronous update (The value written to ***[PMDxTRGCMP0]*** is immediately reflected.)
2:0	TRG0MD[2:0]	000	R/W	***[PMDxTRGCMP0]*** / VExTRGCMP0 mode setting This register selects a match-mode of trigger output(TRG0). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled

Note1: When ***[PMDxMDEN]***<PWMEN>=0, updates asynchronously regardless of setting.

Note2: For detailed update timing, refer to the "Table 4.3 ***[PMDxTRGCMPn]*** buffer Update Timing".

Note3: When a "0" is set to ***[PMDxMDCR]***<PWMMD> (Saw-tooth wave), please do not select.

Note4: If PWM is started(<PWMEN>=1) while ***[PMDxTRGCMPn]***(n=0 to 3) is set to "0x0001" with saw-tooth wave carrier(<PWMMD>=0), there is no trigger output in the first PWM cycle.

Note5: When ***[PMDxTRGCMPn]***=0x0001 (n=0 to 3) and ***[PMDxMDCR]***<PWMMD>=1 (triangular wave), one trigger output is made per period.

4.2.24. *[PMDxTRGSYNCR]* (Trigger Update Timing Setting Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	—	0	R	Read as "0".
1:0	TSYNCS[1:0]	00	R/W	Update timing setting for the buffer of the trigger compare register. 00: PWM carrier bottom or PWM carrier peak is set for each trigger by setting ***[PMDxTRGCR]***<TRGnMD> (n=0 to 3). 01: PWM carrier bottom 10: PWM carrier peak 11: PWM carrier peak and PWM carrier bottom

Note1: Asynchronous update ***[PMDxMDEN]***<PWMEN>=0 regardless of setting.

Note2: Refer to the "Table 4.3 ***[PMDxTRGCMPn]*** buffer Update Timing".

4.2.25. *[PMDxTRGMD]* (Trigger Output Mode Setting Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	—	0	R	Read as "0".
1	TRGOUT	0	R/W	Trigger output mode 0: Fixed trigger output 1: Variable trigger output When fixed trigger outputs are selected, trigger outputs from PMDxTRG0 to PMDxTRG3 output the trigger signals generated by a match with ***[PMDxTRGCMP0]*** to ***[PMDxTRGCMP3]*** respectively. A PMDxTRG4 and a PMDxTRG5 are not output the trigger signals. When variable trigger output is selected, output signals of the ***[PMDxTRGCMP0]*** are output to one of trigger output from PMDxTRG0 to PMDxTRG5. The trigger output signal is selected by trigger output select register.(Note)
0	EMGTGE	0	R/W	Output enable in EMG protection state 0: Disable trigger output in the protection state 1: Enable trigger output in the protection state This bit enables or disables trigger output in the EMG protection state.

Note: Refer to the "Table 4.4 Trigger Output Patterns" when variable trigger outputs is selected (<TRGOUT>=1).

Table 4.4 Trigger Output Patterns

<TRGOUT> Setting	Compare Register	<TRGSEL> Setting	Trigger Output
<TRGOUT>=0	***[PMDxTRGCMP0]***	N/A	PMDxTRG0
	[PMDxTRGCMP1]		PMDxTRG1
	[PMDxTRGCMP2]		PMDxTRG2
	[PMDxTRGCMP3]		PMDxTRG3
<TRGOUT>=1	***[PMDxTRGCMP0]***	0	PMDxTRG0
		1	PMDxTRG1
		2	PMDxTRG2
		3	PMDxTRG3
		4	PMDxTRG4
		5	PMDxTRG5
	[PMDxTRGCMP1]	N/A	No trigger output
	[PMDxTRGCMP2]	N/A	No trigger output
	[PMDxTRGCMP3]	N/A	No trigger output

4.2.26. *[PMDxTRGSEL]* (Trigger Output Select Register)

Bit	Bit Symbol	After reset	Type	Function
31:3	—	0	R	Read as "0".
2:0	TRGSEL[2:0]	000	R/W	Trigger output select 000: Output from PMDxTRG0 001: Output from PMDxTRG1 010: Output from PMDxTRG2 011: Output from PMDxTRG3 100: Output from PMDxTRG4 101: Output from PMDxTRG5 110: No trigger output 111: No trigger output This field is effective when the variable trigger output mode is selected (***[PMDxTRGMD]***<TRGOUT>=1). And an output trigger can be selected by setting the ***[PMDxTRGCMP0]*** register. (Refer to the "Table 4.4 Trigger Output Patterns".)

Note1: When the compare register updated by the bus is loaded to the subsequent stage buffer, set the bus mode (default) by writing "0" to ***[PMDxMODESEL]***<MDSEL3>.

Note2: Since the trigger output selecting register is double-buffered, this register can be changed during the operation of the PWM counter.

Note3: The update timing of the subsequent stage buffer is as the same as the compare register (***[PMDxCMPU/V/W]***).

Note4: When PMD is disabled (***[PMDxMDEN]***<PWMEN>=0), updates asynchronously.

5. Precautions

- When PMD cooperate with a ADC, please refer to the reference manual "12-bit Analog to Digital Convertor".
- The byte write of registers is disabled regardless of whether PWM is operating or stopped.
- ***[PMDxMDCNT]*** value has changed during PWM operation. Therefore, the byte read of ***[PMDxMDCNT]*** should not be done. Read should be done with Word or Half-word unit.
- The following registers have the double-buffer structure. The data written to these registers is transferred to the subsequent stage buffer at each update timing (depending on the setting).

  – ***[PMDxCMPU]***, ***[PMDxCMPV]***, ***[PMDxCMPW]***
  – ***[PMDxMDOUT]***
  – ***[PMDxTRGSEL]***
  – ***[PMDxMDPRD]***
  – ***[PMDxTRGCMP0]*** to ***[PMDxTRGCMP3]***

- Even in the setting of ***[PMDxMDCR]***<PWMMD>=1(Triangular wave carrier) and ***[PMDxTRGCR]*** <TRGnMD> =011(Trigger output at up/down-count match), when ***[PMDxTRGCMPn]*** (n=0 to 3) setting is "0x0001", TRGn is generated only once in the PWM period.
- The PWM carrier is set to the saw-tooth wave, and ***[PMDxTRGCMPn]*** (n=0 to 3) is set to "0x0001". Then, if ***[PMDxMDEN]***<PWMEN> is changed to enable, the TRGn is not generated in the first PWM period.
- Be sure to release processing from the EMG protection state before using the PMD(After setting PORT).
- The EMG protection function is enabled after reset. If it is not used, prohibit it with the following procedure.

  (1) ***[PMDxEMGREL]*** should be set to "0x5A".
  (2) ***[PMDxEMGREL]*** should be set to "0xA5".
  (3) ***[PMDxEMGCR]***<EMGEN> should be set to "0".

  Note: These 3 instructions must be executed consecutively.

- When attempting to stop supplying the clock, make sure to check whether the PMD is stopping. Note that when the MCU shift STOP1/STOP2 mode, make sure to check whether the PMD is stopping as well.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2018-10-03	First release

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