

TOSHIBA Transistor Silicon PNP / NPN Epitaxial Type (PCT Process)

# HN4B102J

## MOS Gate Drive Applications Switching Applications

- Small footprint due to a small and thin package
- High DC current gain : PNP  $h_{FE} = 200$  to  $500$  ( $I_C = -0.2$  A)  
: NPN  $h_{FE} = 200$  to  $500$  ( $I_C = 0.2$  A)
- Low collector-emitter saturation : PNP  $V_{CE(sat)} = -0.20$  V (max)  
: NPN  $V_{CE(sat)} = 0.14$  V (max)
- High-speed switching : PNP  $t_f = 40$  ns (typ.)  
: NPN  $t_f = 45$  ns (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating		Unit
			PNP	NPN	
Collector-base voltage		$V_{CBO}$	-30	60	V
Collector-emitter voltage		$V_{CEO}$	-30	30	V
Emitter-base voltage		$V_{EBO}$	-7	7	V
Collector current	DC (Note 1)	$I_C$	-1.8	2.0	A
	Pulse (Note 1)	$I_{CP}$	-8.0	8.0	
Base current		$I_B$	-0.5	0.5	A
Collector power dissipation (t = 10 s)	Single-device operation	$P_C$ (Note 2)	1.1		W
Collector power dissipation (DC)	Single-device operation	$P_C$ (Note 2)	0.75		W
Junction temperature		$T_j$	150		°C
Storage temperature range		$T_{stg}$	-55 to 150		°C

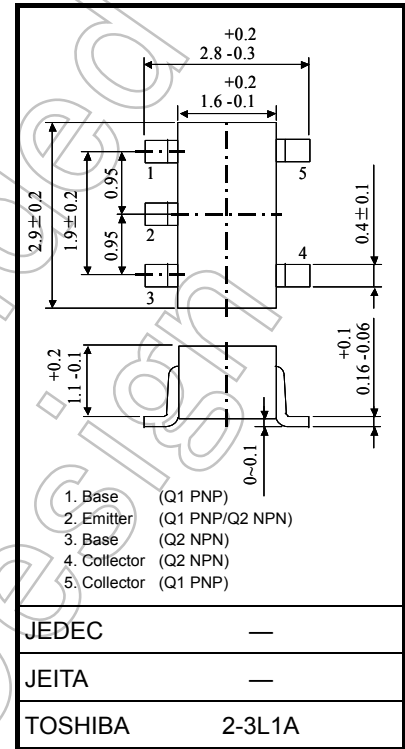
Note 1: Ensure that the channel temperature does not exceed 150°C during use of the device.

Note 2: Mounted on an FR4 board (glass-epoxy; 1.6 mm thick; Cu area, 645 mm<sup>2</sup>)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

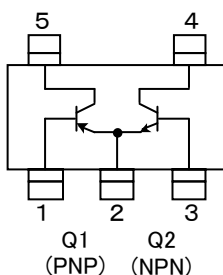
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm

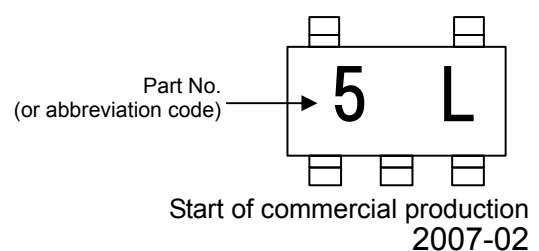


Weight: 0.014g (typ.)

**Figure 1 Circuit Configuration (top view)**



**Figure 2 Marking**



## Electrical Characteristics (Ta = 25°C)

### PNP

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		$I_{CBO}$	$V_{CB} = -30\text{ V}, I_E = 0$	—	—	-100	nA
Emitter cut-off current		$I_{EBO}$	$V_{EB} = -7\text{ V}, I_C = 0$	—	—	-100	nA
Collector-emitter breakdown voltage		$V_{(BR)CEO}$	$I_C = -10\text{ mA}, I_B = 0$	-30	—	—	V
DC current gain		$h_{FE}(1)$	$V_{CE} = -2\text{ V}, I_C = -0.2\text{ A}$	200	—	500	
		$h_{FE}(2)$	$V_{CE} = -2\text{ V}, I_C = -0.6\text{ A}$	125	—	—	
		$h_{FE}(3)$	$V_{CE} = -2\text{ V}, I_C = -2.0\text{ A}$	40	—	—	
Collector-emitter saturation voltage		$V_{CE(sat)}$	$I_C = -0.6\text{ A}, I_B = -20\text{ mA}$	—	—	-0.20	V
Base-emitter saturation voltage		$V_{BE(sat)}$	$I_C = -0.6\text{ A}, I_B = -20\text{ mA}$	—	—	-1.10	V
Collector output capacitance		$C_{ob}$	$V_{CB} = -10\text{ V}, I_E = 0, f = 1\text{ MHz}$	—	16.5	—	pF
Switching time	Rise time	$t_r$	See Figure 3 circuit diagram $V_{CC} \approx -18\text{ V}, R_L = 30\ \Omega$ $I_{B1} = I_{B2} = 20\text{ mA}$	—	40	—	ns
	Storage time	$t_{stg}$		—	280	—	
	Fall time	$t_f$		—	40	—	

### NPN

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		$I_{CBO}$	$V_{CB} = 60\text{ V}, I_E = 0$	—	—	100	nA
Emitter cut-off current		$I_{EBO}$	$V_{EB} = 7\text{ V}, I_C = 0$	—	—	100	nA
Collector-emitter breakdown voltage		$V_{(BR)CEO}$	$I_C = 10\text{ mA}, I_B = 0$	30	—	—	V
DC current gain		$h_{FE}(1)$	$V_{CE} = 2\text{ V}, I_C = 0.2\text{ A}$	200	—	500	
		$h_{FE}(2)$	$V_{CE} = 2\text{ V}, I_C = 0.6\text{ A}$	125	—	—	
		$h_{FE}(3)$	$V_{CE} = 2\text{ V}, I_C = 2.0\text{ A}$	40	—	—	
Collector-emitter saturation voltage		$V_{CE(sat)}$	$I_C = 0.6\text{ A}, I_B = 20\text{ mA}$	—	—	0.14	V
Base-emitter saturation voltage		$V_{BE(sat)}$	$I_C = 0.6\text{ A}, I_B = 20\text{ mA}$	—	—	1.10	V
Collector output capacitance		$C_{ob}$	$V_{CB} = 10\text{ V}, I_E = 0, f = 1\text{ MHz}$	—	14	—	pF
Switching time	Rise time	$t_r$	See Figure 4 circuit diagram $V_{CC} \approx 18\text{ V}, R_L = 30\ \Omega$ $I_{B1} = I_{B2} = 20\text{ mA}$	—	45	—	ns
	Storage time	$t_{stg}$		—	580	—	
	Fall time	$t_f$		—	45	—	

Figure 3. Switching Time Test Circuit & Timing Chart

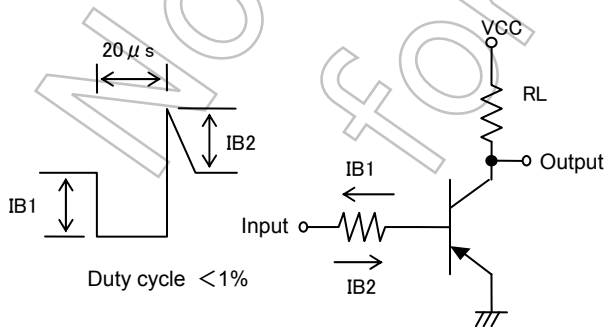
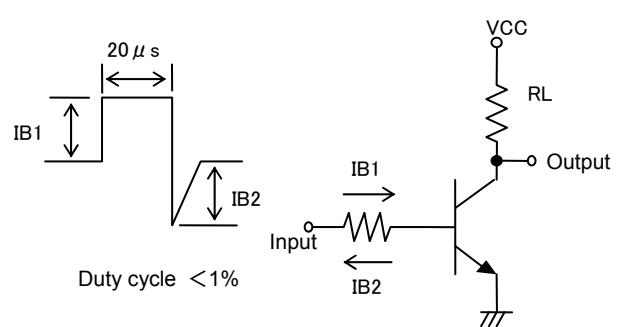
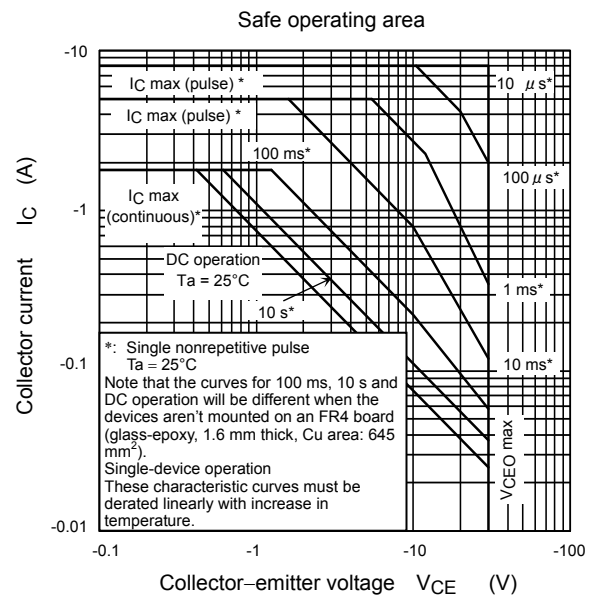
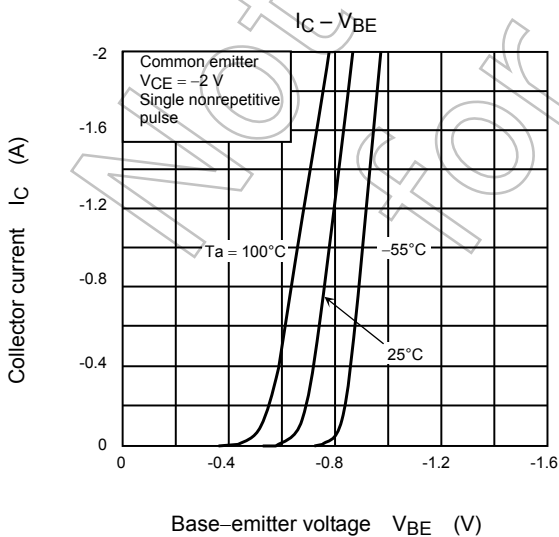
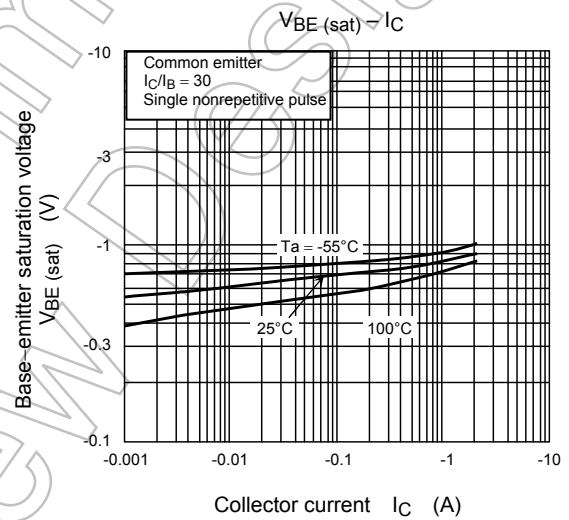
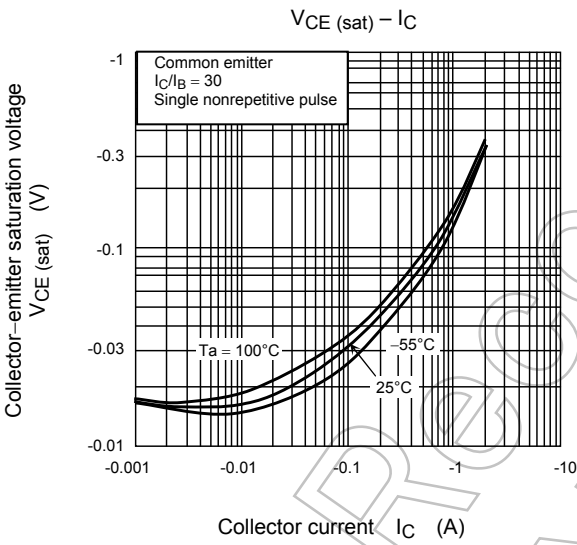
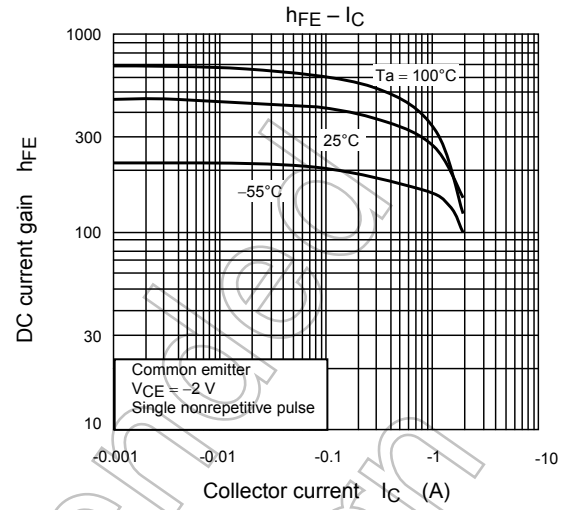
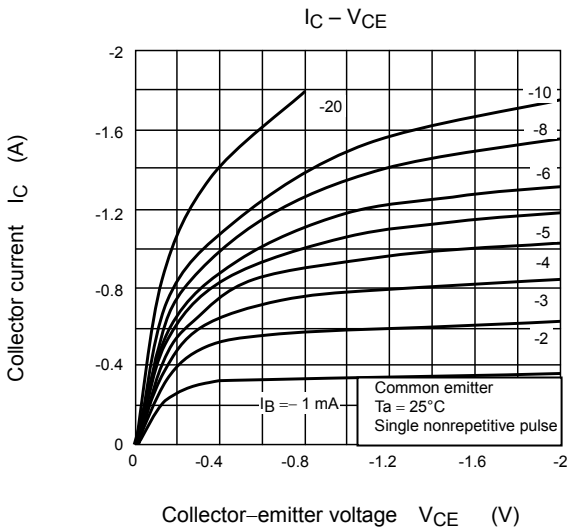


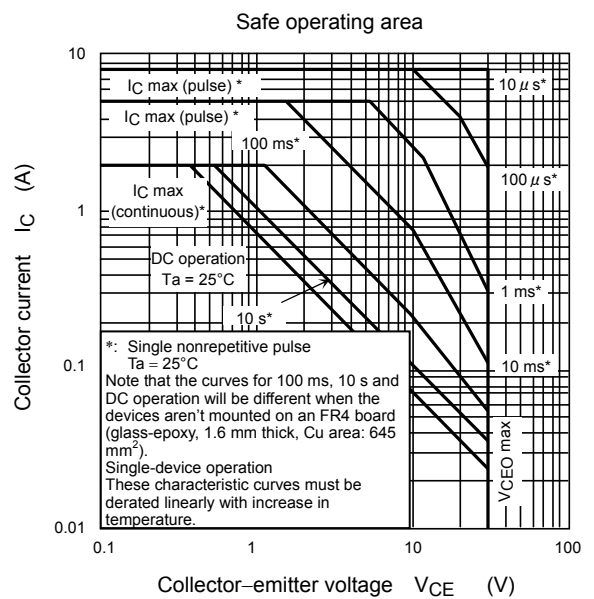
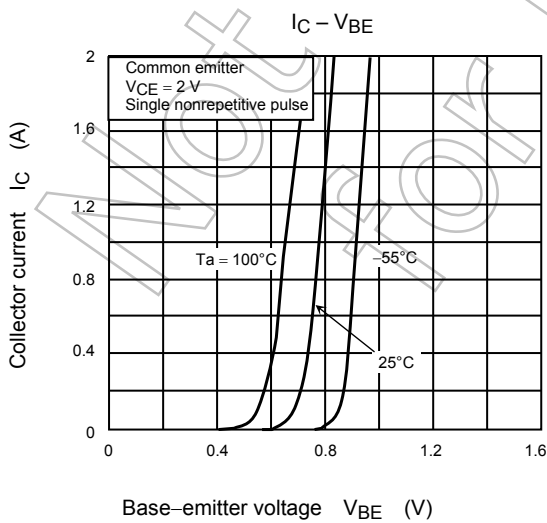
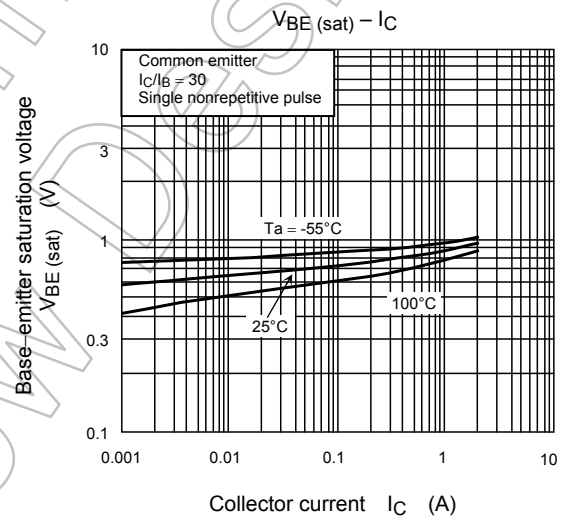
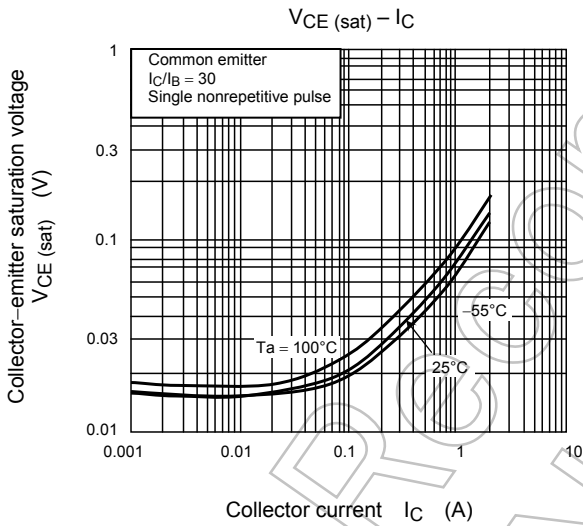
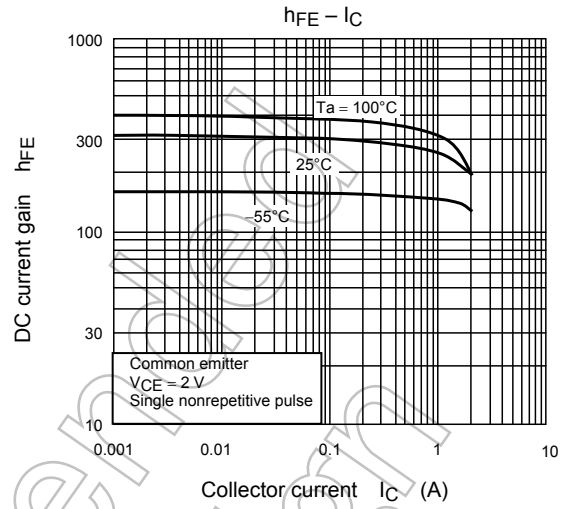
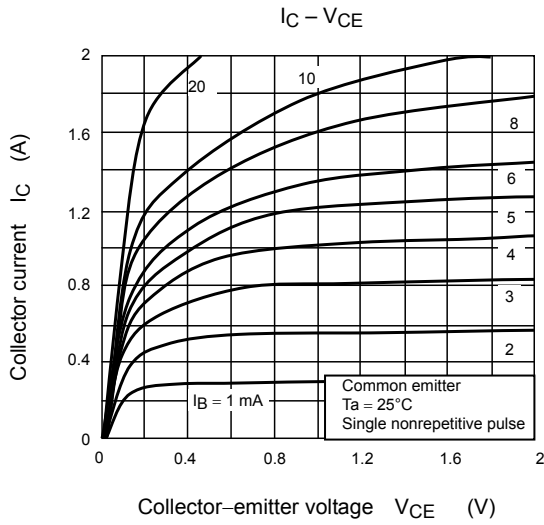
Figure 4. Switching Time Test Circuit & Timing Chart



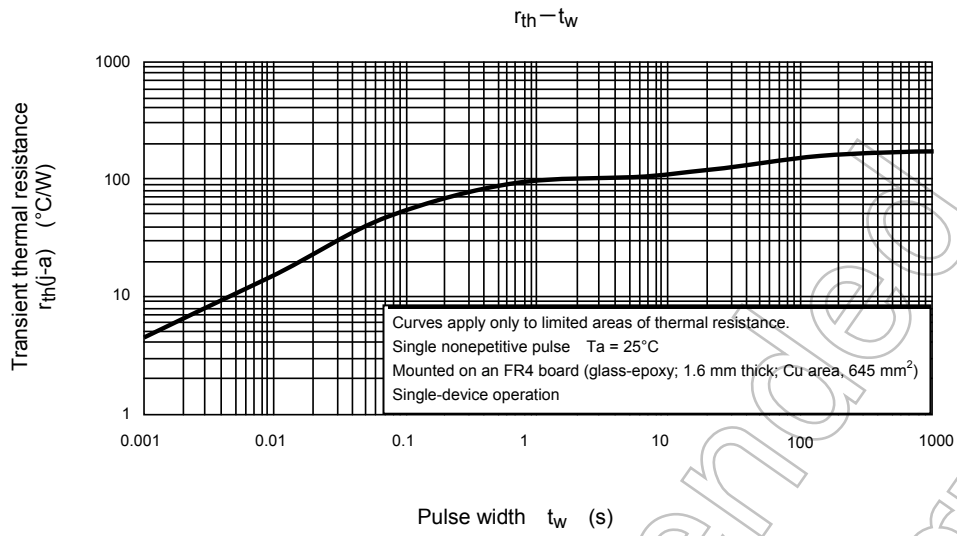
PNP



## NPN



Common



Not Recommended for New Design

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