CMOS Logic IC VHC/VHCT/VHCV (Verry High Speed) Series Outline

Outline:

CMOS Logic ICs VHC/VHCT/VHCV series realize high speed operation (up to 90 MHz) with low-noise performance, and is commonly used in high speed applications.
This document provides an overview of the product, part numbering method, maximum ratings, electrical characteristics, and measurement methods.

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1. General

1.1. General

This document describes the VHC series of C^{2}MOS^{TM} Logic ICs.

The VHC series is indicated by the red frame in Figure 1.1.

This series realizes both high-speed and low-noise performance, and since the speed is highest under the condition of 5 V and light load, the series is most commonly used in applications requiring high-speed operation.

The package lineup is wide, from DIP package to ultra-compact US package.

Table 1.1 shows the outline of the VHC series.

Table 1.1 Outline of VHC Series

Series	Definition
VHC	CMOS level input of VHC series
VHCT	TTL level input of VHC series
VHC9	Schmitt circuit-type input of VHC series
VHCV	Schmitt circuit-type input of VHC series Capable of handling twice as much output current as other products in VHC series

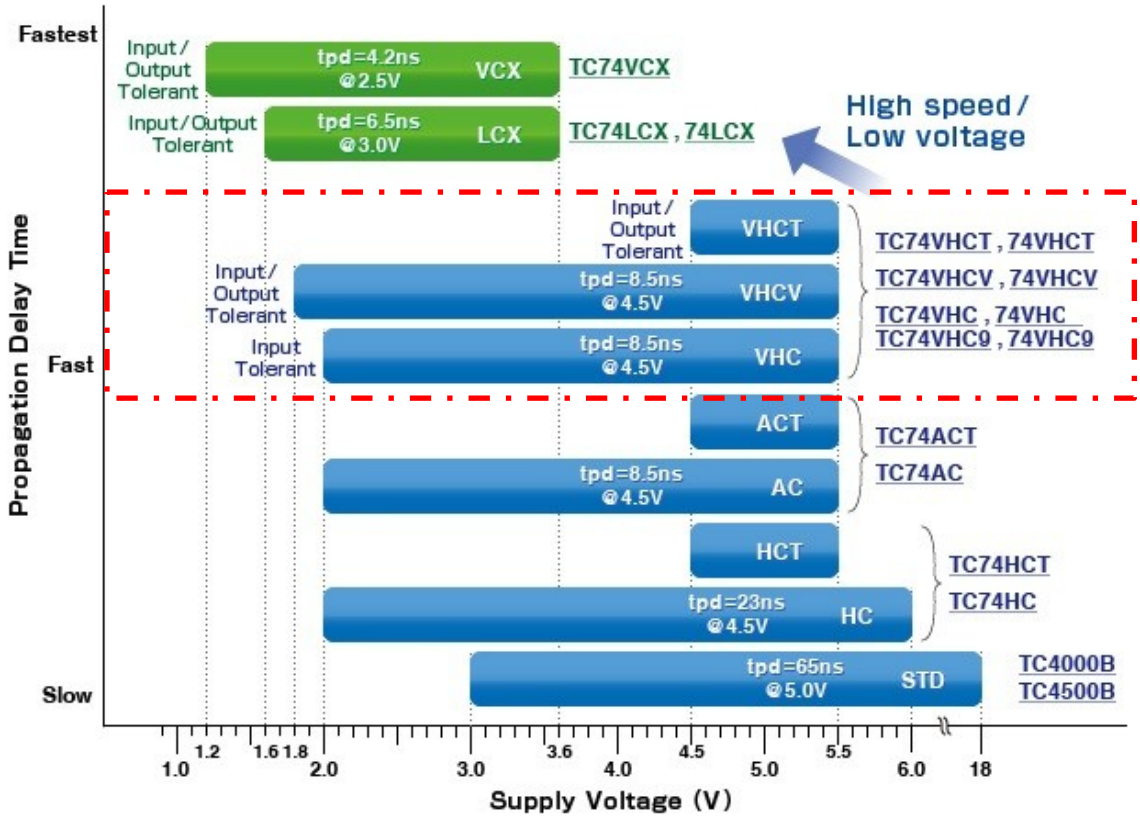


Figure 1.1 Supply Voltage Range and Propagation Delay Time of Each Series

1.2. Features

1.2.1. High-Speed/Low-Voltage Operation

Switching speed of the VHC series is faster than that of the AC series operating at 5 V in light load region, the load capacitance is 50 pF or less, and switching speed operating at 3 V is faster than that of the HC series operating at 5 V.

Figure 1.2 shows output load capacitance vs. switching speed.

- Propagation Delay Time (gate) 3.5 ns Typ. (@5 V, C_L=15 pF)
  5.5 ns Typ. (@3 V, C_L=15 pF)
- Maximum Clock Frequency (flip-flop) 170 MHz Typ. (@5 V, C_L=15 pF)
  125 MHz Typ. (@3 V, C_L=15 pF)

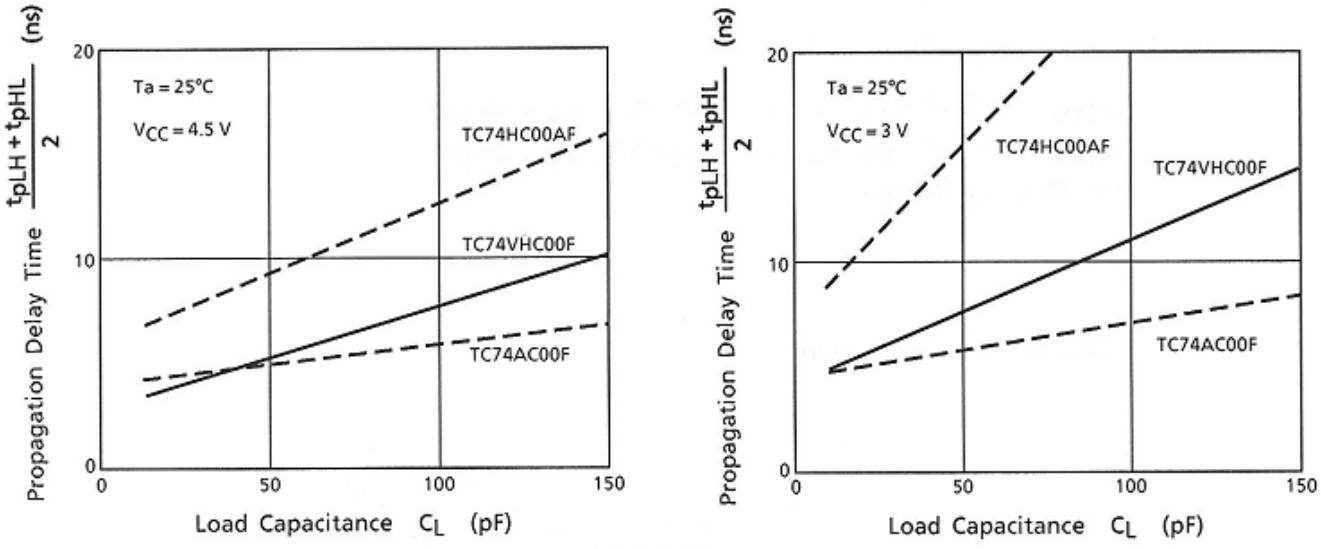


Figure 1.2 Propagation Delay Time vs. Load Capacitance

1.2.2. Low Noise

Radical output transitions with high-speed switching would normally generate output noise such as overshoot and undershoot.

The VHC series is equipped with SRC (SLEW RATE CONTROL) circuit. The SRC circuit reduces switching noise and suppresses di / dt of output, because a time difference is set so that the output buffers do not turn on at the same time.

Table 1.2 shows the quiet output noise waveforms. Compared with the TC74AC244F and TC74HC244AF, the TC74VHC244F's voltage fluctuation is small.

● Low-Noise Performance (TC74VHC244) ····· V_{OLP}, V_{OLV} 0.5 V Typ. (@5 V, C_L=50 pF)

Table 1.2 Definition of Parameters

Parameter	Symbol	Definition
Quiet output maximum dynamic V_{OL}	V_{OLP}	The maximum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.
Quiet output minimum dynamic V_{OL}	V_{OLV} $\lvert V_{OLV} \rvert$	The minimum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.

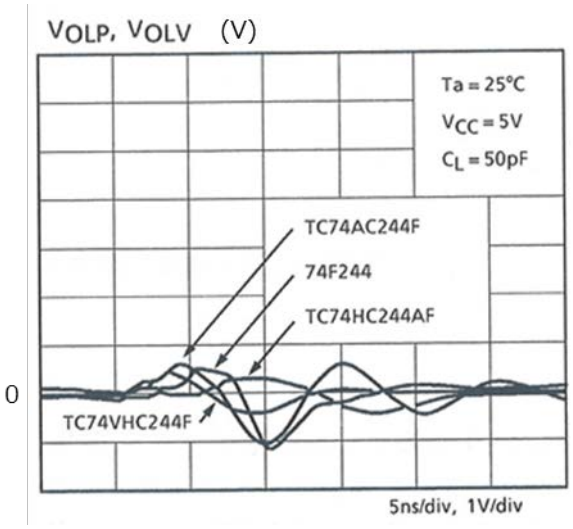


Figure 1.3 Quiet Output Noise Waveforms

Figure 1.4 shows the switching waveforms. Overshoot and undershoot of the TC74VHC00F are smaller than those of the TC74AC00F, and response of the TCH74VHC00F is faster than that of the TC74HC00AF.

● Overshoot / Undershoot (TC74VHC244)‥‥‥ 0.5 V Typ. (@5 V, C_L=50 pF)

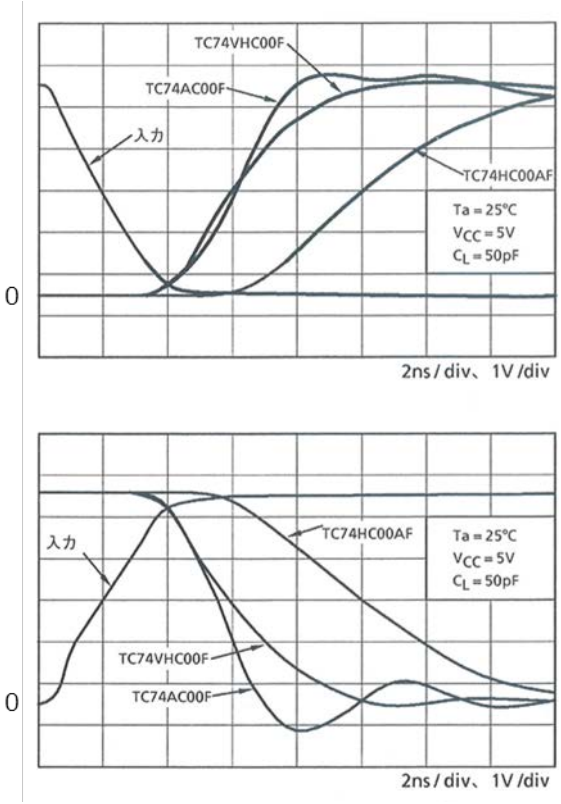


Figure 1.4 Switching Waveforms

1.2.3. Interface Capability

The VHC/VHCT/VHC9/VHCV series adopts an input protection circuit with no diode from input terminal to power supply side. The circuit realizes an input tolerant function and power-down protection, and ensures the voltage of input terminal up to 5.5 V even if the power supply voltage is lower than 5.5 V. (Except for I/O terminals of the VHC 245)

In addition, the VHCT/VHCV series adopts an output circuit with no parasitic diode from output terminal to power supply side. The circuit realizes an output tolerant function and power-down protection, and ensures the voltage of output terminal up to 5.5 V even if the output terminal high-impedance state or the power supply voltage is not applied.

This I/O power-down protection system makes it possible to use VHC series devices on “dual supply systems" or "power management circuits".

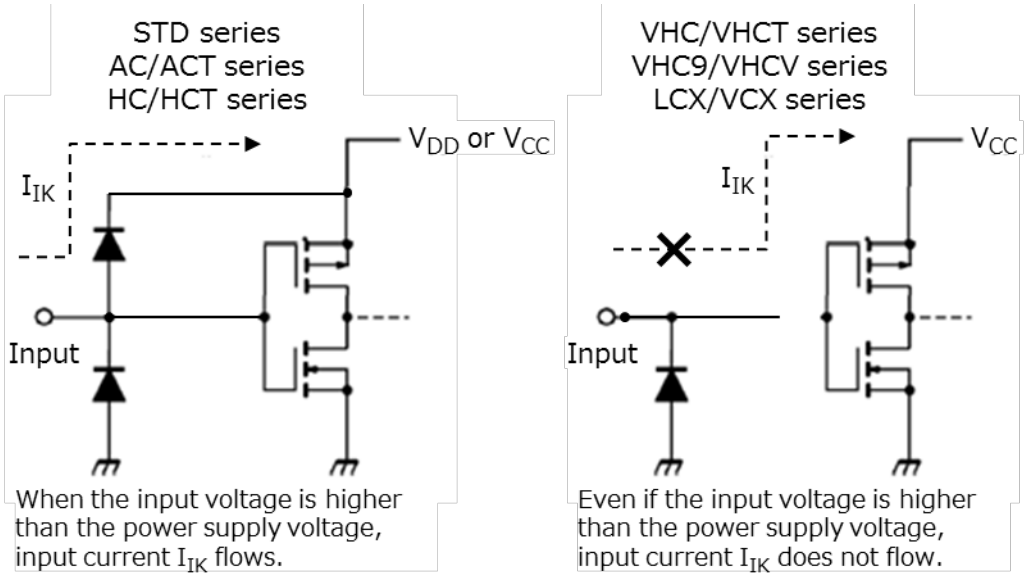


Figure 1.5 Input Equivalent Circuit for Each Series

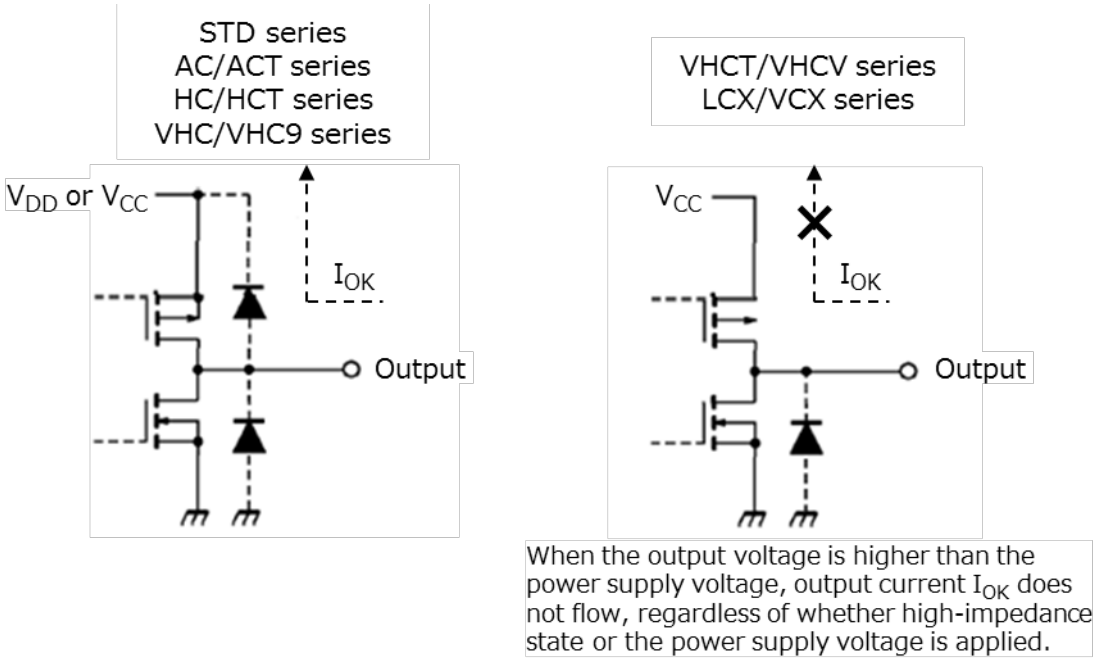


Figure 1.6 Output Equivalent Circuit for Each Series

Table 1.3 Voltage Applicable to I/O Terminals

	VHC	VHCT	VHC9	VHCV
Input Voltage Range				
(Operation)	0 to 5.5 V	0 to 5.5 V	0 to 5.5 V	0 to 5.5 V
(Power Down)	0 to 5.5 V	0 to 5.5 V	0 to 5.5 V	0 to 5.5 V
Output Voltage Range				
(Output Enable)	0 to V_{CC}	0 to V_{CC}	0 to V_{CC}	0 to V_{CC}
(Output Disable)	0 to V_{CC}	0 to 5.5 V	0 to V_{CC}	0 to 5.5 V
(Power Down)	0 (Note 1)	0 to 5.5 V	0 (Note 1)	0 to 5.5 V

Note 1: Voltage cannot be applied.

Table 1.4 Definition of Parameters

Parameter	Definition
Input tolerant function	A function designed to prevent a current from flowing from an input to the power supply when the input voltage is higher than the power supply voltage or when V_{CC} = 0 V.
Output tolerant function	A function designed to prevent a current from flowing from an output to the power supply when the output is in the high-impedance state or when V_{CC} = 0 V.
Power-down protection	A function designed to prevent a current from flowing to the power supply terminal even if a voltage is applied to the input and output terminals when V_{CC} = 0 V.

1.2.4. Output Current

Each of the VHC/VHCT/VHC9/VHCV series has two kinds of output current.

Please refer to Table 1.5.

Table 1.5 Output Current Per Series

	VHC	VHCT	VHC9	VHCV
Output Current (V_{CC} = 4.5 V)	±8 mA	±8 mA	±8 mA	±16 mA
(V_{CC} = 3 V)	±4 mA	±4 mA	±4 mA	±8 mA

2. Method of Designating CMOS Logic ICs

2.1. Part Naming Conventions

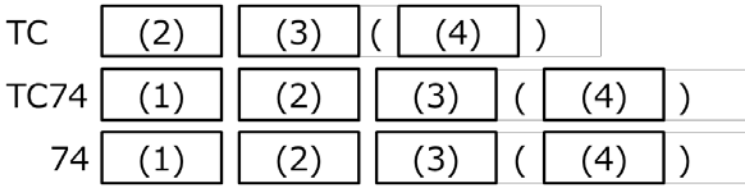


Figure 2.1 Part Naming Conventions

(1) Series, (2) Function, (3) Package, (4) Packing Method

(Example) TC74VCX08FT(EL)

(1) VCX Series, (2) 08 Function, (3) Plastic TSSOP Package, (4) Embossed tape and reel

(1) Series Definition

Table 2.1 shows each series and the input level.

Table 2.1 Series Definition

Series	Definition
Blank	STD series
HC	CMOS level input of HC series
HCT	TTL level input of HC series
AC	CMOS level input of AC series
ACT	TTL level input of AC series
VHC	CMOS level input of VHC series
VHCT	TTL level input of VHC series
VHC9	Schmitt circuit-type input of VHC series
VHCV	Schmitt circuit-type input of VHC series Capable of handling twice as much output current as other products in VHC series.
LCX	TTL level input of LCX series
VCX	TTL level input of VCX series

(2) Function

The function number is represented by 2 to 8 alphanumeric characters.

Function numbers are common for all series.

(3) Package Type

Package classification is common for all series.

P・・・	Dual in-line package (DIP)	14/16/20 pin
F・・・	200-mil small-outline package (SOP)	14/16/20 pin
D・・・	150-mil small-outline package (SOIC)	14/16/20 pin
FT・・・	Thin shrink small-outline package (TSSOP)	14/16/20/48 pin
FK・・・	300-mil small-outline package (US)	14/16/20 pin

(4) Packing Method

Please refer to the Toshiba web page. (URL: https://toshiba.semicon-storage.com/ap-en/top.html)

3. Explanation of Ratings and Standards

The tables below show common ratings and electrical characteristics for the VHC/VHCT/VHC9/VHCV series. When the ratings and electrical characteristics are different from those of individual data sheets, the latter take precedence.

For the meanings of the parameters, please refer to the glossary at end of this document.

3.1. Absolute Maximum Ratings

In general, absolute maximum rating values should not be exceeded, in order to guarantee the life and reliability of integrated circuit products.

Absolute maximum ratings should not be exceeded, even for a moment.

When a device is used in excess of any absolute maximum rating, it may not recover, and in many cases, permanent damage will occur.

Table 3.1 shows the common absolute maximum ratings for the VHC/VHCT/VHC9/VHCV series.

Table 3.1 Absolute Maximum Ratings

Characteristics	Symbol	Rating		Unit
Supply voltage range	V_{CC}	-0.5 to 7.0		V
DC input voltage	V_{IN}	-0.5 to 7.0		V
DC output voltage	V_{OUT}	VHC/VHC9 series	-0.5 to V_{CC}+0.5	V
		VHCT/VHCV series	-0.5 to 7.0 (Note 1) -0.5 to V_{CC}+0.5 (Note 2)	
Input diode current	I_{IK}	-20		mA
Output diode current	I_{OK}	VHC/VHC9 series	±20	mA
		VHCT/VHCV series	±20 (Note 3)	
DC output current	I_{OUT}	±25		mA
DC V_{CC}/ground current	I_{CC}	±50 (Note 4) ±75 (Note 4)		mA
Power dissipation	P_D	500 (DIP) (Note 5) 180 (Other)		mW
Storage temperature	T_{stg}	-65 to 150		°C

Note 1: Output in off-state

Note 2: High or Low State. I_{OUT} absolute maximum rating must be observed.

Note 3: V_{OUT} < GND, V_{OUT} > V_{CC}

Note 4: Different by product

Note 5: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

3.2. Operating Ranges

These are the conditions under which the operation of VHC series devices is guaranteed. When any of these values is exceeded, operation is not guaranteed, even if the value is still within the absolute maximum rating in Table 3.1.

Unused input terminals must be connected to either V_{CC} or GND.

Table 3.2 shows the common operating ranges for the VHC/VHCT/VHC9/VHCV series.

Table 3.2 Operating Ranges

Characteristics	Symbol	Rating				Unit
		VHC	VHCT	VHC9	VHCV	
Supply voltage	VCC	2.0 to 5.5	4.5 to 5.5	2.0 to 5.5	1.8 to 5.5	V
Input voltage	VIN	0 to 5.5				V
Output voltage	VOUT	0 to VCC	0 to 5.5 (Note 1) 0 to VCC (Note 2)	0 to VCC	0 to 5.5 (Note 1) 0 to VCC (Note 2)	V
Operating temperature	Topr	-40 to 85 (Note 3) -40 to 125 (Note 3)				°C
Input Rise and Fall Time	dt/dv	0 to 100 (Note 4) 0 to 20 (Note 5)	0 to 20	-	0 to 20 (Note 4) 0 to 1 (Note 5)	ns/V

Note 1: Output in off-state
Note 2: High or Low State
Note 3: Different by product
Note 4: V_{CC} = 3.3 ± 0.3 V
Note 5: V_{CC} = 5 ± 0.5 V

3.3. DC Characteristics

Tables 3.3 to 3.6 show DC characteristics for the VHC/VHCT/VHC9/VHCV series.

3.3.1. VHC Series

Table 3.3 Characteristics (VHC Series)

Characteristics	Sym-bol	Test Condition		Ta = 25 °C				Ta = -40 to 85 °C		Unit
			V_{CC} (V)	Min	Typ.	Max		Min	Max	
High-level input voltage	V_{IH}	-	2.0 3.0 to 5.5	1.50 V_{CC} × 0.7	- -	- -		1.50 V_{CC} × 0.7	- -	V
Low-level input voltage	V_{IL}	-	2.0 3.0 to 5.5	- -	- -	0.50 V_{CC} × 0.3		- -	0.50 V_{CC} × 0.3	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	- - -	1.9 2.9 4.4	- - -	V
			I_{OH} = -4 mA I_{OH} = -8 mA	3.0 4.5	2.58 3.94	- -	- -	2.48 3.80	- -	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0 3.0 4.5	- - -	0.0 0.0 0.0	0.1 0.1 0.1	- - -	0.1 0.1 0.1	
			I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5	- -	- -	0.36 0.36	- -	0.44 0.44	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	-	-	±0.25	-	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	-	-	±0.1	-	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA

3.3.2. VHCT Series

Table 3.4 Characteristics (VHCT Series)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25 °C			Ta = -40 to 85 °C		Unit
					Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	-		4.5 to 5.5	2.0	-	-	2.0	-	V
Low-level input voltage	V_{IL}	-		4.5 to 5.5	-	-	0.8	-	0.8	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH} = -8 mA	4.5	3.94	-	-	3.80	-	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	-	0.0	0.1	-	0.1	
			I_{OL} = 8 mA	4.5	-	-	0.36	-	0.44	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	-	-	±0.25	-	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	-	-	±0.1	-	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	-	-	1.35	-	1.50	mA
Output leakage current	I_{OPD}	V_{OUT} = 5.5 V		0	-	-	0.5	-	5.0	μA

3.3.3. VHC9 Series

Table 3.5 Characteristics (VHC9 Series)

Characteristics	Symbol	Test Condition		Ta = 25 °C				Ta = -40 to 85 °C		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max	
Positive threshold voltage	V_P	-		3.0 4.5 5.5	- - -	- - -	2.20 3.15 3.85	- - -	2.20 3.15 3.85	V
Negative threshold voltage	V_N	-		3.0 4.5 5.5	0.90 1.35 1.65	- - -	- - -	0.90 1.35 1.65	- - -	V
Hysteresis voltage	V_H	-		3.0 4.5 5.5	0.30 0.40 0.50	- - -	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	- - -	1.9 2.9 4.4	- - -	V
			I_{OH} = -4 mA I_{OH} = -8 mA	3.0 4.5	2.58 3.94	- -	- -	2.48 3.80	- -	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0 3.0 4.5	- - -	0.0 0.0 0.0	0.1 0.1 0.1	- - -	0.1 0.1 0.1	
			I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5	- -	- -	0.36 0.36	- -	0.44 0.44	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	-	-	±0.25	-	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	-	-	±0.1	-	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA

3.3.4. VHCV Series

Table 3.6 Characteristics (VHCV Series)

Characteristics	Symbol	Test Condition		Ta = 25 °C				Ta = -40 to 85 °C		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max	
Positive threshold voltage	V_P	-		1.8 2.3 3.0 4.5 5.5	- - - - -	- - - - -	1.65 1.85 2.20 3.15 3.85	- - - - -	1.65 1.85 2.20 3.15 3.85	V
Negative threshold voltage	V_N	-		1.8 2.3 3.0 4.5 5.5	0.15 0.45 0.90 1.35 1.65	- - - - -	- - - - -	0.15 0.45 0.90 1.35 1.65	- - - - -	
Hysteresis voltage	V_H	-		1.8 2.3 3.0 4.5 5.5	0.15 0.20 0.30 0.40 0.50	- - - - -	1.05 1.10 1.20 1.40 1.60	0.15 0.20 0.30 0.40 0.50	1.05 1.10 1.20 1.40 1.60	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	1.8 3.0 4.5	1.7 2.9 4.4	1.8 3.0 4.5	- - -	1.7 2.9 4.4	- - -	V
			I_{OH} = -8 mA I_{OH} = -16 mA	3.0 4.5	2.58 3.94	- -	- -	2.48 3.80	- -	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	1.8 3.0 4.5	- - -	0.0 0.0 0.0	0.1 0.1 0.1	- - -	0.1 0.1 0.1	
			I_{OL} = 8 mA I_{OL} = 16 mA	3.0 4.5	- -	- -	0.36 0.44	- -	0.44 0.55	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 5.5V		1.8 to 5.5	-	-	±0.5	-	±5.0	μA
Power-off leakage current	I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	-	-	0.5	-	5.0	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	-	-	±0.1	-	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	-	-	2.0	-	20.0	μA

3.4. Noise Characteristics

(INPUT $t_r = t_f = 3$ ns)

Table 3.7 Noise Characteristics

Characteristics		Symbol	Test Condition	Ta = 25 °C		Unit
				V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}		V_{OLP}	C_L = 50 pF	5.0	0.5*	0.8*	V
Quiet output minimum dynamic V_{OL}		V_{OLV}	C_L = 50 pF	5.0	-0.5*	-0.8*	V
Minimum high-level dynamic input voltage	VHC	V_{IHD}	C_L = 50 pF	5.0	-	3.5	V
	VHCT			5.0	-	2.0	
Maximum low-level dynamic input voltage	VHC	V_{ILD}	C_L = 50 pF	5.0	-	1.5	V
	VHCT			5.0	-	0.8	

*74VHC244

4. Explanation of Symbols Used in Data sheets

4.1. How to Read a Truth Table

Table 4.1 Definition of Symbols Used in Truth Tables

SYMBOL	DEFINITION
H	High level (indicates stationary input or output)
L	Low level (indicates stationary input or output)
⨍	Indicates leading edge changing from L to H.
⨏	Indicates leading edge changing from H to L.
X	Don't care (either H or L)
Z	High-impedance state
a…h	The level of the parallel inputs A to H (either H or L).
Q0	Level of Q just before input condition indicated in truth table
Qn	Level of Q just before input active edge (⨍ or ⨏)
⎍	One H-level pulse
⎎	One L-level pulse

4.2. AC Characteristics

The AC characteristics of datasheets specify the transient characteristics.

Figure 4.1 shows measuring circuit. Figure 4.2, 4.3 shows I/O switching waveforms.

(Condition of input waveform: The amplitude range is between V_{DD} and V_{SS}, and rise and fall times are 3 ns.)

To ensure normal functioning of the device, the following timings must be adhered to.

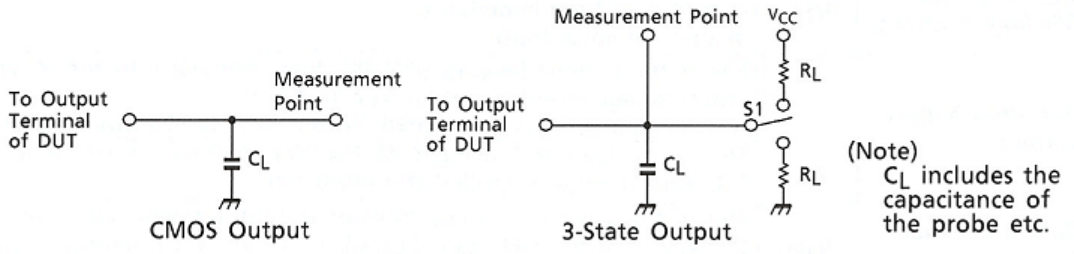
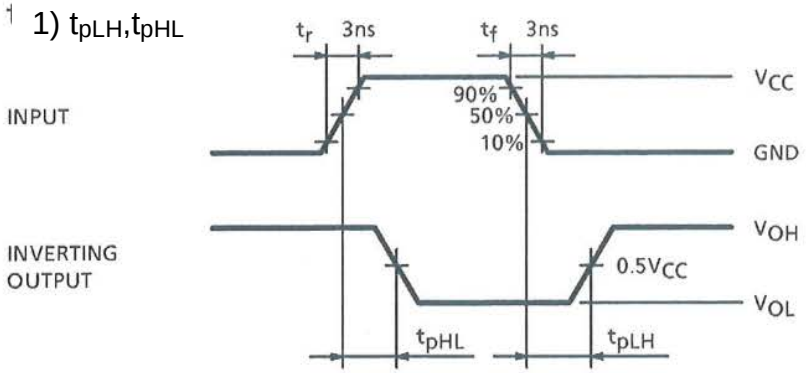


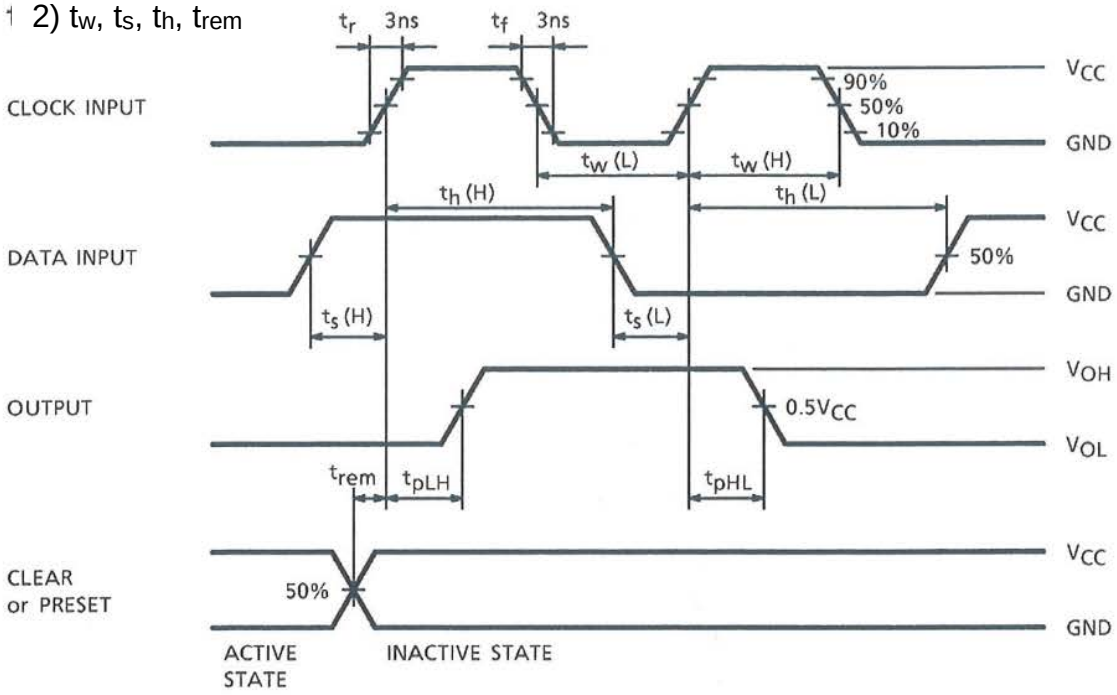
Figure 4.1 Measuring Circuit of Output

4.2.1. I/O Switching Waveform of VHC/VHC9/VHCV Series

1) t_{pLH},t_{pHL}



2) t_w, t_s, t_h, t_{rem}



3) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

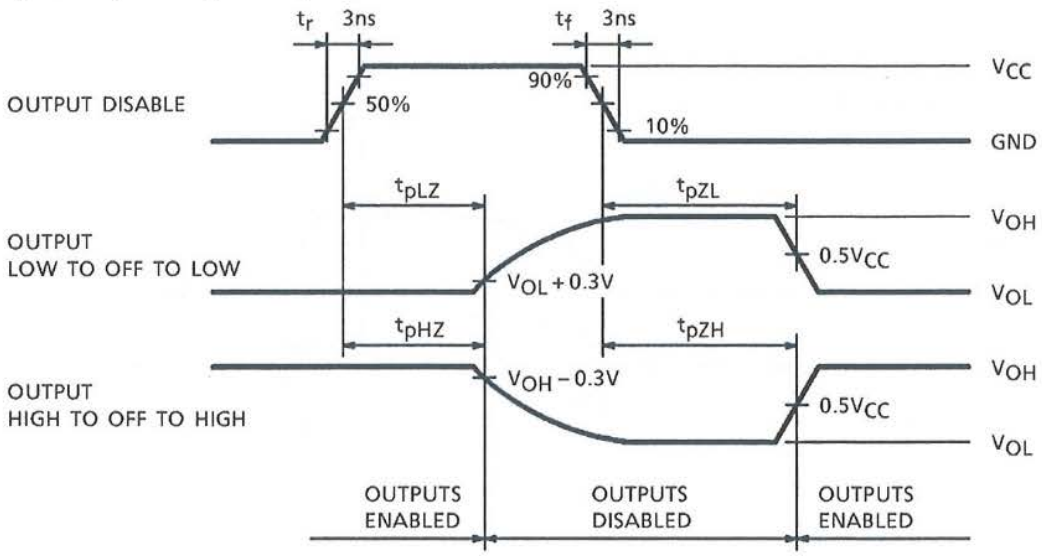
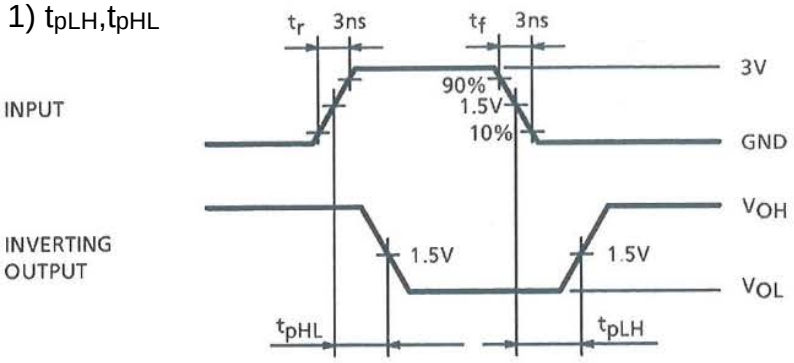


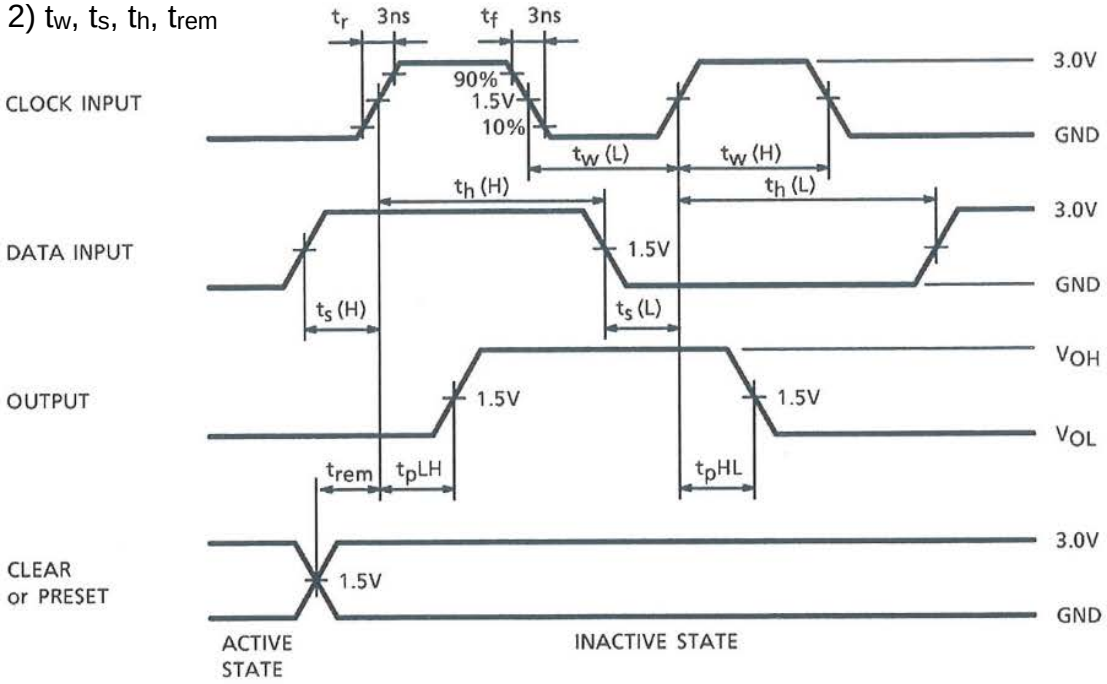
Figure 4.2 I/O Switching Waveform of VHC/VHC9/VHCV Series

4.2.2. I/O Switching Waveform of VHCT Series

1) t_{pLH},t_{pHL}



2) t_w, t_s, t_h, t_{rem}



3) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

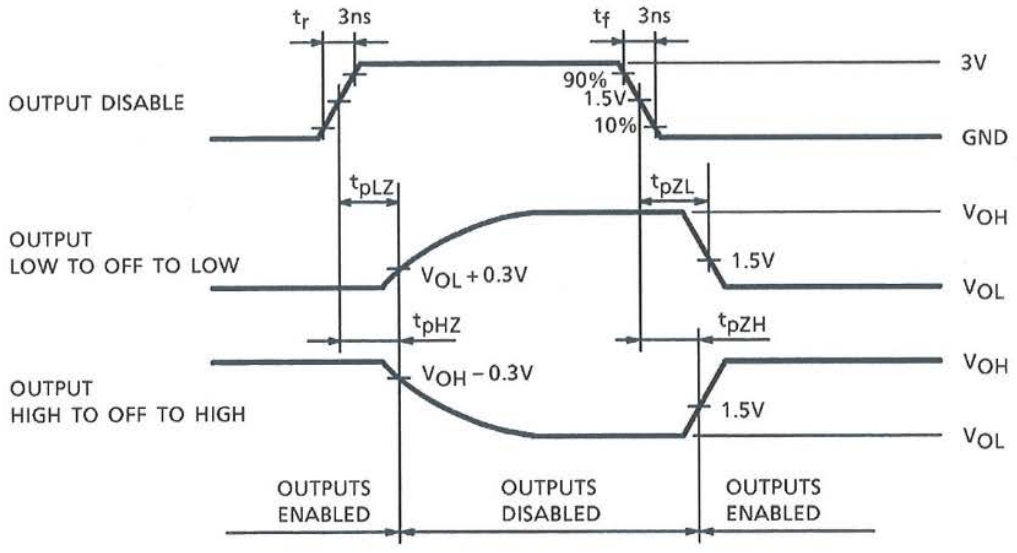


Figure 4.3 I/O Switching Waveform of VHCT Series

4.3. Standardized Test Procedure for Power Dissipation Capacitance

Measurements for all devices are under the conditions of "V_{CC} = 5.0 V" and "Ta = 25 deg C".

And a relatively high frequency, about 1 MHz, is used for measurement of power consumption, because if a device is tested at a high enough frequency, the contribution of the DC supply current to the overall power consumption will be negligible and can be ignored. Devices with 3-state outputs are measured in the enabled state.

In the case of devices that have several circuits in the same package (e.g., the VHC04 hex inverter or the VHC74 dual F/F), only one circuit is measured and the result is shown on the data sheet as the C_{pd} per circuit.

In the case of devices that contain several circuits in the same package operating simultaneously from the same clock signal (e.g., the VHC174 hex D-F/F), the C_{pd} can be obtained by measuring either the C_{pd} of the device with only one output active, or the C_{pd} with all device outputs active.

The pin states for each IC are listed in the table.

C_{PD} Measuring Condition

Table 4.2 C_{PD} Measuring Condition

Type No.		Pin No. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
00		P	H	O	X	X	O	G	O	X	X	O	X	X	V										
02		O	P	L	O	X	X	G	X	X	O	X	X	O	V										
03		P	H	R	X	X	O	G	O	X	X	O	X	X	V										
04		P	O	X	O	X	O	G	O	X	O	X	O	X	V										
05		P	R	X	O	X	O	G	O	X	O	X	O	X	V										
07		P	R	X	O	X	O	G	O	X	O	X	O	X	V										
08		P	H	O	X	X	O	G	O	X	X	O	X	X	V										
14		P	O	X	O	X	O	G	O	X	O	X	O	X	V										
17		P	O	X	O	X	O	G	O	X	O	X	O	X	V										
20		P	H	O	H	H	O	G	O	X	X	O	X	X	V										
21		P	H	O	H	H	O	G	O	X	X	O	X	X	V										
27		P	L	X	X	X	O	G	O	X	X	X	O	L	V										
32		P	L	O	X	X	O	G	O	X	X	O	X	X	V										
74		H	Q	P	H	O	O	G	O	O	X	X	X	X	V										
86		P	L	O	X	X	O	G	O	X	X	O	X	X	V										
123		L	H	P	O	O	O	O	G	X	X	X	O	O	O	R	V								
125		H	P	O	X	X	O	G	O	X	X	O	X	X	V										
126		H	P	O	X	X	O	G	O	X	X	O	X	X	V										
132		P	H	O	X	X	O	G	O	X	X	O	X	X	V										
138		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V								
139		L	P	L	O	O	O	O	G	O	O	O	O	X	X	X	V								
153		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V								
157	1*	P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V								
157	4*	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V								
161		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V								
163		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V								
164		Q	H	O	O	O	O	G	P	H	O	O	O	O	V										
165		H	P	X	X	X	X	O	G	O	Q	X	X	X	X	L	V								
174	1*	H	O	Q	X	O	X	O	G	P	O	X	O	X	X	O	V								
174	6*	H	O	Q	Q	O	Q	O	G	P	O	Q	O	Q	Q	O	V								
221		L	H	P	O	O	O	O	G	X	X	X	O	O	O	R	V								
238		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V								
240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V				
244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V				
245		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
273	1*	H	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V				
273	8*	H	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V				
373	1*	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V				
373	8*	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V				
374	1*	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V				
374	8*	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V				
393		P	L	O	O	O	O	G	O	O	O	O	X	X	V										
540	1*	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
540	8*	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V				
541	1*	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
541	8*	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V				
573	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V				
573	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V				

*: Number of active outputs

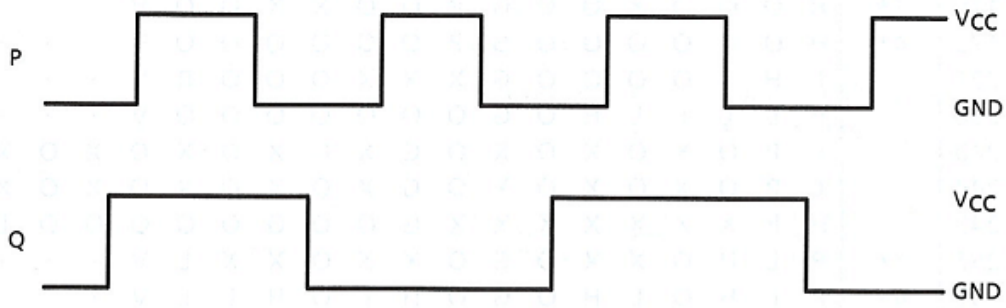
Table 4.3 C_{PD} Measuring Condition (Continued)

Type No.		Pin No. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
574	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V				
574	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V				
595		O	O	O	O	O	O	O	G	O	H	P	P	L	Q	O	V								
4020		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V								
4040		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V								
4051		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V								
4052		O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V								
4053		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V								
4066		O	O	O	O	X	X	G	O	O	O	O	X	P	V										
9125		H	P	X	X	X	X	G	L	O	O	O	O	O	V										
9126		H	P	X	X	X	X	G	L	O	O	O	O	O	V										
9151		P	X	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	O	V				
9152		P	X	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	O	V				
9164		L	H	Q	P	O	O	O	G	O	O	O	O	O	O	O	V								
9273		H	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V				
9541		L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
9595		H	Q	P	P	O	O	O	G	O	O	O	O	O	O	O	V								

*: Number of active outputs

-Explanation of symbols-

V = V_{CC} (+5.0 V)
G = GND (0 V)
H = Logic 1 (V_{CC})
L = Logic 0 (GND)
X = Don't care. V_{CC} or GND (but not switching)
R = 1.0 kΩ pull-up resistor connected between the IC and a 5-V power supply other than V_{CC}.
O = Open
P = 50% duty cycle input pulse (shown below)
Q = 50% duty cycle half-frequency out-of-phase input pulse (shown below)



Input Pulse Waveforms

4.4. Noise Characteristics and Measurement Circuit

Noise characteristics caused by high-speed switching are specified for the VHC series.

Noise is generated by rush current flowing through the internal V_{CC} or GND lines of a device when several outputs are switching simultaneously.

Table 4.4 shows an explanation of noise parameters.

Figures 4.4 and 4.5 show the noise characteristic measurement circuit.

Table 4.4 Definition of Noise Parameters

Parameter	Symbol	Definition
Quiet output maximum dynamic V_{OL}	V_{OLP}	The maximum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.
Quiet output minimum dynamic V_{OL}	V_{OLV} $\|V_{OLV}\|$	The minimum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.
Minimum high-level dynamic input voltage V_{IH}	V_{IHD}	High-level dynamic threshold voltage when all inputs are switching simultaneously
Maximum low-level dynamic input voltage V_{IL}	V_{ILD}	Low-level dynamic threshold voltage when all inputs are switching simultaneously.

Noise Characteristics Measurement Circuit

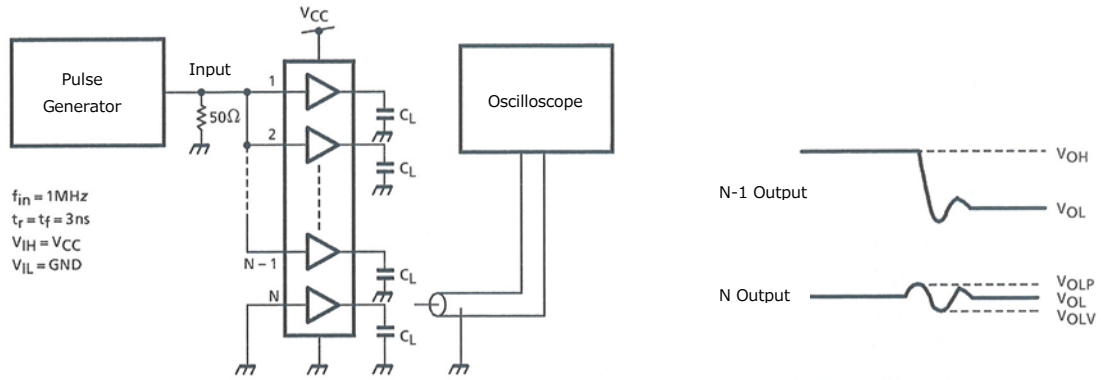


Figure 4.4 Quiet Output Dynamic V_{OLP} and V_{OLV} Measurement Circuit

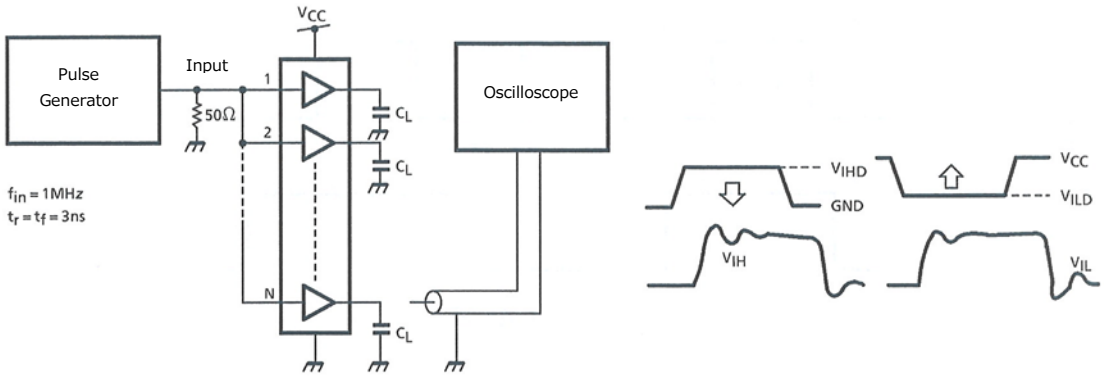


Figure 4.5 Dynamic Input Voltage V_{IHD} and V_{ILD} Measurement Circuit

5. Other Electrical Characteristics

5.1. Power Dissipation

The power dissipation is given by the sum of the quiescent supply current and the dynamic operating current. Therefore, it can be obtained from the following equation:

$P_D = C_{PD} \cdot f_{IN} \cdot V_{CC}^2 + C_L \cdot f_{OUT} \cdot V_{CC}^2 + I_{CC} \cdot V_{CC}$

C_{PD} : Power Dissipation Capacitance

C_L : Load Capacitance

f_{IN} : Input Frequency

f_{OUT} : Output Frequency

In the case of CMOS ICs, if inputs are held at V_{CC} or GND, either the N-ch MOS or the P-ch MOS turns off. As a result, the quiescent supply current from V_{CC} to GND is just a few nA at room temperature.

Therefore, the quiescent supply current increases in direct proportion to the power supply voltage and increases exponentially with the temperature.

The dynamic power dissipation of CMOS ICs is calculated by summing the switching currents and the through currents. The switching currents are due to the charging and discharging of each gate capacitance, when the gate in the circuit that includes the output buffer inverts, and the through currents flow from V_{CC} to GND when the P-ch MOS and the N-ch MOS that constitute the gate turn on briefly at the same time during inversion time.

When the rise and fall times of the input signal are small (a few ns), the through current in the gate is negligible compared with the switching current. Thus, the dynamic supply current is determined by the internal capacitance of the IC and the charging and discharging currents of the load capacitance (C_L).

However, in specific applications such as crystal oscillators, supply current characteristics depend on the through current, and the result calculated using C_{PD} cannot be used.

Figure 5.1 shows the characteristics for power consumption vs. input frequency.

The power consumption of the 74VHC is similar to that of TTL devices operating at high frequency.

However, since the system does not always operate at high frequency, the VHC series can help to reduce the total power consumption of equipment.

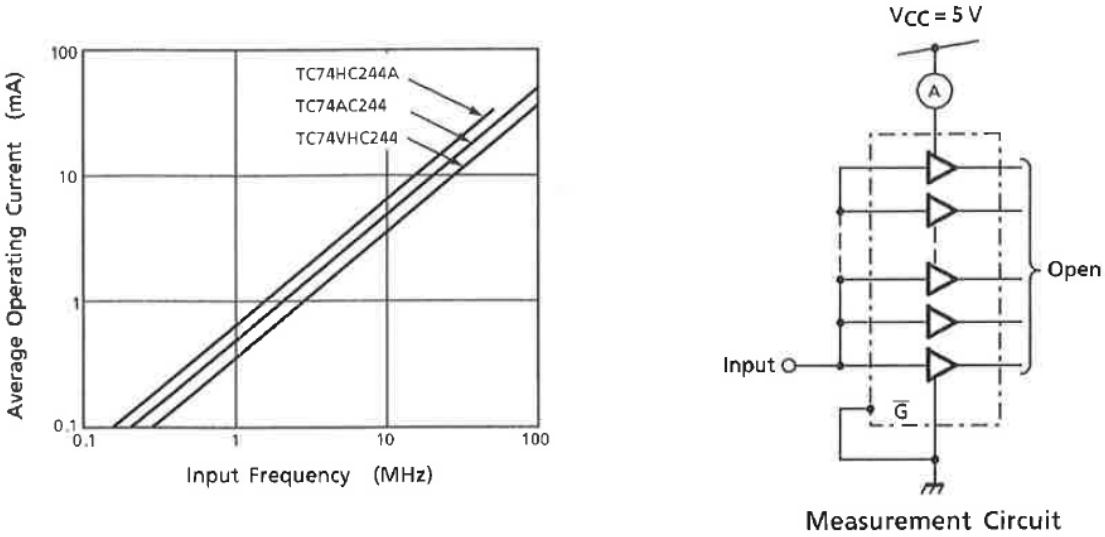


Figure 5.1 Average Operating Current vs. Input Frequency

5.2. Input Characteristics

5.2.1. Simplified Schmitt Input

The VHC/VHCT series adopts the simplified Schmitt input, except for the VHC14 (Schmitt trigger inverter) and the VHC132 (Schmitt trigger NAND).

This improves the dynamic V_{IH}, V_{IL} and slow clock input characteristics.

The hysteresis voltages are 0.15 V (Typ.) for the VHC/VHCT series.

5.3. Output Current Characteristics

± 8 mA drive current of both I_{OH} and I_{OL} is guaranteed for the VHC/VHCT series.

Figure 5.2 (VHC/VHCT series at V_{CC} = 4.5 V) and Figure 5.3 (VHC series at V_{CC} = 3 V) show output current vs. output voltage.

The dotted lines represent the minimum output current characteristics. In the design, please refer to the dotted line.

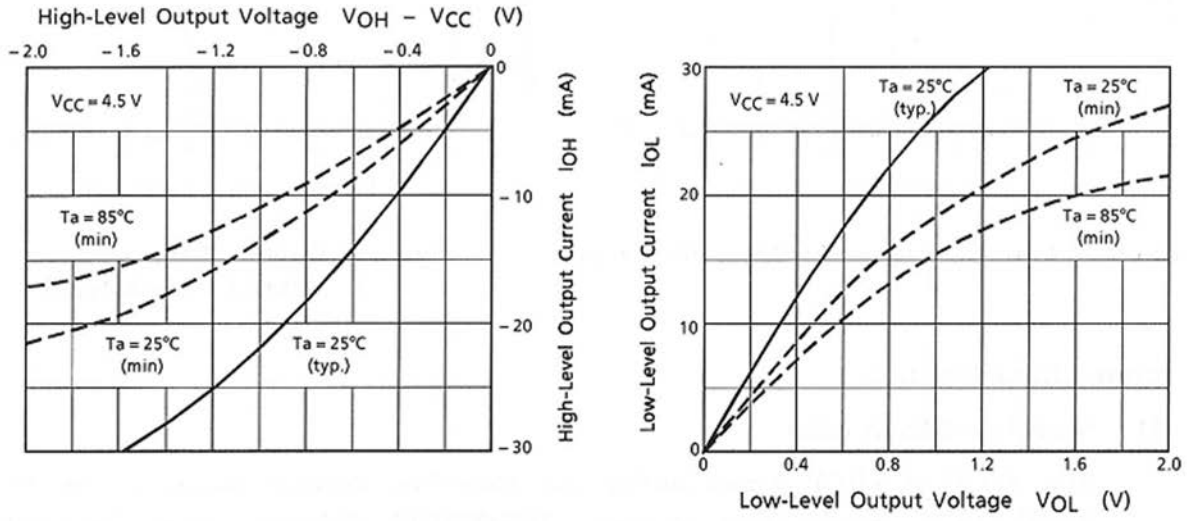


Figure 5.2 Output Current Characteristics V_{CC} = 4.5 V (VHC/VHCT Series)

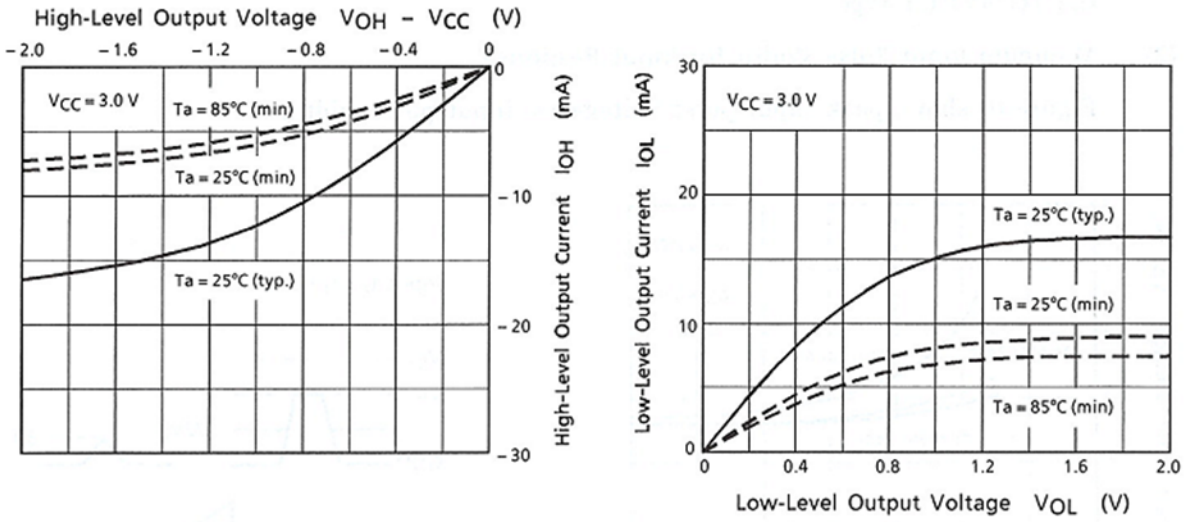


Figure 5.3 Output Current Characteristics V_{CC} = 3.0 V (VHC Series)

Figures 5.4 and 5.5 show the characteristic supply voltage vs. output current (Typ.).
At low voltage, variation in output current becomes larger, so be careful.

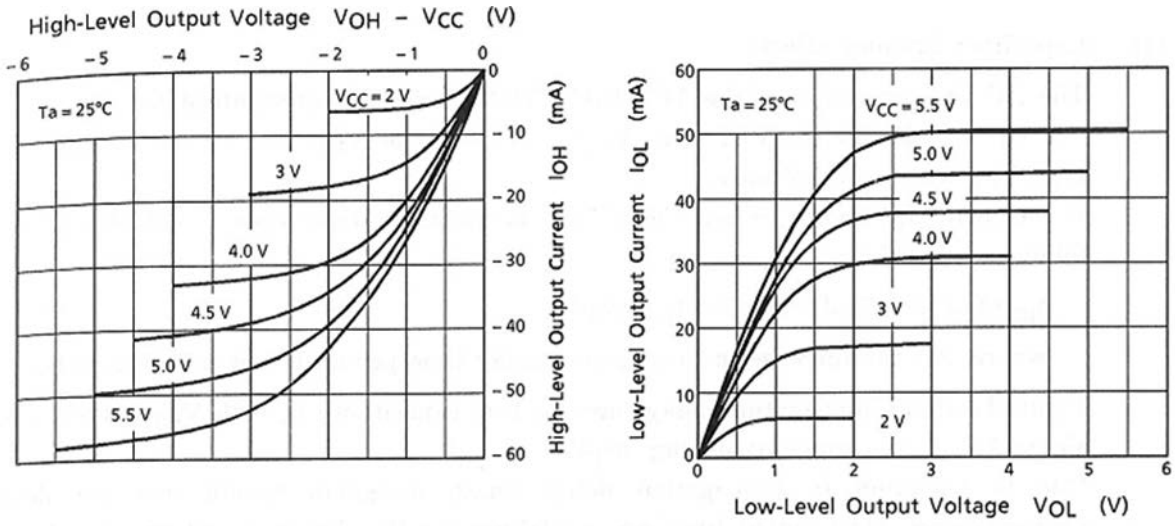


Figure 5.4 Output Current Characteristics (VHC Series)

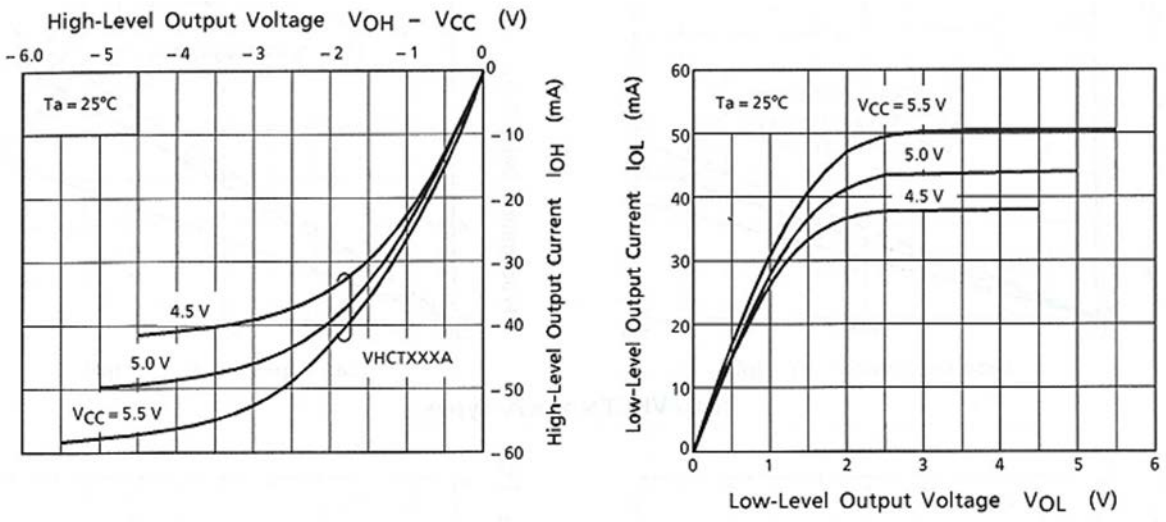


Figure 5.5 Output Current Characteristics (VHCT Series)

5.4. AC Electrical Characteristics

5.4.1. Capacitive Loading Effects

The AC characteristics of the VHC/VHCT series are guaranteed for both C_L = 15 pF and C_L = 50 pF. For the VHC series V_{CC} = 5 V ± 0.5 V or V_{CC} = 3.3 V ± 0.3 V. For the VHCT series V_{CC} = 5.0 V ± 0.5 V only.

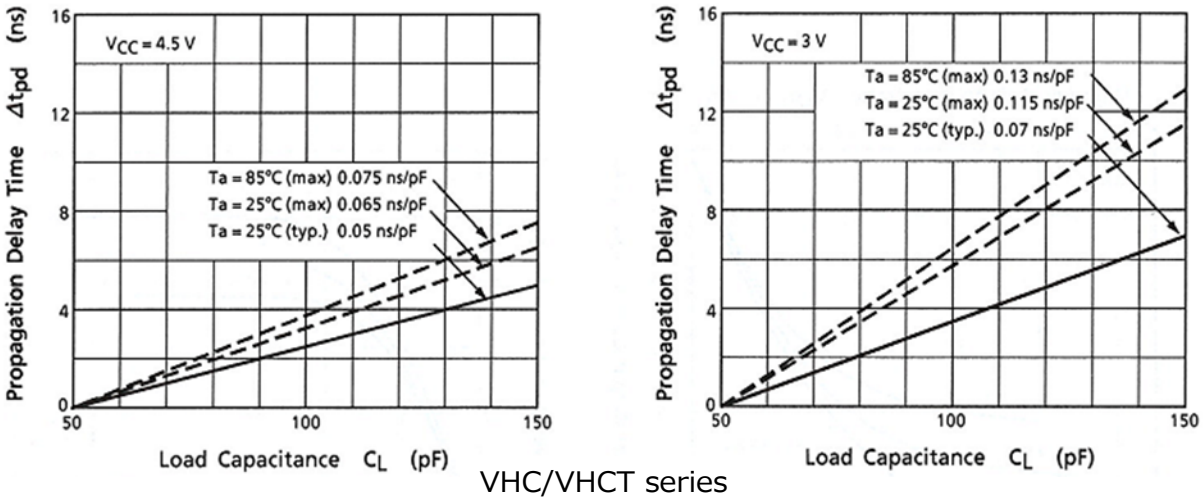
If the load capacitance exceeds 50 pF, the propagation delay time is calculated using the following equation:

$$t_{pd}\,(XpF) = A\,(X\text{ pF} - 50\text{ pF}) + t_{pd}\,(50\text{ pF})$$

where: A = the increase in propagation delay time per unit load capacitance (ns/pF)

Figure 5.6 shows propagation delay time vs. load capacitance at both V_{CC} = 4.5 V and V_{CC} = 3 V, in the range exceeding 50 pF.

Due to variation in propagation delay times, designers should use the dotted-line characteristics. (The dotted lines are guidelines for the designer and are not guaranteed values.)



VHC/VHCT series

Figure 5.6 Propagation Delay Time vs. Load Capacitance

Figure 5.7 shows typical relative propagation delay time values for each power supply voltage when the propagation delay time at V_{CC} = 4.5 V is normalized to 1.

Figure 5.8 shows typical relative transition time values.

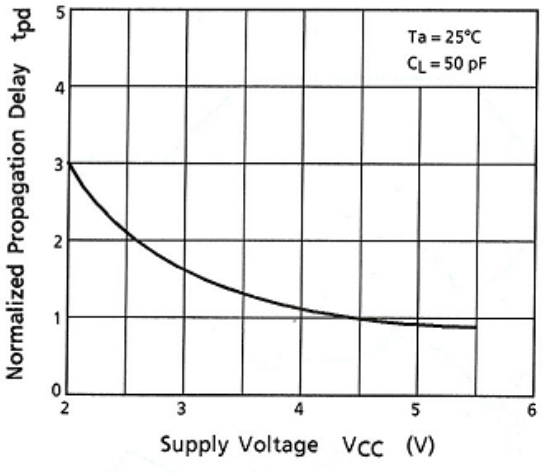


Figure 5.7 Normalized Propagation Delay vs. Supply Voltage (Typ.)

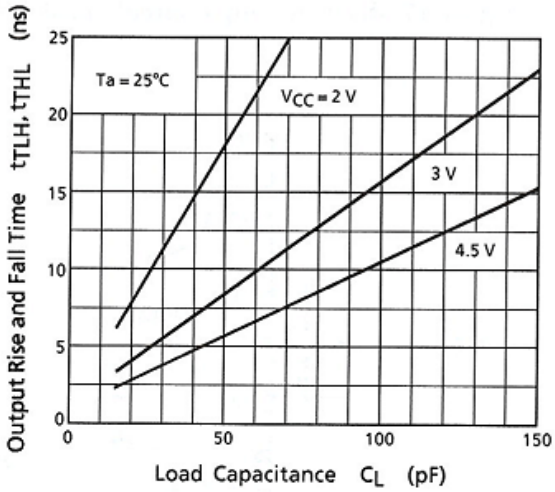


Figure 5.8 Output Transition Time vs. Load Capacitance (Typ.)

5.4.2. Output Skew Characteristics

Output skew (t_{osLH}, t_{osHL}) is specified for all 8-bit products of the VHC/VHCT series.

The design of the IC guarantees an output skew value of 1.0 ns at V_{CC} = 5 ± 0.5 V and of 1.5 ns at V_{CC} = 3.3 ± 0.3 V.

Table 5.1 shows typical values for representative products.

Table 5.1 t_{osLH}, t_{osHL} Test Result

Ta=25 °C, V_{CC}=5 V, C_L=50 pF

	t_{osLH}	t_{osHL}	UNIT
TC74VHC244	0.3	0.2	ns
TC74VHC245	0.3	0.2	
TC74VHC541	0.2	0.2	
TC74VHC373	0.4	0.4	

5.5. Noise Characteristics

Noise characteristics caused by high-speed switching are specified for the VHC/VHCT series. These noises are generated by rush current flowing through the internal VCC or GND lines of the devices when several outputs are switching simultaneously.

Figure 5.9 shows a simple circuit model for a device driving a standard test load.

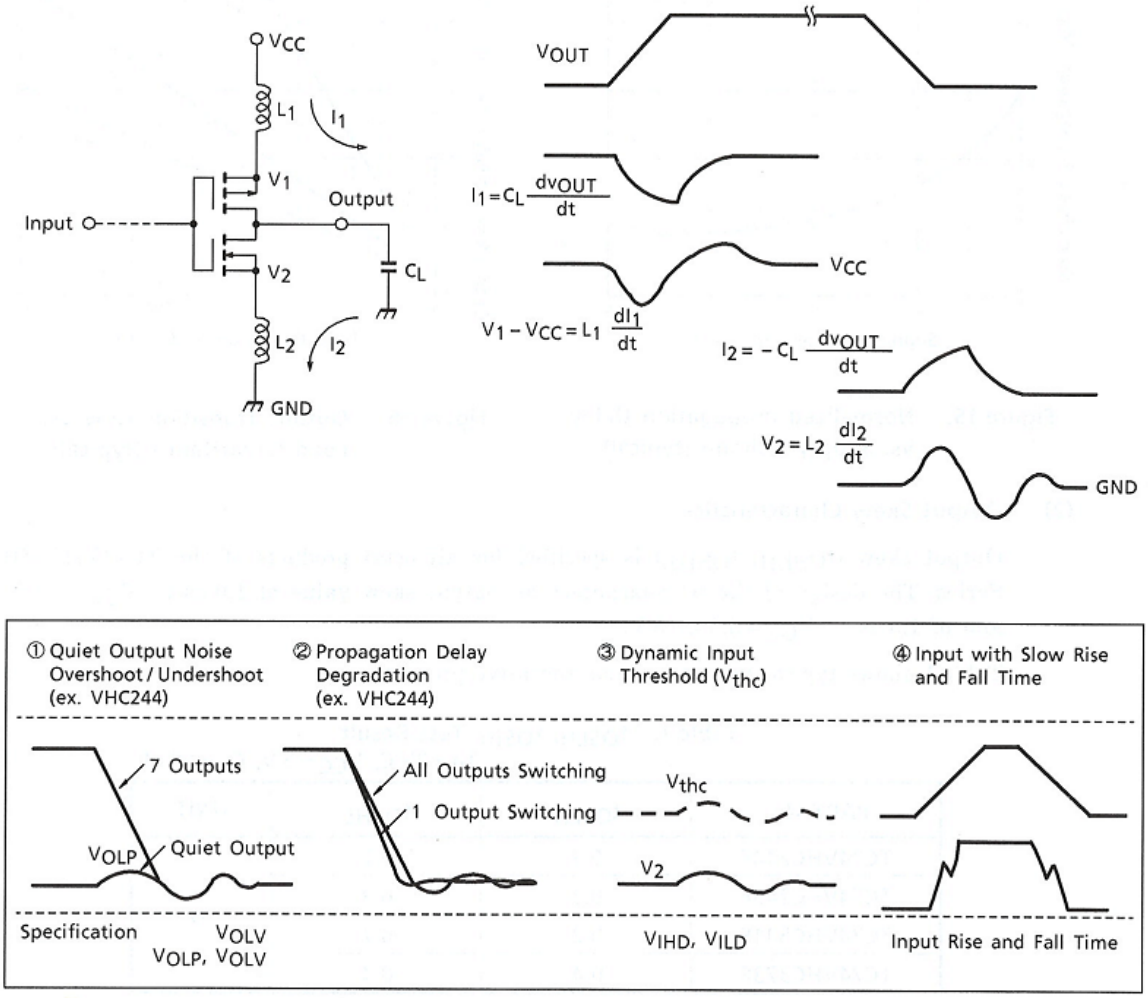
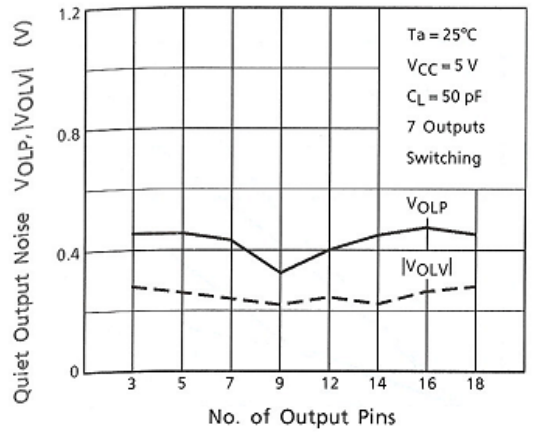


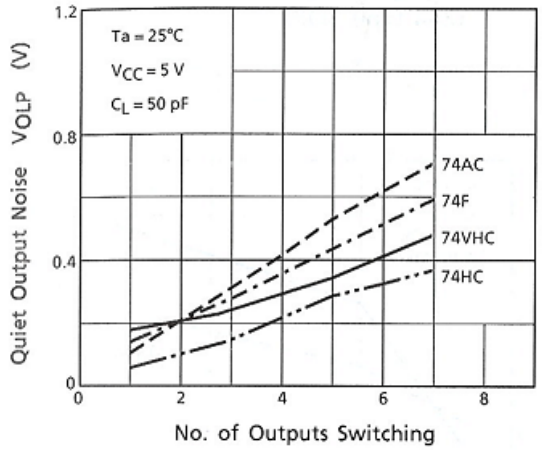
Figure 5.9 Simple Circuit Model for a Device Driving a Standard Test Load

5.5.1. Quiet Output Noise V_{OLP}, V_{OLV}

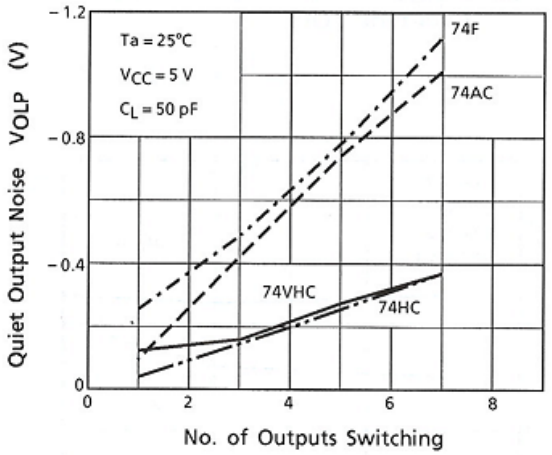
Figure 5.10 shows quiet output noise.



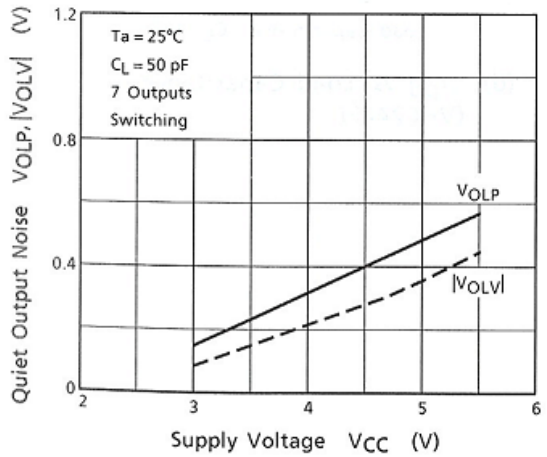
(a) V_{OLP}, V_{OLV} vs. Pin Location (Typ.) (VHC244F)



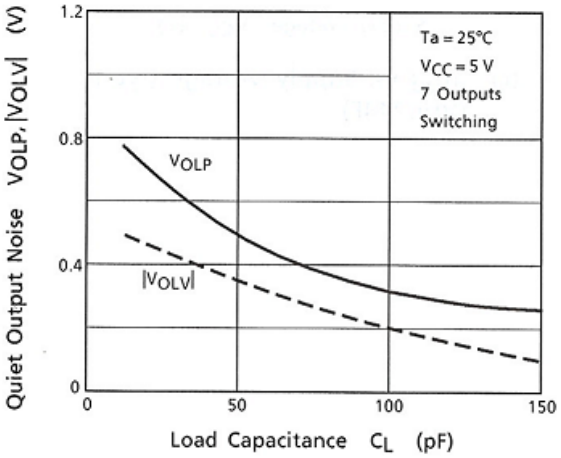
(b) V_{OLP} Series Comparison (Typ.) (244-type SOP)



(c) V_{OLV} Series Comparison (Typ.) (244-type SOP)



(d) V_{OLP}, V_{OLV} vs. Supply Voltage (Typ.) (VHC244F)

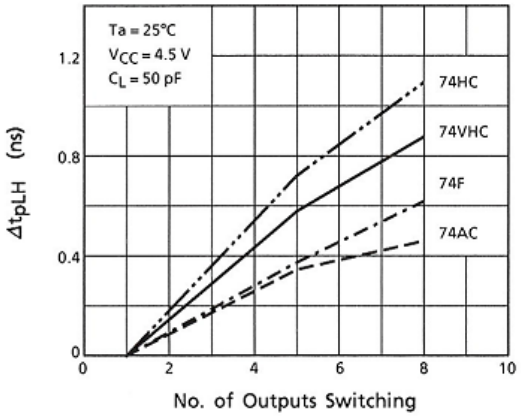


(e) V_{OLP}, V_{OLV} vs. Load Capacitance (Typ.) (VHC244F)

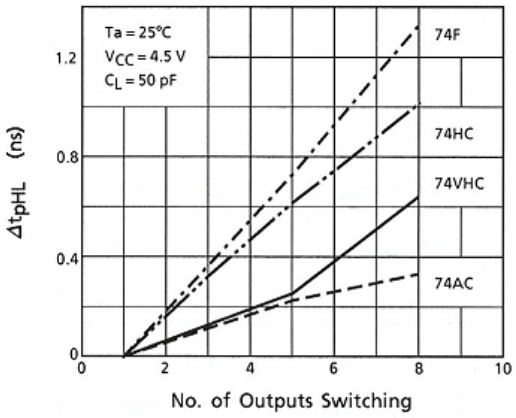
Figure 5.10 Quiet Output Noise V_{OLP}, V_{OLV}

5.5.2. Propagation Delay Degradation (Simultaneous Switching)

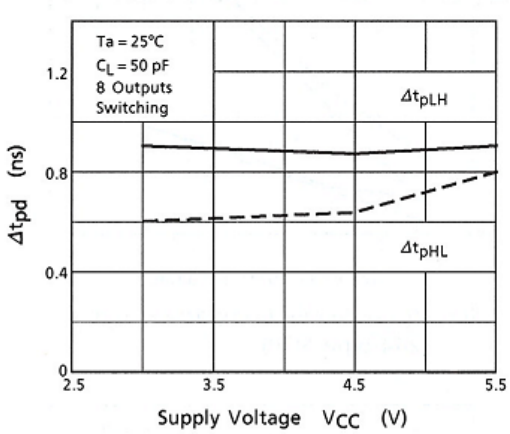
Figure 5.11 shows propagation delay degradation (simultaneous switching).



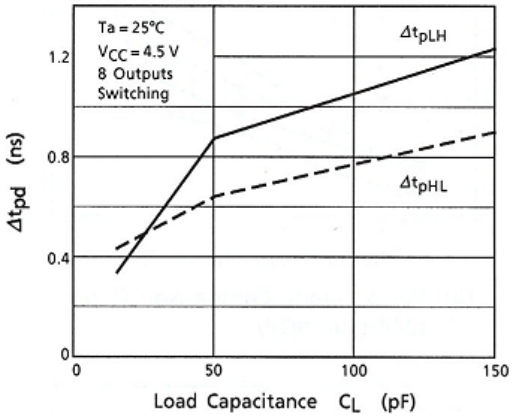
(a) Δt_{pLH} Series Comparison (Typ.) (244-type SOP)



(b) Δt_{pHL} Series Comparison (Typ.) (244-type SOP)



(c) Δt_{pd} vs. Supply Voltage (Typ.) (VHC244F)



(d) Δt_{pd} vs. Load Capacitance (Typ.) (VHC244F)

Figure 5.11 Propagation Delay Degradation (Simultaneous Switching)

6. Glossary of CMOS Logic IC Terms

6.1. Absolute Maximum Ratings

Parameter	Symbol	Definition
Supply voltage	V_{DD} - V_{SS} V_{CC}	The rated voltage of the power supply terminal at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Supply voltage	V_{DD} - V_{EE} V_{CC} - V_{EE}	The rated voltage across the V_{CC}, V_{DD} and V_{EE} terminals at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Input voltage	V_{IN}	The rated voltage of the input terminal at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Output voltage	V_{OUT}	The rated voltage of the output terminal at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Switch I/O voltage	$V_{I/O}$	The rated voltage across the input and output terminals at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Input diode current	I_{IK}	The rated current of the input terminal at which an IC will not suffer breakdown due to latch-up.
Output diode current	I_{OK}	The rated current of the output terminal at which an IC will not suffer breakdown due to latch-up.
Output current	I_{OUT}	The rated current that can flow through one output terminal.
Switch through current	I_T	The rated current between the input and output terminals of a switch at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
V_{CC}/ground current	I_{CC} I_{CC} / I_{GND}	The rated current between the power supply and ground terminals at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability. As V_{CC} / ground current includes output current, substantial V_{CC} / ground current can flow in an IC having multiple output terminals.
Power dissipation	P_D	Power consumption that does not cause IC breakdown over the entire operating temperature range.
Storage temperature	T_{stg}	The ambient temperature range over which no deterioration of characteristics or reliability occurs when an IC is stored for a long period of time or is transported with no supply voltage present.

6.2. Operating Ranges

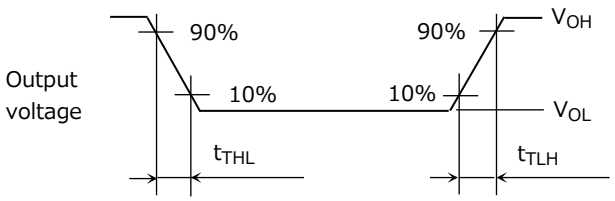
Parameter	Symbol	Definition
Supply voltage	V_{DD} V_{CC} V_{EE} $V_{DD} - V_{EE}$ V_{CC} - V_{EE}	The supply voltage range over which the normal operation of an IC is guaranteed.
Input voltage	V_{IN}	The input voltage range over which the normal operation and electrical characteristics of an IC are guaranteed.
Output voltage	V_{OUT}	The output voltage range over which the normal operation and electrical characteristics of an IC are guaranteed.
Switch I/O voltage	V_S $V_{I/O}$	The switch I/O voltage range over which the normal operation and electrical characteristics of an IC are guaranteed.
Output current	I_{OUT} I_{OH} , I_{OL} I_{OL}	The maximum output current at which the normal operation and electrical characteristics of an IC are guaranteed.
Input rise and fall times	t_r,t_f dt/dv	The ranges of rise and fall times of an input signal that will not cause malfunction due to oscillation of the output.
External capacitor	C_X	The external capacitance range over which the normal operation and electrical characteristics of a multivibrator IC are guaranteed.
External resistor	R_X	The external resistance range over which the normal operation and electrical characteristics of a multivibrator IC are guaranteed.
Operating temperature	T_{opr}	The operating temperature range over which the normal operation and electrical characteristics of an IC are guaranteed.

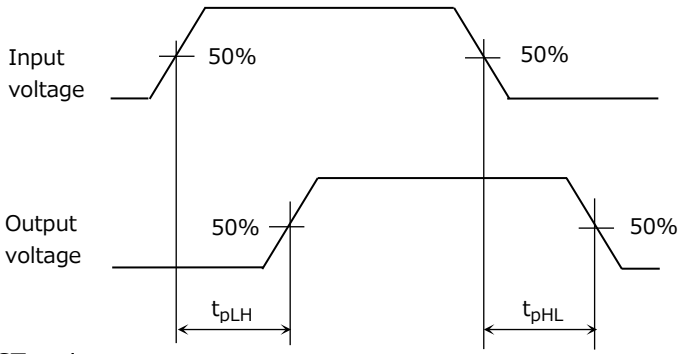
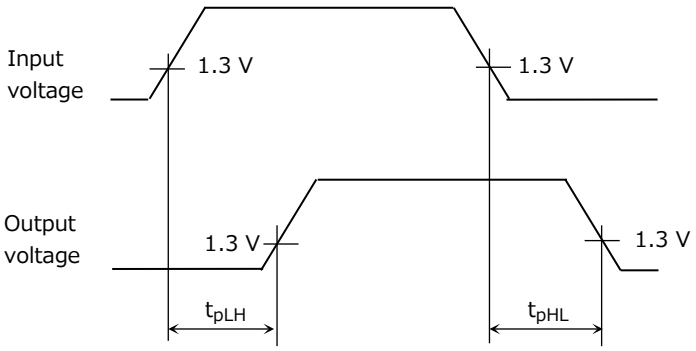
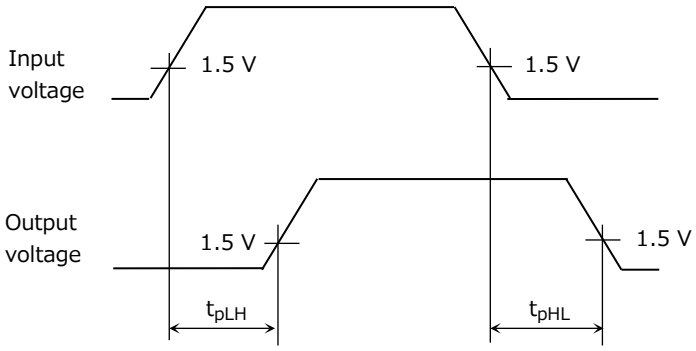
6.3. Electrical Characteristics

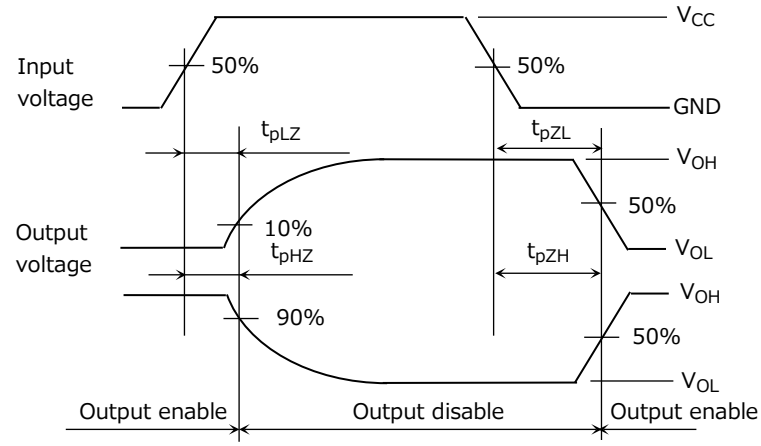
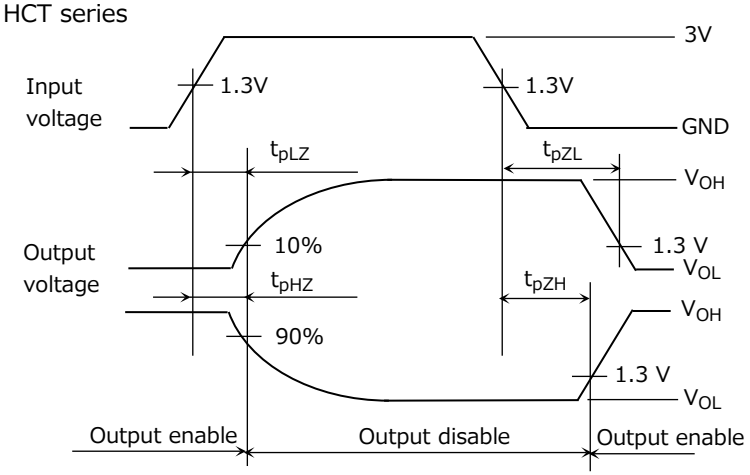
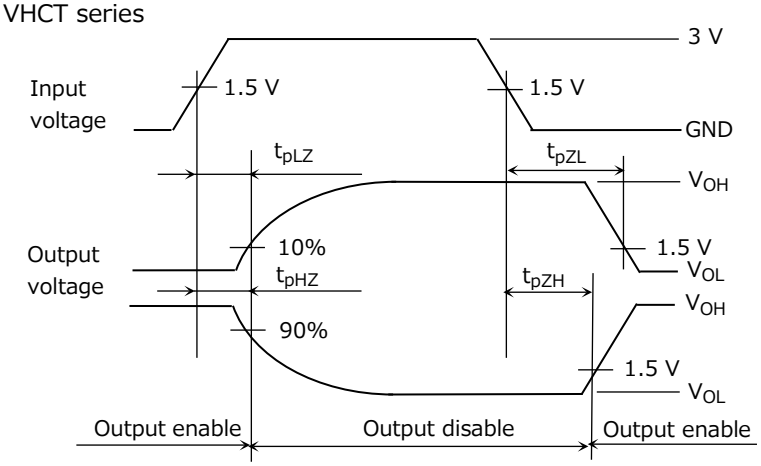
＊電気的特性は測定条件下において規定されます。

Parameter	Symbol	Definition
High-level input voltage	V_{IH}	The input voltage at which input of an IC is driven to the High level.
Low-level input voltage	V_{IL}	The input voltage at which the input of an IC is driven to the Low level.
Positive threshold voltage	V_P	The input threshold voltage at which a Schmitt-trigger input is driven to the High level.
Negative threshold voltage	V_N	The input threshold voltage at which a Schmitt-trigger input is driven to the Low level.
Hysteresis voltage	V_H	The difference between the positive and negative threshold voltages of a Schmitt-trigger input.
High-level output voltage	V_{OH}	The voltage that appears at the output when either VIH or VIL is applied to each input terminal such that the output is set to the High level.
Low-level output voltage	V_{OL}	The voltage that appears at the output when either VIH or VIL is applied to each input terminal such that the output is set to the Low level.
Power-off leakage current	I_{OFF}	The leakage current that flows into an IC via input and output terminals when the power supply is off.
Input leakage current	I_{IN}	The leakage current that flows through the input terminal when a voltage is present at the input terminal of an IC.
Output off-state leakage current	I_{OZ}	The leakage current of an IC with an open-drain output that flows through the output terminal when it is in the high-impedance state.
Output leakage current (Power-off)	I_{OPD}	The leakage current that flows into an IC via the output terminals when V_{CC} is in the off state (V_{CC} = 0 V)
3-state output off-state leakage current	I_{OZ}	The leakage current of an IC with an open-drain or three-state output that flows through the output terminal when it is in the high-impedance state.

Parameter	Symbol	Definition
Input/output leakage current (Switch off)	I_{OFF}	The leakage current that flows through an IC from the input terminals to the output terminal when the power supply is off.
Input/output leakage current (Switch on)	$I_{I/O}$	The leakage current that flows from the input terminal to the output terminal in the switch-on and open-output states.
Control input leakage current	I_{IN}	The leakage current that flows through the control input terminal of an IC when a voltage is applied to the terminal.
RX/CX terminal off-state current	I_{IN}	The current that flows through the RX/CX terminal of a multivibrator IC when a voltage is applied to the terminal.
T2 terminal input leakage current	I_{IN}	The current that flows through the T2 terminal of a multivibrator IC when a voltage is applied to the terminal.
Quiescent supply current	I_{CC}	The current that flows into an IC via the V_{CC} terminal when the V_{CC} or ground level is held constant without changing the input voltage.
	ΔI_{CC}	The current that flows into an IC via the V_{CC} terminal when V_{CC} - 0.6 V is applied to one input terminal.
	I_{CCT}	The current that flows into an IC with TTL-level input via the V_{CC} terminal when a TTL-level voltage is applied to one input terminal.
Active-state supply current (per circuit)	$I_{CC(opr)}$	The average current that flows in the no-load condition between the power supply and ground terminals due to an internal circuit operation.
On-resistance	R_{ON}	The resistance between the input and the output of an analog switch, multiplexer or demultiplexer IC in the switch-on state.
Difference of on-resistance between switches	ΔR_{ON}	The difference in on-resistance between different input-output pairs of an analog switch, multiplexer or demultiplexer IC.

Parameter	Symbol	Definition
Minimum pulse width	$t_{w(H)}$ $t_{w(L)}$	The minimum pulse width that is accepted at a clock input, etc. as a normal pulse.
Minimum setup time	t_S	The time interval during which data must be stable before the associated input (e.g., clock) changes. For example, when data is latched on the rising edge of a clock pulse, it is necessary to apply data at least t_S before the rising edge of the clock.
Minimum hold time	t_h	The time interval during which data must be stable after the active transition of the associated input (e.g., clock).
Minimum removal time	t_{rem}	The minimum time between the release of an asynchronous input (e.g., Clear, Preset) and the application of the next input (e.g., clock).
Minimum retrigger time	t_{rr}	The minimum time necessary for a multivibrator IC to accept the next trigger signal after having received one.
Output transition time	t_{TLH} t_{THL}	The rise and fall times of the output voltage. t_{TLH} is the time from 10% to 90% when the output transitions from Low to High, and t_{THL} is the time from 90% to 10% when the output transitions from High to Low. 

Parameter	Symbol	Definition
Propagation delay time	t_{pLH} t_{pHL}	The delay time between the application of an input signal and an output response. t_{pLH} is defined as the time required for an output to transition from Low to High, and t_{pHL} is defined as the time required for an output to transition from High to Low. HC/VHC series  HCT series  VHCT series 

Parameter	Symbol	Definition
Output enable time Output disable time	t_{pLZ} t_{pHZ} t_{pZL} t_{pZH}	The output enable time is defined as the delay time required for a three-state terminal to be driven High or Low after the output control terminal is set to an inactive level. The output disable time is defined as the delay time required for an output terminal to assume the high-impedance state after the output control signal is set to an active level. HC/VHC series  HCT series  VHCT series 

Parameter	Symbol	Definition
Propagation delay time	Δt_{PD}	For counter ICs, the delay time defined for an IC from when the Qn output is inverted to when the next output (Qn+1) is inverted.
Output pulse width	t_{wOUT}	For multivibrator ICs, the width of the output pulse generated when a prescribed external component is connected and a prescribed voltage is applied.
Output pulse width error between circuits (in the same package)	Δt_{wOUT}	For multivibrator ICs, a difference in output pulse width between two circuits in the same package.
Output skew	t_{osLH} t_{osHL} t_{osZL}	Differences in propagation delay time among output terminals when some outputs in the same package change from the Low level to the High level, from the High level to the Low level, or from the high-impedance state to the Low level.
Phase difference between input and output	$\varphi_{I/O}$	For analog switch, multiplexer and demultiplexer ICs, the delay time from the input to the output when a signal is applied to the input in the switch-on state.
Clock frequency	f	The clock frequency at which an IC operates.
Maximum clock frequency	f_{MAX}	The maximum clock frequency at which the IC operates normally.
Maximum frequency response Phase difference between input and output	$f_{MAX(I/O)}$ f_{MAX}	For analog switch, multiplexer and demultiplexer ICs, the maximum input frequency that the signal can transmit to the output in the switch-on state.
Input capacitance	C_{IN}	The capacitance between the input and ground terminals.
Control input capacitance	C_{IN}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the control input and ground terminals.
Common terminal capacitance	C_{IS}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the common and ground terminals in the off state.
Switch terminal capacitance	C_{OS}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the switch and ground terminals in the off state.

Parameter	Symbol	Definition
Feedthrough capacitance	C_{IOS}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the switch and common terminals in the off state.
Bus I/O capacitance	$C_{I/O}$	The capacitance between the bus and ground terminals.
Power dissipation capacitance	C_{PD}	The equivalent internal capacitance of a device calculated by measuring the operating current in the no-load condition.
Output capacitance	C_{OUT}	The capacitance between the output and ground terminals for a three-state or open-drain output in the high-impedance state.
Sine Wave Distortion	THD	For analog switch, multiplexer and demultiplexer ICs, the distortion rate of the sine wave that is output when a sine wave is input in the on state.
Feed-through attenuation (switch off)	FTH	For analog switch, multiplexer and demultiplexer ICs, the ratio of the leakage voltage that appears at the output to the input voltage applied in the off state
Crosstalk (control input to signal output)	X_{talk}	For analog switch, multiplexer and demultiplexer ICs, the leakage voltage of a signal to the input and output that occurs when the control input changes.
Crosstalk (between any switches)	X_{talk}	For analog switch, multiplexer and demultiplexer ICs, the ratio of the voltage applied to a switch (port) in the on state to the voltage that appears at a switch (port) in the off state
Quiet output maximum dynamic V_{OL}	V_{OLP}	The maximum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.
Quiet output minimum dynamic V_{OL}	V_{OLV} $\lvert V_{OLV} \rvert$	The minimum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.
Quiet output minimum dynamic V_{OH}	V_{OHV}	The minimum peak voltage induced into an output that is fixed at the High level when the other outputs are switching simultaneously.
Minimum high-level dynamic input voltage	V_{IHD}	High-level dynamic threshold voltage when all inputs are switching simultaneously
Maximum low-level dynamic input voltage	V_{ILD}	Low-level dynamic threshold voltage when all inputs are switching simultaneously.

6.4. Built-in Function

Parameter	Definition
Input tolerant function	A function designed to prevent a current from flowing from an input to the power supply when the input voltage is higher than the power supply voltage or when V_{CC} = 0 V.
Output tolerant function	A function designed to prevent a current from flowing from an output to the power supply when the output is in the high-impedance state or when V_{CC} = 0 V.
Power-down protection	A function designed to prevent a current from flowing to the power supply terminal even if a voltage is applied to the input and output terminals when V_{CC} = 0 V.
Bus-hold function	A function designed to hold the input logic level using a latch circuit even when the input terminal becomes open.

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