

Silicon P Channel MOS Type / Silicon Epitaxial Schottky Barrier Diode

# SSM6G18NU

## Power Management Switch Applications

- Combined a P-channel MOSFET and a Schottky barrier diode in one package.
- Low  $R_{DS(ON)}$  and Low  $V_F$ 
  - $R_{DS(ON)} = 261\text{ m}\Omega$  (max) (@ $V_{GS} = -1.5\text{ V}$ )
  - $R_{DS(ON)} = 185\text{ m}\Omega$  (max) (@ $V_{GS} = -1.8\text{ V}$ )
  - $R_{DS(ON)} = 143\text{ m}\Omega$  (max) (@ $V_{GS} = -2.5\text{ V}$ )
  - $R_{DS(ON)} = 112\text{ m}\Omega$  (max) (@ $V_{GS} = -4.5\text{ V}$ )

## Absolute Maximum Ratings

### MOSFET ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		$V_{DSS}$	-20	V
Gate-Source voltage		$V_{GSS}$	$\pm 8$	V
Drain current	DC	$I_D$ (Note 1)	-2.0	A
	Pulse	$I_{DP}$ (Note 1)	-4.0	
Power dissipation	$P_D$ (Note 2)		1	W
	$t < 10\text{ s}$		2	
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$

### Schottky Barrier Diode( $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Reverse voltage	$V_R$	30	V
Average forward current	$I_O$	1.0	A
Peak one cycle surge forward current(10ms)	$I_{FSM}$	5.0	A
Junction temperature	$T_j$	150	$^\circ\text{C}$

### MOSFET and Diode ( $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Storage temperature range	$T_{stg}$	-55 to 150	$^\circ\text{C}$

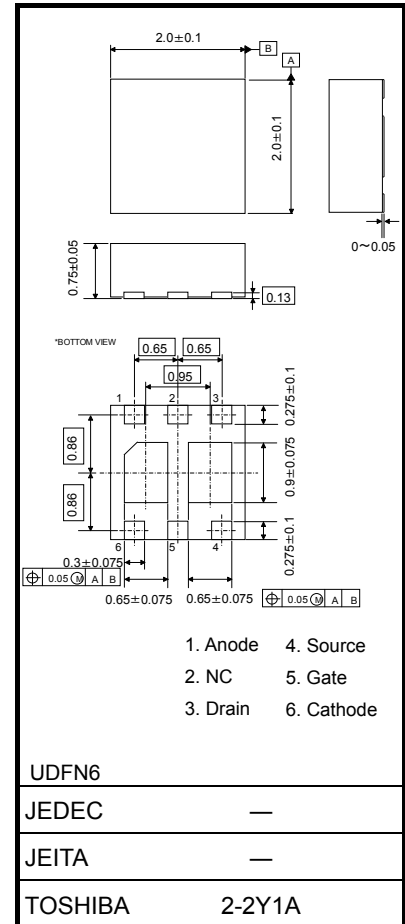
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The junction temperature should not exceed  $150^\circ\text{C}$  during use.

Note 2: Mounted on FR4 board.  
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645mm<sup>2</sup>)

Unit: mm



Start of commercial production  
2010-11

## MOSFET

### Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$	-20	—	—	V
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}, V_{GS} = 5 \text{ V}$ (Note 4)	-15	—	—	
Drain cut-off current	$I_{DSS}$	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	—	-1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -1.0 \text{ A}$ (Note 3)	2.7	5.4	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -1.0 \text{ A}, V_{GS} = -4.5 \text{ V}$ (Note 3)	—	89	112	m $\Omega$
		$I_D = -0.6 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note 3)	—	107	143	
		$I_D = -0.4 \text{ A}, V_{GS} = -1.8 \text{ V}$ (Note 3)	—	128	185	
		$I_D = -0.2 \text{ A}, V_{GS} = -1.5 \text{ V}$ (Note 3)	—	148	261	
Input capacitance	$C_{iss}$	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	270	—	pF
Output capacitance	$C_{oss}$		—	40	—	
Reverse transfer capacitance	$C_{rss}$		—	32	—	
Total Gate Charge	$Q_g$	$V_{DD} = -10 \text{ V}, I_D = -2.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}$	—	4.6	—	nC
Gate-Source Charge	$Q_{gs1}$		—	0.4	—	
Gate-Drain Charge	$Q_{gd}$		—	0.9	—	
Switching time	Turn-on time	$t_{on}$	$V_{DD} = -10 \text{ V}, I_D = -1.0 \text{ A}$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_G = 4.7 \Omega$	—	17	ns
	Turn-off time	$t_{off}$		—	43	
Drain-Source forward voltage	$V_{DSF}$	$I_D = 2.0 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 3)	—	0.86	1.2	V

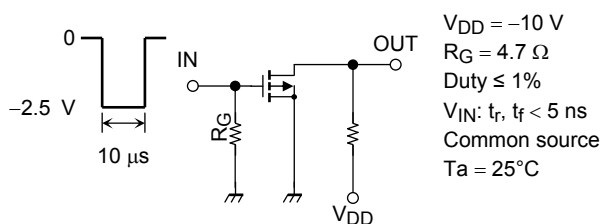
Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode.

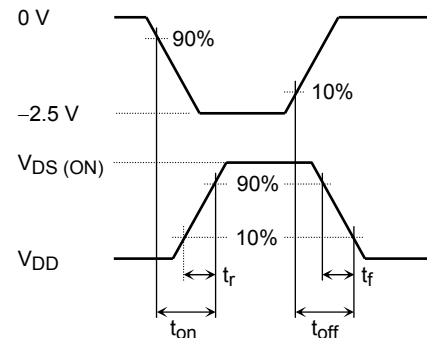
Note that the drain-source breakdown voltage is lowered in this mode

### Switching Time Test Circuit

#### (a) Test circuit



#### (b) $V_{IN}$



#### (c) $V_{OUT}$

### Precaution

$V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = -1\text{mA}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires lower voltage than  $V_{th}$ .

(Relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ )

Please take this into consideration for using the device.

## Schottky Barrier Diode

### Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Forward voltage	$V_F (1)$	$I_F = 100 \text{ mA}$	—	0.31	—	V
	$V_F (2)$	$I_F = 200 \text{ mA}$	—	0.36	—	
	$V_F (3)$	$I_F = 500 \text{ mA}$	—	0.38	0.45	
	$V_F (4)$	$I_F = 1000 \text{ mA}$	—	0.48	0.58	
Reverse current	$I_R$	$V_R = 30 \text{ V}$	—	5	50	$\mu\text{A}$
Total capacitance	$C_T$	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$	—	120	—	pF

### Precaution

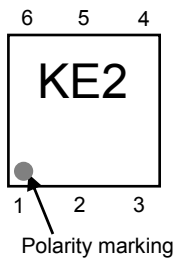
The Schottky barrier diode in this device has large reverse current leakage compared to typical switching diodes. Thus, excessive operating temperature or voltage may cause thermal runaway. To avoid this problem, be sure to take both forward and reverse loss into consideration.

### Handling Precaution

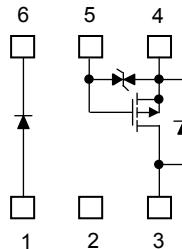
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance  $R_{th(ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

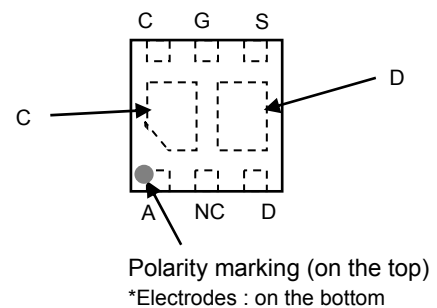
### Marking(Top View)



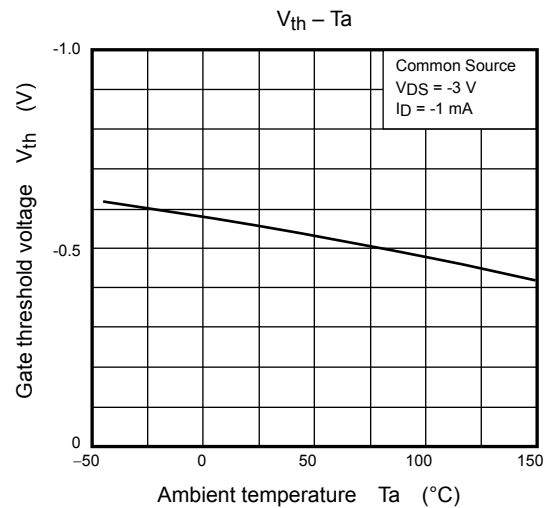
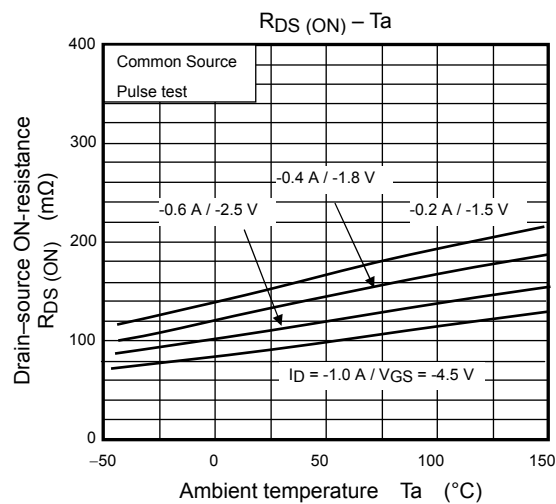
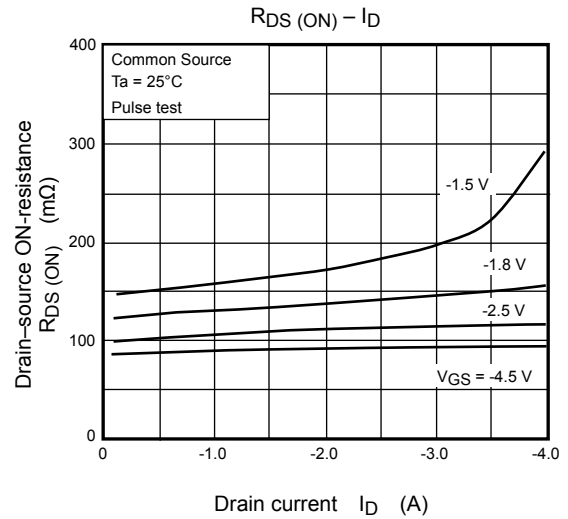
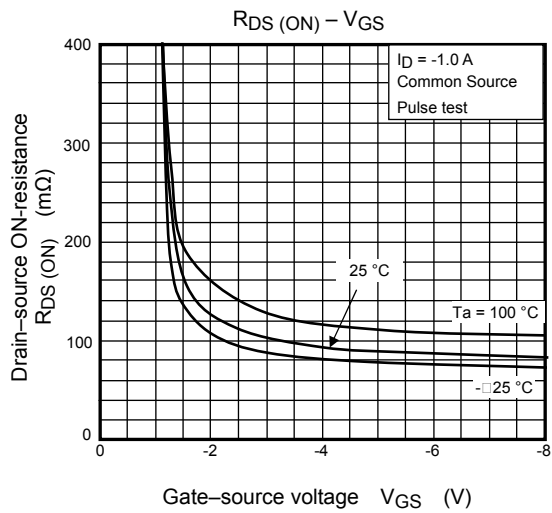
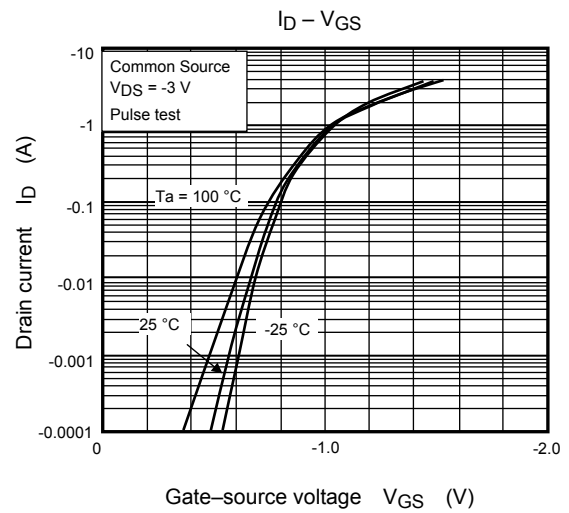
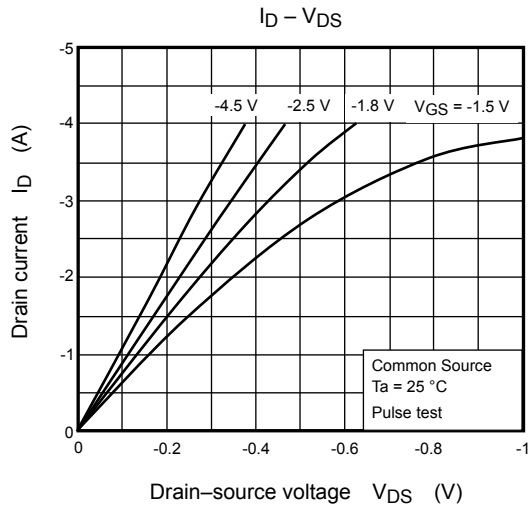
### Equivalent Circuit(Top View)

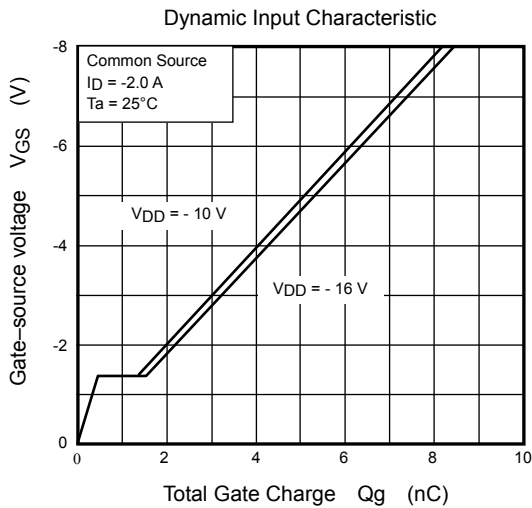
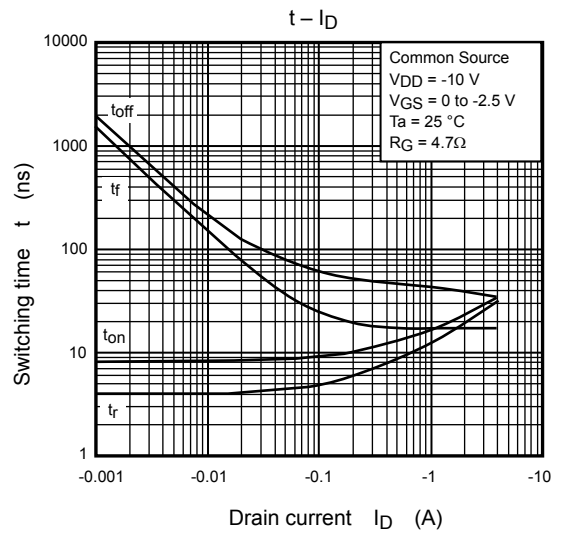
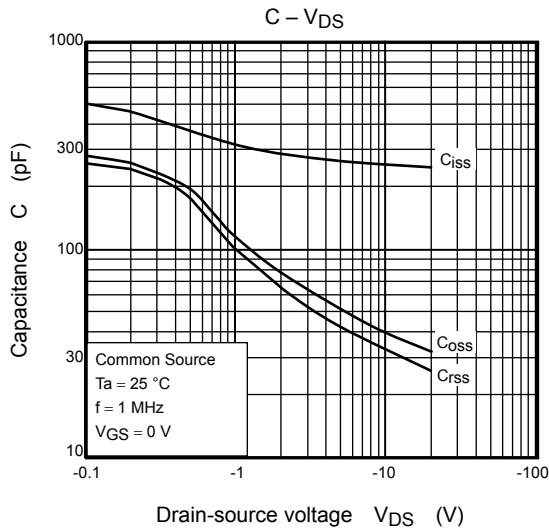
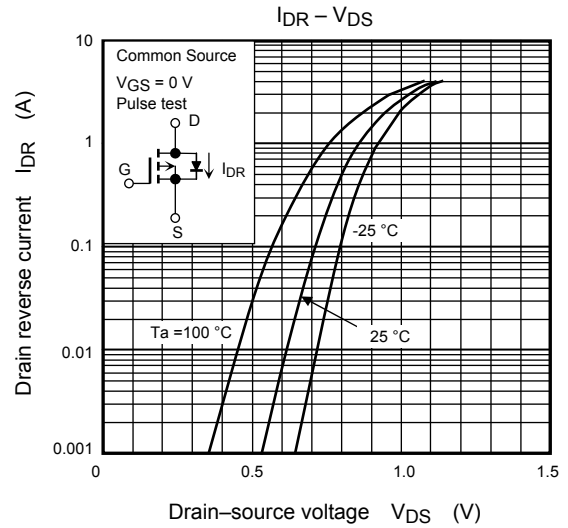
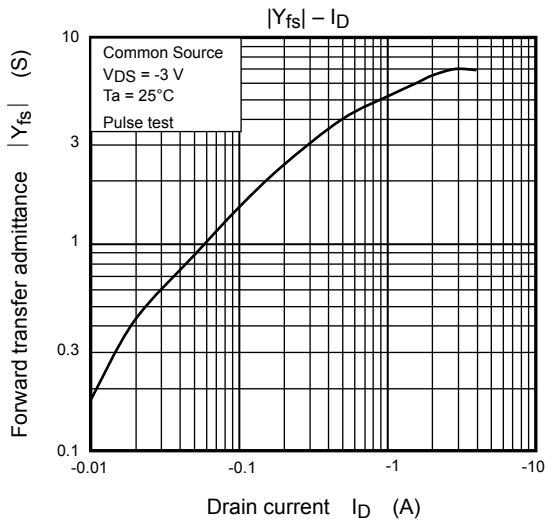


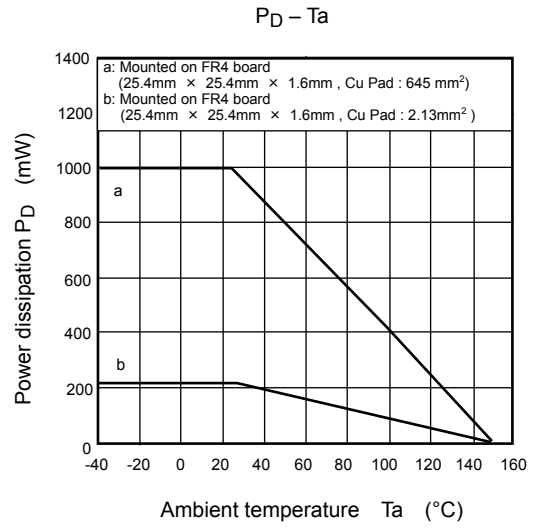
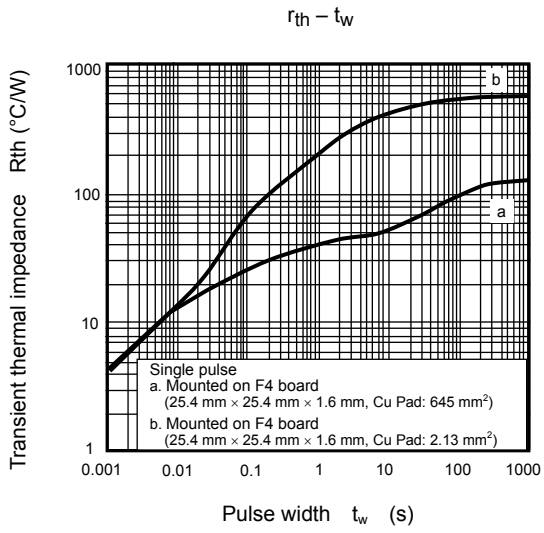
### Pin Condition(Top View)



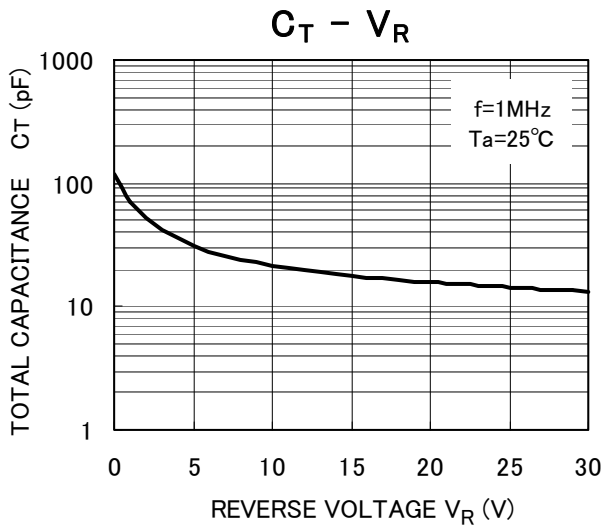
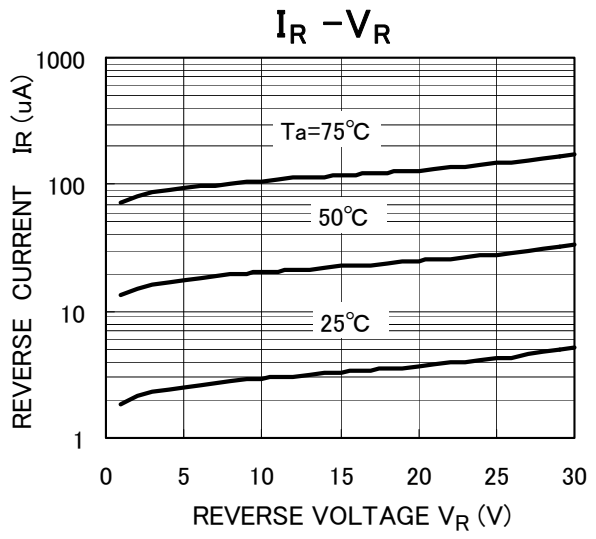
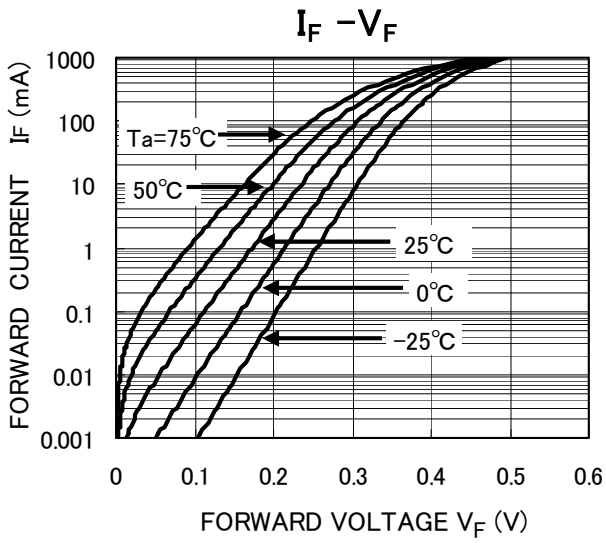
## •MOSFET







**Schottky Barrier Diode**



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