MOSFETs Silicon N-channel MOS (U-MOSⅨ-H)

TPW1R104PB

1. Applications

- Automotive
- Motor Drivers
- Switching Voltage Regulators

2. Features

(1) AEC-Q101 qualified

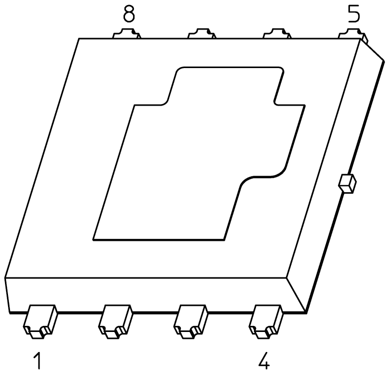
(2) Small, thin package

(3) Low drain-source on-resistance: $R_{DS(ON)}$ = 0.95 mΩ (typ.) (V_{GS} = 10 V)

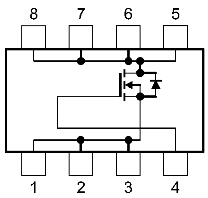
(4) Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 40 V)

(5) Enhancement mode: V_{th} = 2.0 to 3.0 V (V_{DS} = 10 V, I_D = 0.5 mA)

3. Packaging and Internal Circuit



DSOP Advance(WF)M



1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain

Start of commercial production
2018-08

4. Absolute Maximum Ratings (Note) (T_a = 25 °C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	40	V
Gate-source voltage			V_{GSS}	±20	
Drain current (DC)		(Note 1)	I_D	120	A
Drain current (pulsed)		(Note 1)	I_{DP}	360	
Power dissipation	(T_c = 25 °C)	(Note 6)	P_D	132	W
Power dissipation	(t = 10 s)	(Note 2)		3.0	
Power dissipation	(t = 10 s)	(Note 3)		0.96	
Single-pulse avalanche energy		(Note 4)	E_{AS}	140	mJ
Single-pulse avalanche current			I_{AS}	120	A
Channel temperature		(Note 5)	T_{ch}	175	°C
Storage temperature		(Note 5)	T_{stg}	-55 to 175	

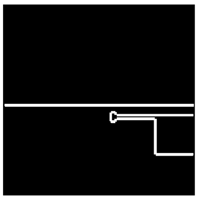
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: When the body or a connecting part of a semiconductor product is subjected to vibration, impact or stress in actual equipment, bonding fault or device destruction may result.
Therefore, be sure to keep this in mind at the time of structural design.
If a semiconductor product is subject to especially strong vibration, impact or stress, the package or chip may crack. If stress is applied to a semiconductor chip through the package, changes in the resistance of the chip may result due to piezoelectric effects, resulting in fluctuation in element characteristics.
Furthermore, if a stress that does not instantly result in damage is applied continually for a long period of time, product deformation may result, causing defects such as disconnection or element failure.
Thus, at the time of structural design, carefully consider vibration, impact and stress.

5. Thermal Characteristics

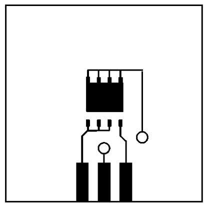
Characteristics	Symbol	Max	Unit
Channel-to-case thermal impedance (T_c = 25 °C)	$z_{th(ch-c)}$	1.13	°C/W
Channel-to-top-plate thermal impedance (Note 7)	$z_{th(ch-tp)}$	1.5	
Channel-to-ambient thermal impedance (t = 10 s) (Note 2)	$z_{th(ch-a)}$	50	
Channel-to-ambient thermal impedance (t = 10 s) (Note 3)	$z_{th(ch-a)}$	156	

Note 1: Ensure that the channel temperature does not exceed 175 °C.
Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1
Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2
Note 4: V_{DD} = 32 V, T_{ch} = 25 °C (initial), L = 7.47 μH, R_G = 25 Ω, I_{AS} = 120 A
Note 5: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.
Note 6: T_c is defined as a temperature of the drain electrode.
Note 7: A maximum of the $z_{th(ch-tp)}$ measured at Toshiba's test environment is only used for reference.
An area of the top-plate is shown in Figure 5.3.
Be aware that the top-plate has the same electric potential as the sources; however, not intended for an electrode.



FR-4
25.4 × 25.4 × 1.6
(Unit: mm)
2 oz copper

Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)



FR-4
25.4 × 25.4 × 1.6
(Unit: mm)
2 oz copper

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

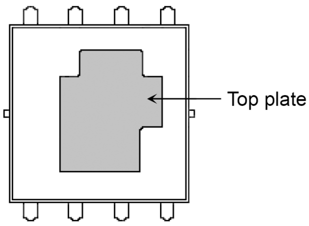


Fig. 5.3 Top view

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	40	—	—	V
	$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = -20 V	20	—	—	
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 0.5 mA	2.0	—	3.0	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 6 V, I_D = 60 A	—	1.30	1.96	mΩ
		V_{GS} = 10 V, I_D = 60 A	—	0.95	1.14	

6.2. Dynamic Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 300 kHz	—	4560	—	pF
Reverse transfer capacitance	C_{rss}		—	320	—	
Output capacitance	C_{oss}		—	2940	—	
Gate resistance	r_g		—	2.9	—	Ω
Switching time (rise time)	t_r	See Fig. 6.2.1	—	8	—	ns
Switching time (turn-on time)	t_{on}		—	22	—	
Switching time (fall time)	t_f		—	23	—	
Switching time (turn-off time)	t_{off}		—	71	—	

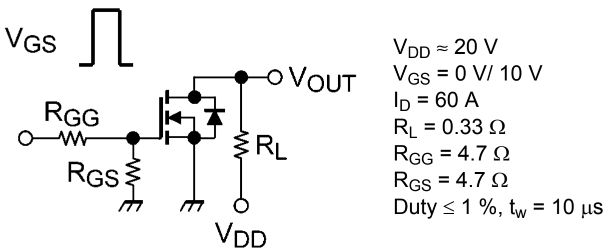


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ 32 V, V_{GS} = 10 V, I_D = 120 A	—	55	—	nC
Gate-source charge 1	Q_{gs1}		—	20	—	
Gate-drain charge	Q_{gd}		—	13	—	

6.4. Source-Drain Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 8)	I_{DRP}	—	—	—	360	A
Diode forward voltage	V_{DSF}	I_{DR} = 120 A, V_{GS} = 0 V	—	—	-1.2	V

Note 8: Ensure that the channel temperature does not exceed 175 °C.

7. Marking

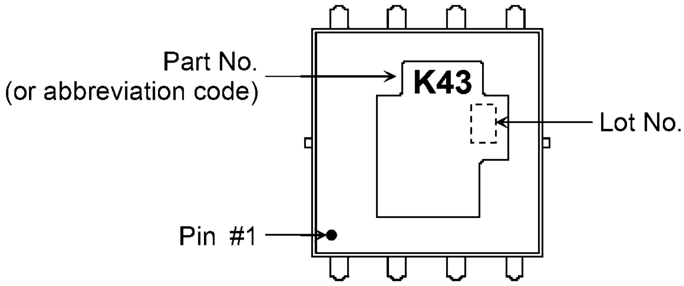


Fig. 7.1 Marking

8. Characteristics Curves (Note)

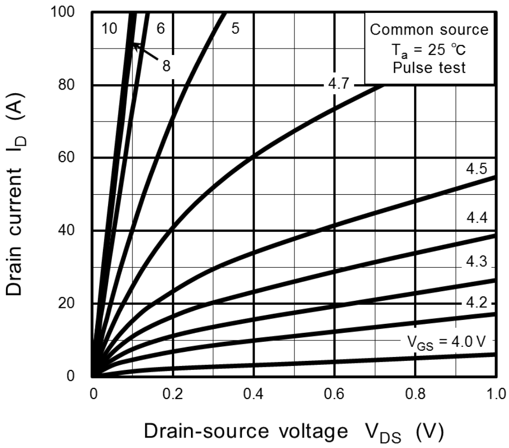


Fig. 8.1 I_D - V_{DS}

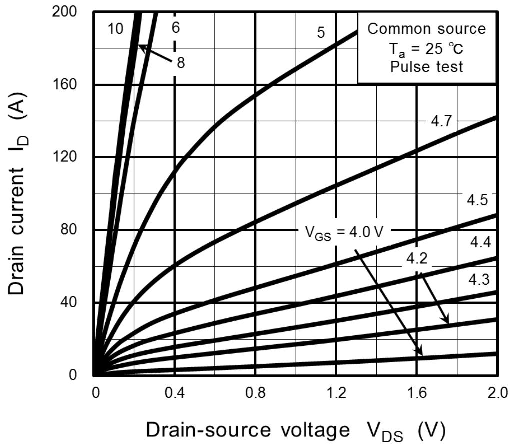


Fig. 8.2 I_D - V_{DS}

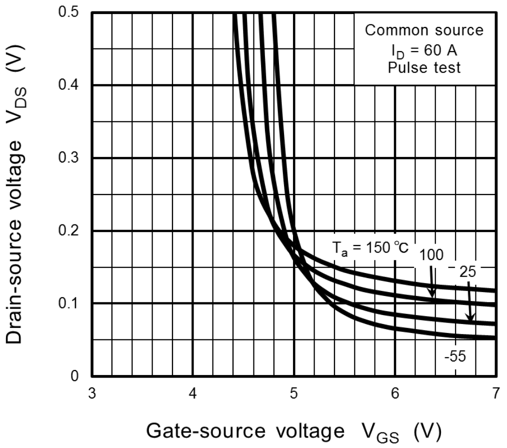


Fig. 8.3 V_{DS} - V_{GS}

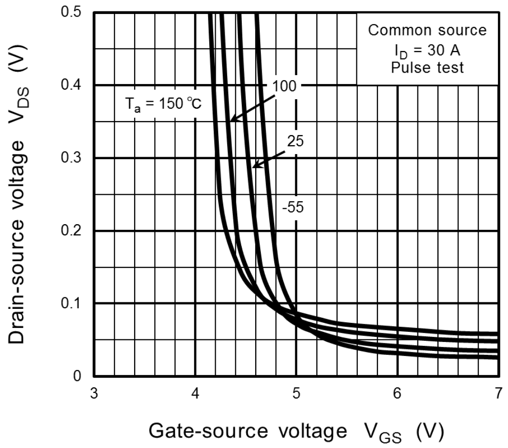


Fig. 8.4 V_{DS} - V_{GS}

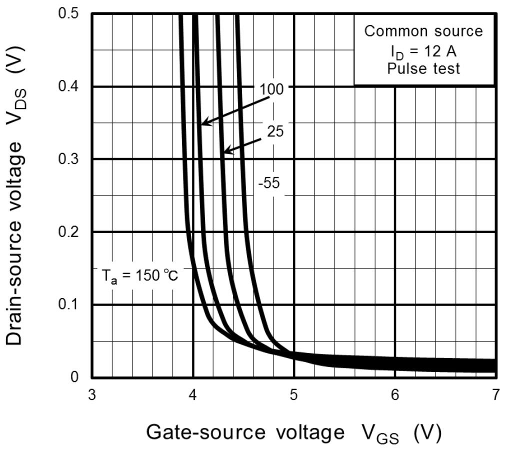


Fig. 8.5 V_{DS} - V_{GS}

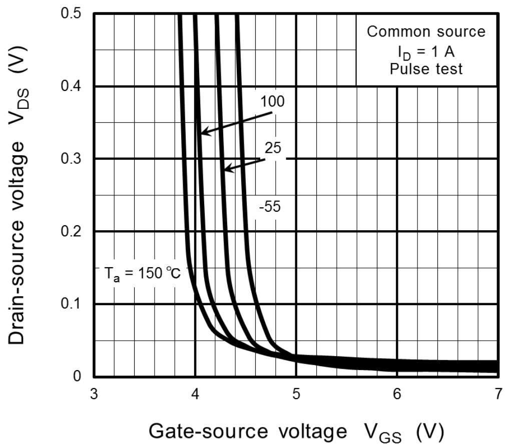


Fig. 8.6 V_{DS} - V_{GS}

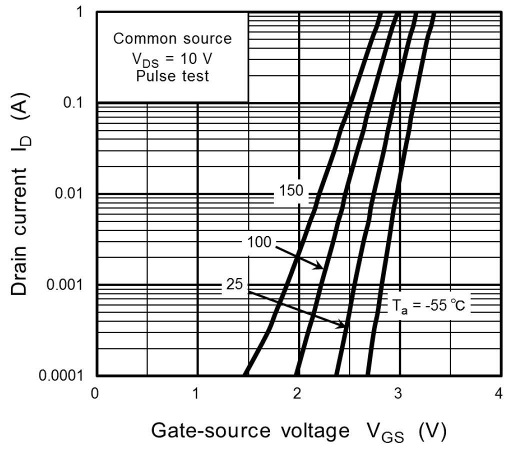


Fig. 8.7 I_D - V_{GS}

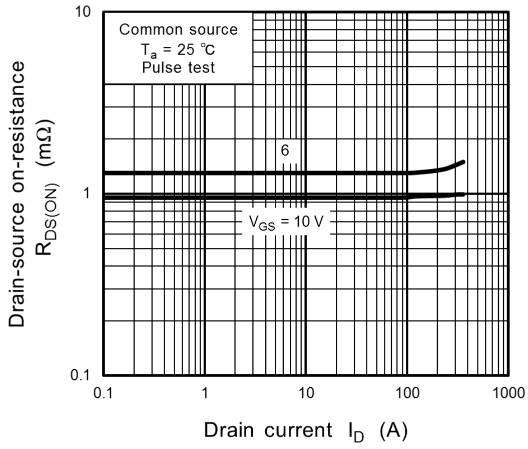


Fig. 8.8 $R_{DS(ON)}$ - I_D

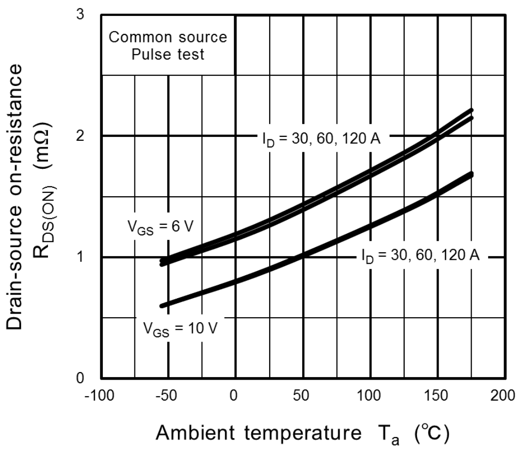


Fig. 8.9 $R_{DS(ON)}$ - T_a

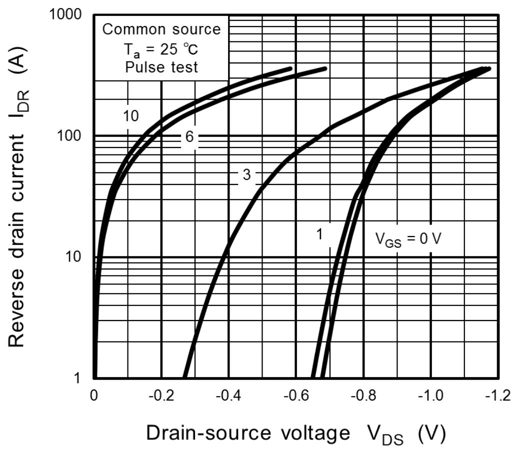


Fig. 8.10 I_{DR} - V_{DS}

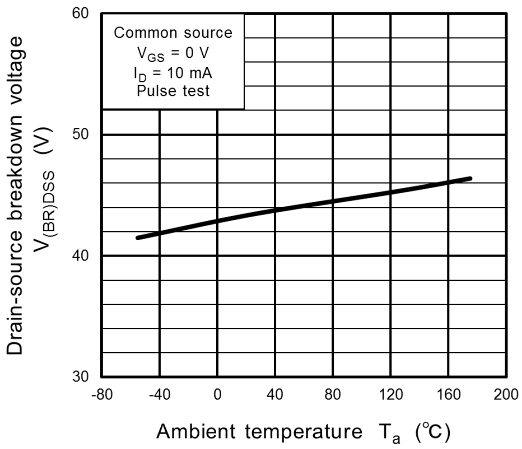


Fig. 8.11 $V_{(BR)DSS}$ - T_a

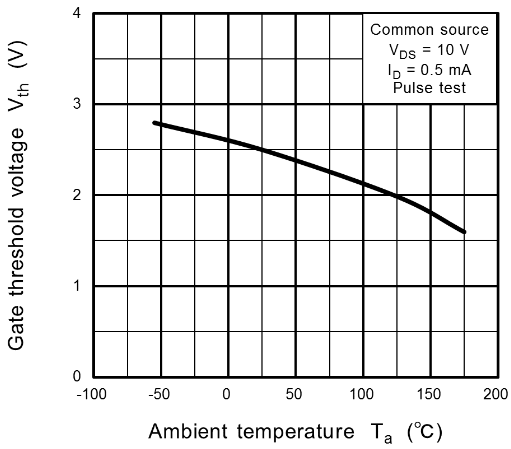


Fig. 8.12 V_{th} - T_a

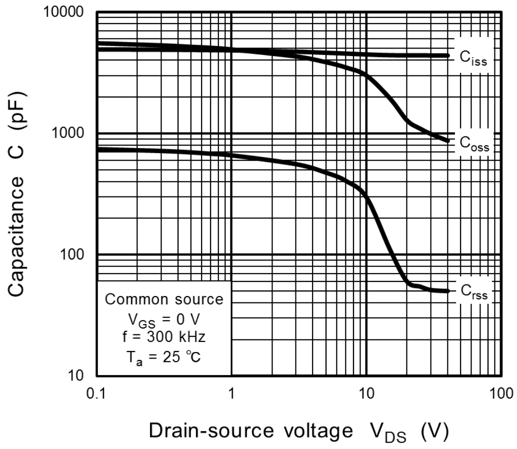


Fig. 8.13 Capacitance - V_{DS}

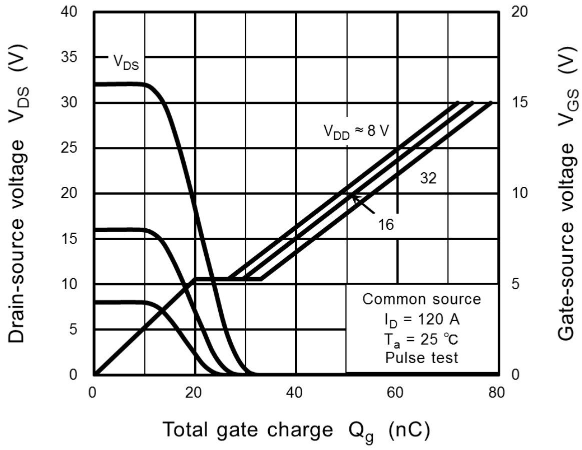


Fig. 8.14 Dynamic Input/Output Characteristics

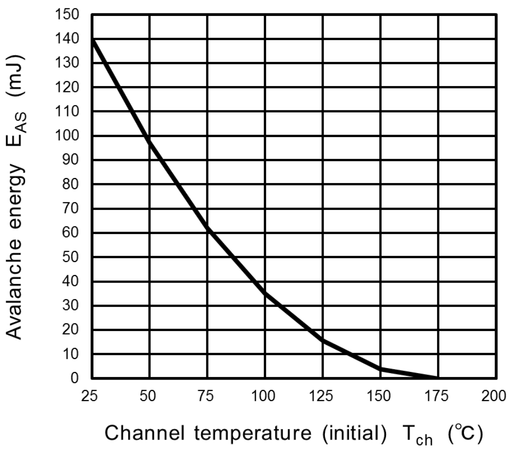
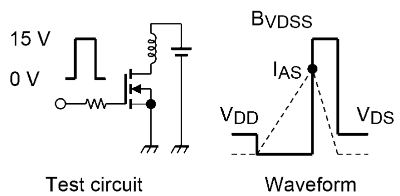


Fig. 8.15 E_{AS} - T_{ch}(Guaranteed Maximum)



RG = 25 Ω
VDD = 32 V, L = 7.47 μH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \left(\frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \right)$$

Fig. 8.16 Test Circuit/Waveform

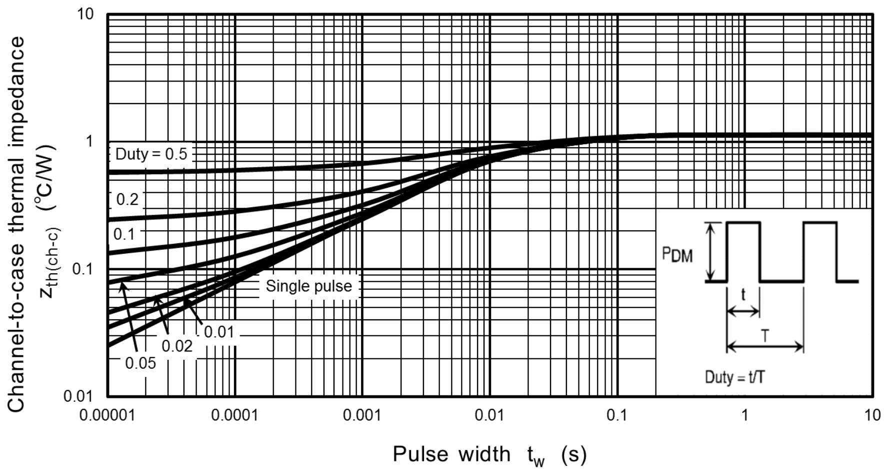


Fig. 8.17 $z_{th(ch-c)}$ - t_w
(Guaranteed Maximum)

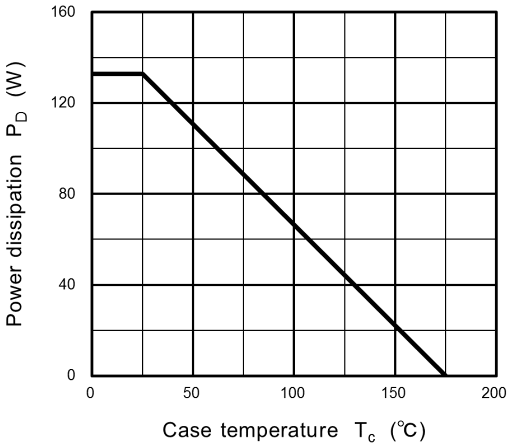


Fig. 8.18 P_D - T_c
(Guaranteed Maximum)

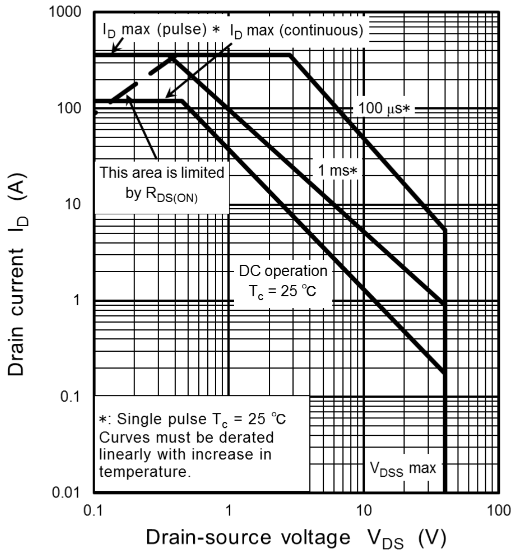


Fig. 8.19 Safe Operating Area
(Guaranteed Maximum)

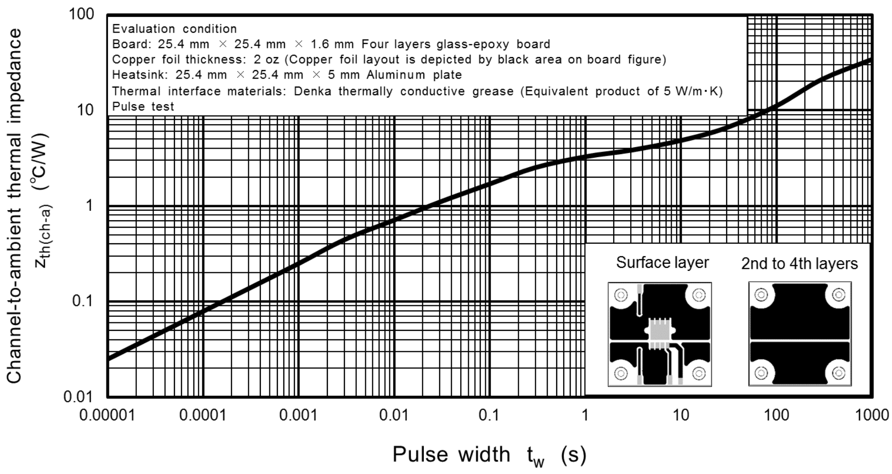
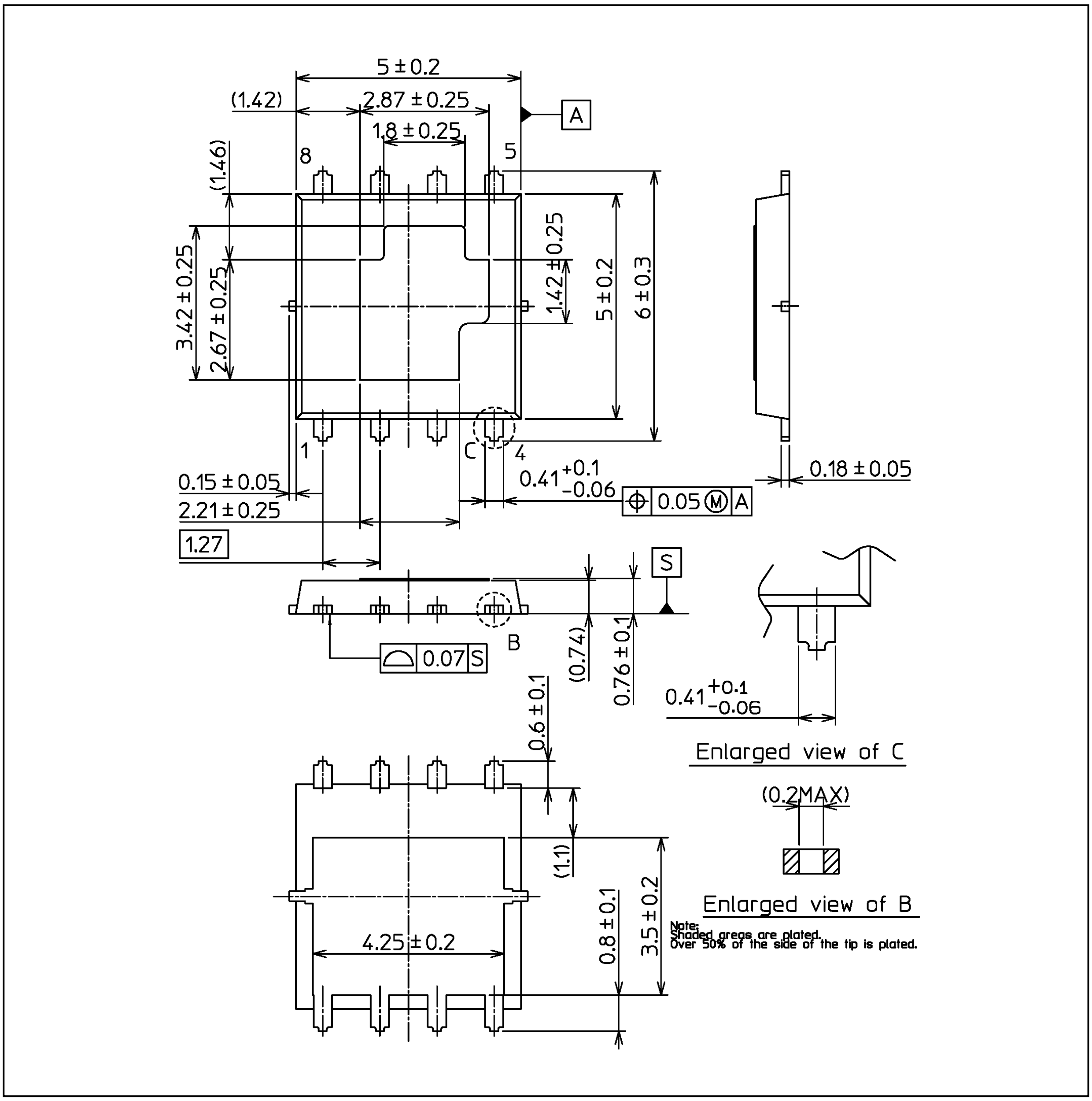


Fig. 8.20 $z_{th(ch-a)}$ - t_w
(Reference Values)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.088 g (typ.)

Package Name(s)
TOSHIBA: 2-5U1A
Nickname: DSOP Advance(WF)M

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