CMOS Digital Integrated Circuits Silicon Monolithic

TC74VHC9125FK,TC74VHC9126FK

1. Functional Description

- 5-Bit Universal Schmitt Buffer with 3-State Outputs

2. General

The TC74VHC9125FK/TC74VHC9126FK are an ultra-high-speed 5-bit Schmitt buffer fabricated using silicon-gate CMOS technology. The TC74VHC9125FK/TC74VHC9126FK combines low power consumption of CMOS with Schottky TTL speeds.

Y1 to Y4 outputs can be put in the high-impedance state by placing a logic HIGH on the Enable ($\overline{G}$) input. The CONT input determines the logical inversion of data. A logic LOW on the CONT input configures the TC74VHC9125FK/TC74VHC9126FK as an inverter; a logic HIGH on the CONT input configures the TC74VHC9125FK/TC74VHC9126FK as a buffer.

TC74VHC9125FK Y5 output is an inverting type, and the TC74VHC9126FK Y5 output is a non-inverting type.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHC9125FK/TC74VHC9126FK are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Additionally, all the inputs have a newly developed protection circuit without a diode returned to V_{CC}. This enables the inputs to be tolerant of up to 5 volts even when power supply is down. The input power-down protection capability makes the TC74VHC9125FK/TC74VHC9126FK ideal for a wide range of applications, such as interfacing between different voltages, voltage translation from 5 V to 3 V and battery back-up circuits.

3. Features

(1) High speed: tpd = 5.0 ns (typ.) at V_{CC} = 5.0 V

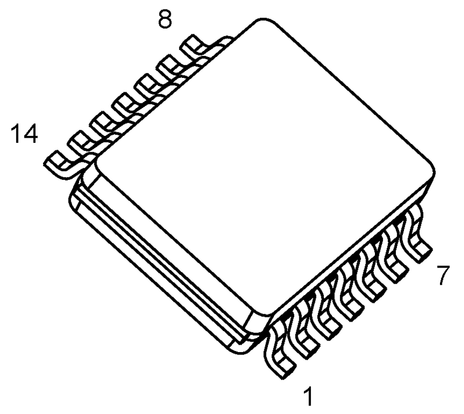
(2) Low supply current: I_{CC} = 2.0 μA (max) (T_a = 25 °C)

(3) All inputs are provided with power-down protection.

(4) Symmetrical rise and fall delays: $t_{PLH} \approx t_{PHL}$

(5) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 V to 5.5 V

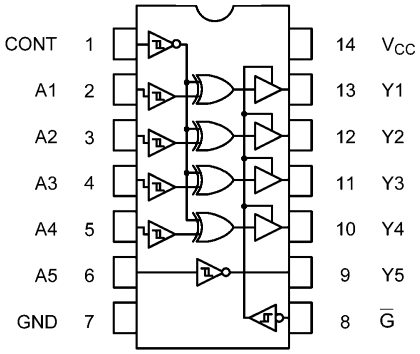
4. Packaging



US14

Start of commercial production
2009-04

5. Pin Assignment



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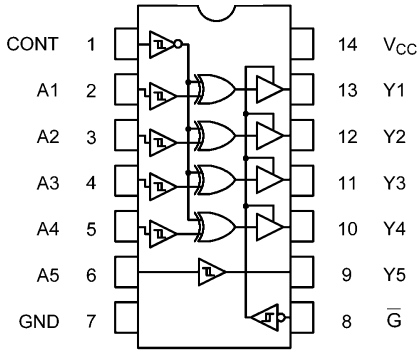

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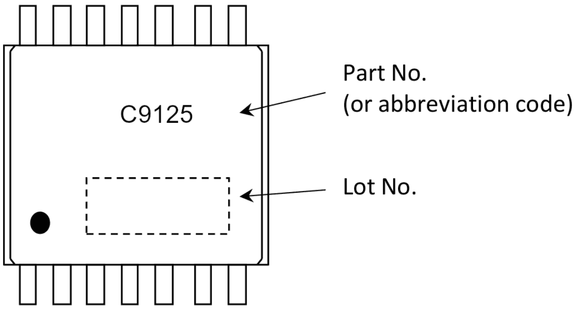
6. Marking



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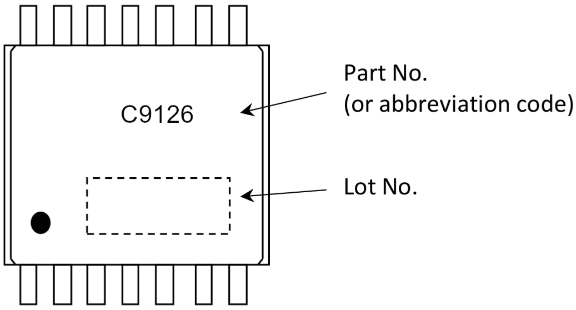


TC74VHC9126FK

7. Truth Table

Inputs			Outputs
$\overline{G}$	CONT	A1 to 4	Y1 to 4
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H

Inputs	Outputs	
A5	Y5(9125)	Y5(9126)
L	H	L
H	L	H

X: Don't care
Z: High impedance

8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_{IN}	-0.5 to 7.0	V
Output voltage	V_{OUT}	-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20	mA
Output current	I_{OUT}	±25	mA
V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	℃

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

9. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	℃

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

10. Electrical Characteristics

10.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
Positive threshold voltage	V_P	—		3.0	—	—	2.20	V
				4.5	—	—	3.15	
				5.5	—	—	3.85	
Negative threshold voltage	V_N	—		3.0	0.90	—	—	V
				4.5	1.35	—	—	
				5.5	1.65	—	—	
Hysteresis voltage	V_H	—		3.0	0.30	—	1.20	V
				4.5	0.40	—	1.40	
				5.5	0.50	—	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	3.0	2.58	—	—	
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	
			I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	μA

10.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Positive threshold voltage	V_P	—		3.0	—	2.20	V
				4.5	—	3.15	
				5.5	—	3.85	
Negative threshold voltage	V_N	—		3.0	0.90	—	V
				4.5	1.35	—	
				5.5	1.65	—	
Hysteresis voltage	V_H	—		3.0	0.30	1.20	V
				4.5	0.40	1.40	
				5.5	0.50	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	3.0	2.48	—	
			I_{OH} = -8 mA	4.5	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	3.0	—	0.44	
			I_{OL} = 8 mA	4.5	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	20.0	μA

10.3. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: t_r = t_f = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time (A1 to A4 - Y1 to Y4)	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	—	6.0	8.0	ns
					50	—	9.0	12.5	
				5.0 ± 0.5	15	—	5.0	5.5	
					50	—	7.0	8.5	
Propagation delay time (CONT - Y1 to Y4)	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	—	8.5	11.5	ns
					50	—	13.0	17.0	
				5.0 ± 0.5	15	—	6.5	8.0	
					50	—	10.5	12.5	
Propagation delay time (A5 - Y5)	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	—	6.0	8.0	ns
					50	—	9.0	12.5	
				5.0 ± 0.5	15	—	5.0	5.5	
					50	—	7.0	8.5	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	3.3 ± 0.3	15	—	6.0	8.0	ns
					50	—	10.5	13.5	
				5.0 ± 0.5	15	—	4.5	5.5	
					50	—	9.0	10.5	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	3.3 ± 0.3	50	—	12.5	13.5	ns
				5.0 ± 0.5	50	—	9.0	9.5	
Output skew (A1 to A4 - Y1 to Y4)	t_{osLH}, t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	—	1.5	ns
				5.0 ± 0.5	50	—	—	1.0	
Input capacitance	C_{IN}		—			—	4	10	pF
Output capacitance	C_{OUT}		—			—	6	—	pF
Power dissipation capacitance	C_{PD}	(Note 2)	f_{IN} = 1 MHz			—	10	—	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

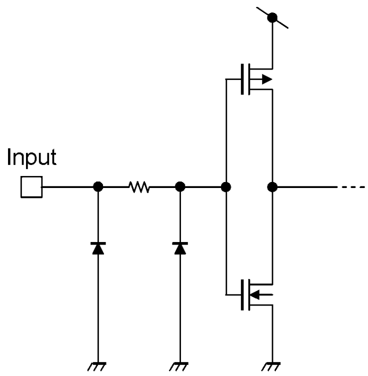
$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/5$ (per bit)

10.4. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (A1 to A4 - Y1 to Y4)	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	10.0	ns
					50	1.0	15.0	
				5.0 ± 0.5	15	1.0	7.0	
					50	1.0	10.0	
Propagation delay time (CONT - Y1 to Y4)	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	13.5	ns
					50	1.0	20.5	
				5.0 ± 0.5	15	1.0	9.5	
					50	1.0	15.0	
Propagation delay time (A5 - Y5)	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	10.0	ns
					50	1.0	15.0	
				5.0 ± 0.5	15	1.0	7.0	
					50	1.0	10.0	
3-state output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	3.3 ± 0.3	15	1.0	9.5	ns
					50	1.0	16.5	
				5.0 ± 0.5	15	1.0	6.5	
					50	1.0	12.5	
3-state output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	3.3 ± 0.3	50	1.0	16.0	ns
				5.0 ± 0.5	50	1.0	11.0	
Output skew (A1 to A4 - Y1 to Y4)	t_{osLH},t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	1.5	ns
				5.0 ± 0.5	50	—	1.0	
Input capacitance	C_{IN}		—			—	10	pF

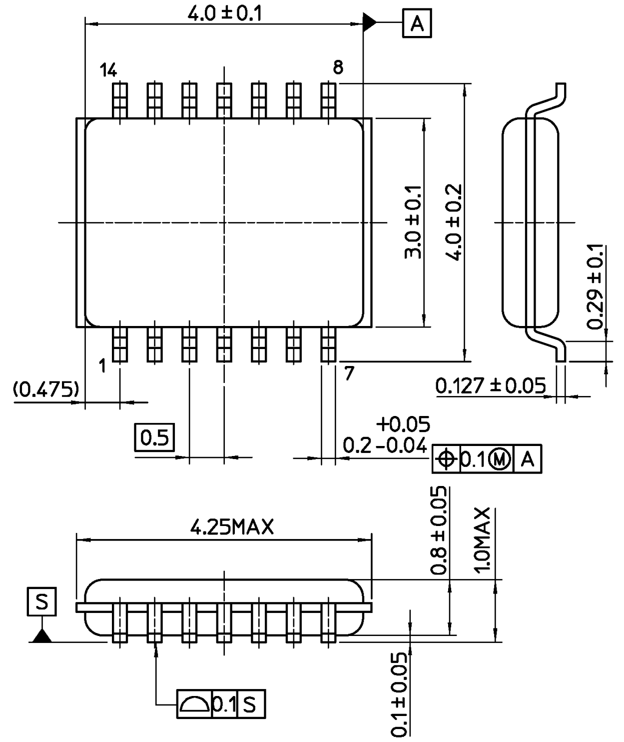
Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

11. Internal Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.02 g (typ.)

Package Name(s)
Nickname: US14

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