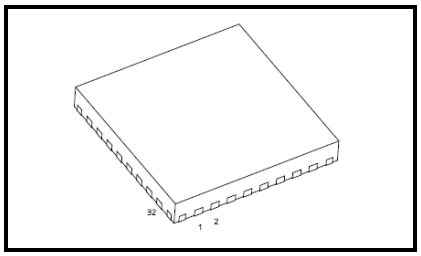
Toshiba Intelligent Power Device Silicon Monolithic Power MOS Integrated Circuit

TPD7212F

Power MOSFET Gate Driver for 3-Phase DC Motor

The TPD7212F is a power MOSFET gate driver for 3-phase full-bridge circuits for the charge pump method by the BiCD process. The inclusion of a charge pump circuit for drivers inside the IC makes it easy to configure a 3-phase full-bridge circuit.



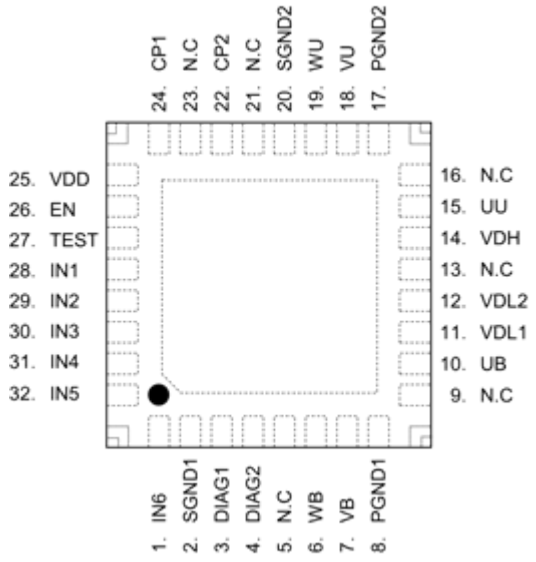
P-WQFN32-0505-0.50-002
Weight: 0.06g (typ.)

Features

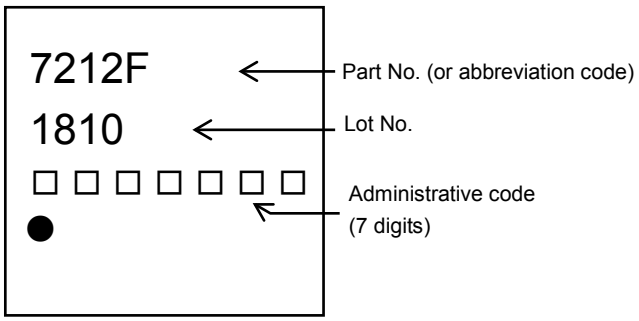
- Power MOSFET gate driver for 3-phase DC motor.
- Built-in power supply for driver and diagnosis function of output voltage.
- Built-in charge pump circuit.
- Package is provided with a WQFN32 embossed-tape packing.

Pin Assignment

(TOP VIEW)



Marking

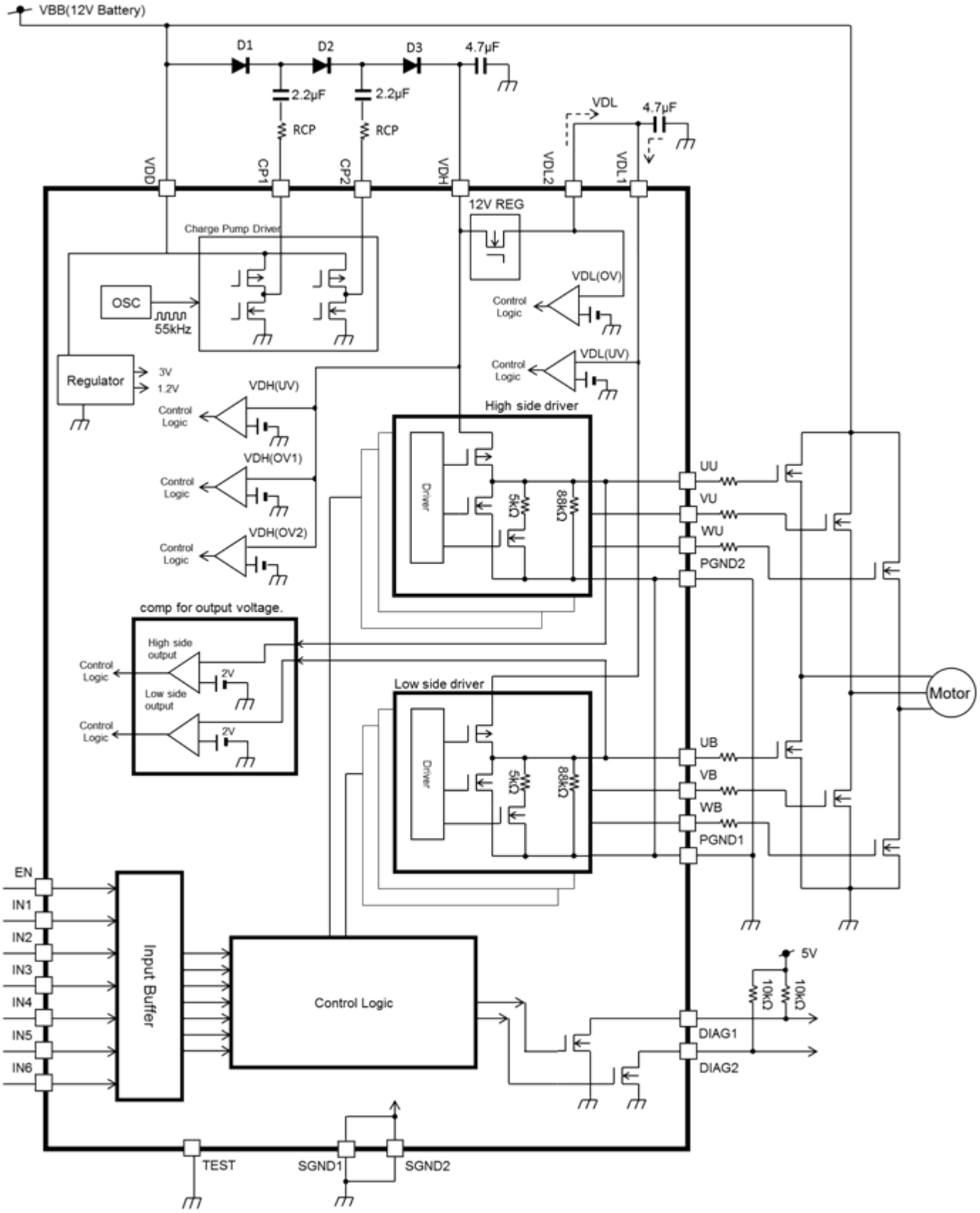


Note : The dotted line expresses exposure of the frame on the back.
The exposed area of the back central part is electrically connected with the unindicated name corner pin.
(Please insulate or short to GND.)

This product has a MOS structure and is sensitive to electrostatic discharge

Start of commercial production
2018-08

Block diagram / Application circuit



Pin Description

Pin No.	Symbol	Pin Description
1	IN6	Input pin: It controls for WB. Built in pull down resistor (100kΩ typ.).
2	SGND1	Signal block GND pin.: shared internally with SGND2.
3	DIAG1	Diagnosis detection pin. Nch open drain.
4	DIAG2	Diagnosis detetion pin. Nch open drain.
5	N.C	No-Connect pin.
6	WB	Drives the power MOSFET connected to the low side of the W phase.
7	VB	Drives the power MOSFET connected to the low side of the V phase.
8	PGND1	Power block GND pin.: shared internally with PGND2.
9	N.C	No-Connect pin.
10	UB	Drives the power MOSFET connected to the low side of the U phase.
11	VDL1	Power supply pin for low side drive. please connnect to VDL2 pin outside.
12	VDL2	Power supply pin for low side drive. please connnect to VDL1 pin outside.
13	N.C	No-Connect pin.
14	VDH	Output pin for charge pump.
15	UU	Drives the power MOSFET connected to the high side of the U phase.
16	N.C	No-Connect pin.
17	PGND2	Power block GND pin.: shared internally with PGND1.
18	VU	Drives the power MOSFET connected to the high side of the V phase.
19	WU	Drives the power MOSFET connected to the high side of the W phase.
20	SGND2	Signal block GND pin.: shared internally with SGND1.
21	N.C	No-Connect pin.
22	CP2	Capacitor pin for charge pump
23	N.C	No-Connect pin.
24	CP1	Capacitor pin for charge pump
25	VDD	Power supply pin
26	EN	Inhibit pin (high active). Built in pull down resistor (400kΩtyp.).
27	TEST	For internal test. Please connect to GND during normal operation.
28	IN1	Input pin: It controls for UU. Built in pull down resistor (100kΩ typ.).
29	IN2	Input pin: It controls for VU. Built in pull down resistor (100kΩ typ.).
30	IN3	Input pin: It controls for WU. Built in pull down resistor (100kΩ typ.).
31	IN4	Input pin: It controls for UB. Built in pull down resistor (100kΩ typ.).
32	IN5	Input pin: It controls for VB. Built in pull down resistor (100kΩ typ.).

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	Note
Supply voltage	DC	$V_{DD(DC)}$	-0.3 to 25	V	
	pulse	$V_{DD(Pulse)}$	-0.3 to 40	V	t≤300ms
PGND voltage		V_{PGND}	-0.3 to 0.3	V	Standard in SGND
Output voltage	High side	V_{xU}	-0.3 to VDH+0.3	V	UU,VU,WU pin
	Low side	V_{xB}	-0.3 to VDL+0.3	V	UB,VB,WB pin
Output current	Source current	I_{xU}	-1.0	A	
	Sink current	I_{xB}	+1.5	A	
Input voltage	IN1 to IN6	V_{IN}	-0.3 to 6	V	
	EN	V_{EN}	-0.3 to 25	V	
Diagnosis output voltage		V_{DIAG}	-0.3 to 6	V	
Diagnosis output current		I_{DIAG}	5	mA	
Power dissipation		P_D	3.6	W	Note2
Operating temperature		T_{opr}	-40 to 150	°C	
Junction temperature		T_j	175	°C	
Storage temperature		T_{stg}	-55 to 175	°C	

Note1: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Rating	Unit
Thermal resistance, channel to ambient	$R_{th\ (j-a)}$	41	°C / W

Note 2: JEDEC standard.
Glass epoxy board
Material: FR-4(4 layer)
Board size：76.2mm×114.3mm×1.6mm
Via：φ0.3mm(9 point)

Electrical Characteristics (Unless otherwise specified Tj = −40 to 125°C, VDD = 5 to 18V)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Operating supply voltage		$V_{DD(opr)}$	-	4.5	12	18	V
Supply current		I_{DD}	V_{EN}=H,V_{INx}=L, V_{DD}=4.5 to 18V Note2	-	3.9	8	mA
Input voltage(IN)	High level	V_{INHx}	-	2.0	-	-	V
	Low level	V_{INLx}	-	-	-	1.0	V
Input voltage(EN)	High level	V_{ENHx}	-	2.0	-	-	V
	Low level	V_{ENLx}	-	-	-	1.0	V
Input current(IN)	High level	I_{INxH}	V_{INx}=5V	-	50	100	μA
	Low level	I_{INxL}	V_{INx}=0V	-1	0	1	μA
Input current(EN)	High level	I_{ENH}	V_{EN}=5V	-	12	30	μA
	Low level	I_{ENL}	V_{EN}=0V	-1	0	1	μA
Output voltage	High level	V_{OHxU1}	V_{DD}=4.5V,I_o=-1mA, Note2	V_{DD}+6	V_{DD}+7	-	V
		V_{OHxU2}	V_{DD}=7 to 18V,Io=-1mA, Note2	V_{DD}+10	V_{DD}+12	V_{DD}+16	V
		V_{OHxB1}	V_{DD}=4.5V,I_O=-1mA, Note2	7	10	-	V
		V_{OHxB2}	V_{DD}=7 to 18V,I_O=-1mA, Note2	10	13	16	V
	Low level	V_{OLxU1}	V_{DD}=4.5V,I_O=1mA	-	-	0.5	V
		V_{OLxU2}	V_{DD}=5 to 18V,I_O=1mA	-	-	0.5	V
		V_{OLxB1}	V_{DD}=4.5V,I_O=1mA	-	-	0.5	V
		V_{OLxB2}	V_{DD}=5 to 18V,I_O=1mA	-	-	0.5	V
Output detection voltage	High level	V_{OM}	V_{DD}=5 to 18V, V_{PGND}=V_{SGND}=0V	2.0	2.5	3.5	V
Mask time for monitoring output detection voltage.		t_{mask}	V_{DD}=5 to 18V	1.0	3.0	5.0	μs
Output pull down resistance	Normal mode	R_{pd1}	-	45	88	135	kΩ
	Hiz mode	R_{pd2}	I_O=+0.5mA,V_{DD}=5 to 18V	3.5	5.0	6.5	kΩ
Driver on resistance	Source side DMOS	$R_{DS(ON)HS}$	I_O=-0.1A,V_{DD}=5 to 18V	-	1.3	3.0	Ω
	Sink side DMOS	$R_{DS(ON)LS}$	I_O=+0.1A,V_{DD}=5 to 18V	-	0.7	2.0	Ω

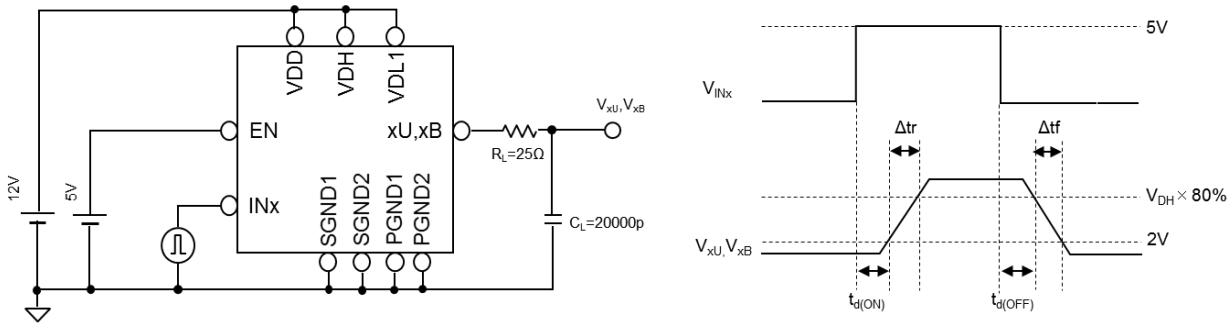
Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Diagnosis output voltage	Low level	V_{DIAG}	I_{DIAG}=0.5mA,V_{DD}=5 to 18V	-	-	0.5	V
Diagnosis output leakage current.	High level	I_{DIAG}	V_{DIAG}=6V,V_{DD}=5 to 18V	-	-	10	μA
V_{DH}drop detection		$V_{DH(UV)}$	V_{DD}=5 to 18V	V_{DD}+4	V_{DD}+4.5	V_{DD}+6	V
V_{DL}drop detection		$V_{DL(UV)}$	-	4	4.5	6	V
V_{DL}over voltage detection		$V_{DL(OV)}$	-	-	18	-	V
Delay time	V_{OUT}=L→H	$t_{d(ON)}$	V_{DD}=V_{DH}=V_{DL}=12V	-	0.21	0.4	μs
	V_{OUT}=H→L	$t_{d(OFF)}$	R_L=25Ω,C_L=20000pF	-	0.21	0.4	μs
Slew Rate (rise)		$dv/dt_{(ON)}$	-	-	75	-	V/μs
Slew Rate (fall)		$dv/dt_{(OFF)}$	-	-	75	-	V/μs
Propagation delay time	Same output	$\Delta t_{d(OFF-ON)1}$	-	-0.2	-	0.2	μs
	Top and bottom output	$\Delta t_{d(OFF-ON)2}$	-	-0.2	-	0.2	μs
Dead time		tdead	VDD=12V, Vth=2.0V	-	0.64	1	μs
Charge pump frequency		f_{osc}	V_{DD}=5 to 18V	30	55	80	kHz

Note 1 typical value if not specified is the 12V condition.

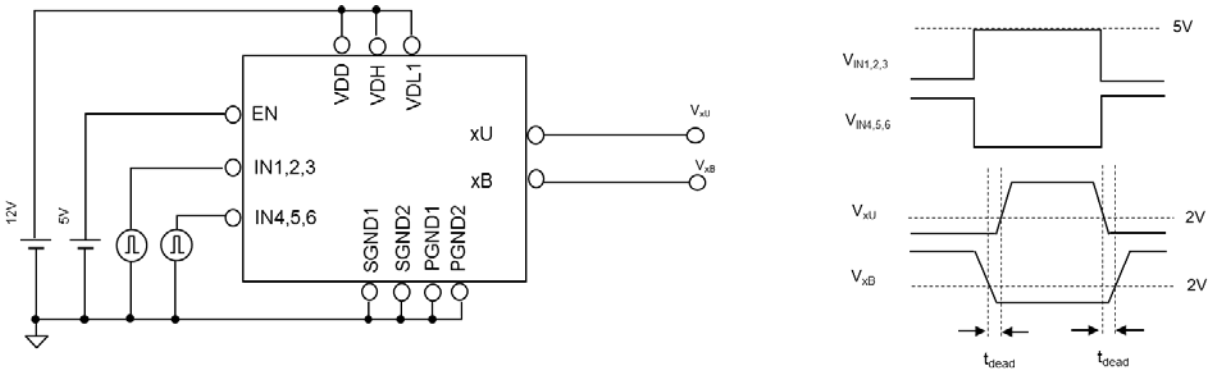
Note 2 D1.D2.D3=CRH01.R_{CP}=10Ω, Charge pump capacitance=2.2μF

Test circuit

●Slew Rate

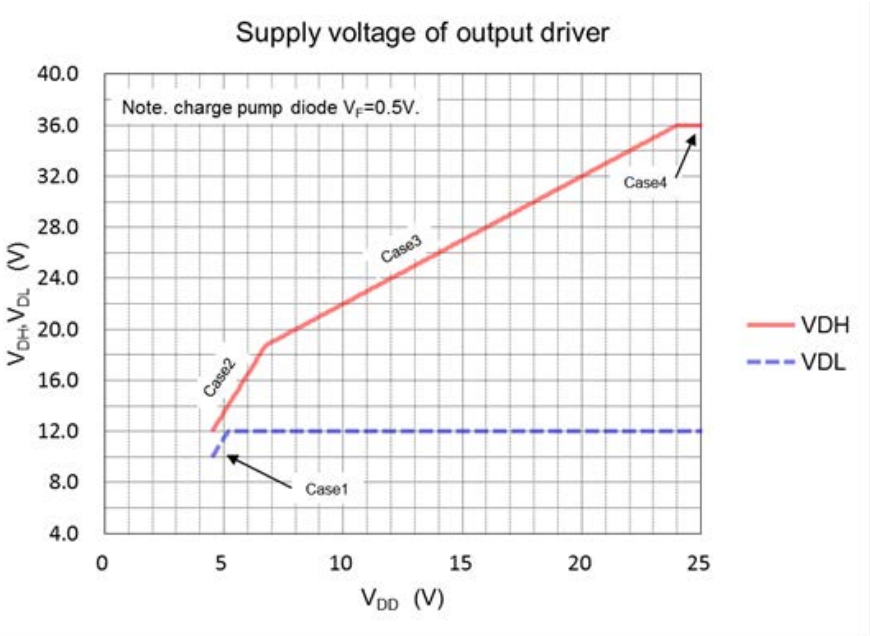


●Dead time



Note: INx: IN1,IN2,IN3,IN4,IN5,IN6 xU: UU,VU,WU xB: UB,VB,WB

Supply voltage for driver circuit.



This graph shows the relationship between the supply voltages. V_{DH} shows the power supply voltage characteristics of the high-side driver. V_{DL} shows the power supply voltage of the low-side driver. In order to ensure that the MOSFET drive voltage is at a low power supply voltage, the IC supplies power to the V_{DL} via a regulator from the V_{DH}. Both the V_{DH} and V_{DL} will exhibit the following characteristics.

Case1) $V_{DH} = 3 \times (V_{DD}-V_F)$
V_{DL} = VDH-2V
Case2) $V_{DH} = 3 \times (V_{DD}-V_F)$
V_{DL} = 12V
Case3) $V_{DH} = V_{DD}$ + 12V
V_{DL} = 12V
Case4) V_{DH} = 36V
V_{DL} = 12V

Note: The Overvoltage protection of the charge pump circuit operates under the following conditions.

Case1) $V_{DH} \geq V_{DD}$ + 12V(typ.) ,VDH(OV1)

Case2) $V_{DH} \geq$ 36V(typ.) ,VDH(OV2)

Truth table

EN	IN1 (IN2,3)	IN4 (IN5,6)	Charge pump Boost operation	Output voltage		DIAG1 output	DIAG2 output	Remarks
				UU output (VU,WU)	UB output (VB,WB)			
L	L	L	boost	L	L	H	L	All output off in V_{EN}=L.
	H	L		L	L	H	L	
	L	H		L	L	H	L	
	H	H		L	L	H	L	
H	L	L	boost	L	L	H	L	I/O is normal in V_{EN}=H.
	H	L		H	L	H	L	
	L	H		L	H	H	L	
	H	H		L(self-return)	L(self-return)	L(self-return)	L	Top and bottom short circuit input mode

●Abnormal output pin.(VDD short, GND short)

During both “turn on” and “turn off” of the driver, the output voltage is monitored. Depending on the judgment threshold after a mask time of 2.5μs (typ.), a diagnosis is made and a separate output signal will trigger a switch off of all drivers in the event of an “abnormal output”. The DMOS for 5kΩ pull down will be turned out and the DIAG1=L will be latched. (Latch will be reset in the event where EN signal changes from L to H)

●Diagnosis of the driver power supply voltage

<V_{DH} drop>
Judge $V_{DH} \leq V_{DD}$+5V(typ.) to be abnormal and output DIAG2=H.

<V_{DL} drop>
Judge $V_{DL} \leq$5V(typ.) to be abnormal and output DIAG2=H.

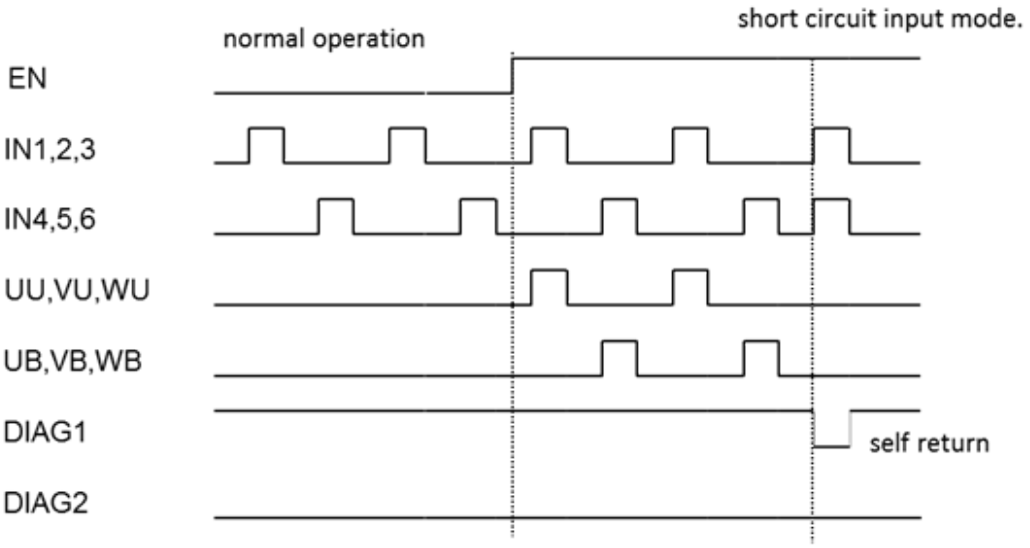
<V_{DL} over voltage>
Judge $V_{DL} \geq$18V(typ.)to be abnormal and output low side (UB,VB,WB)=L , and output DIAG2=H.

Output DIAG2=H (abnormal) when V_{DH} or V_{DL} voltage are abnormal.
Upon recover to the normal voltage, the DIAG2 output is automatically reset (DIAG2=L).

Note: Driver power supply (V_{DH} and V_{DL}) is boosted by the charge pump. Boost operation will start with V_{DD}> 4.5V. In order to prevent a malfunction, please enter the signal to IN1 to 6 after checking the DIAG2 = "L".

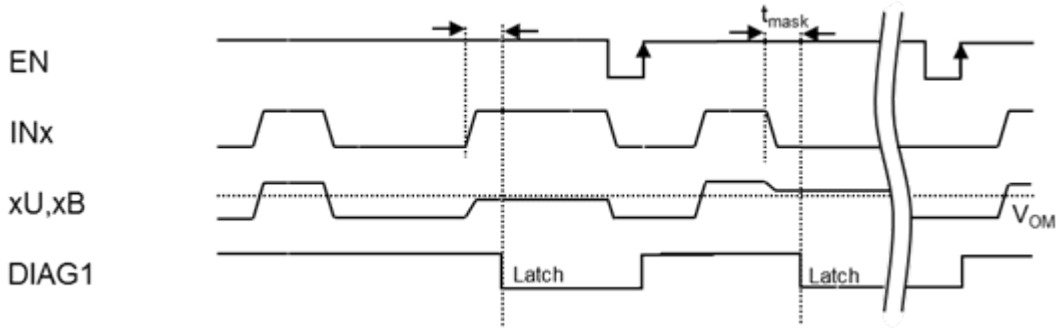
Timing chart

●Normal operation, Top and bottom short circuit input mode

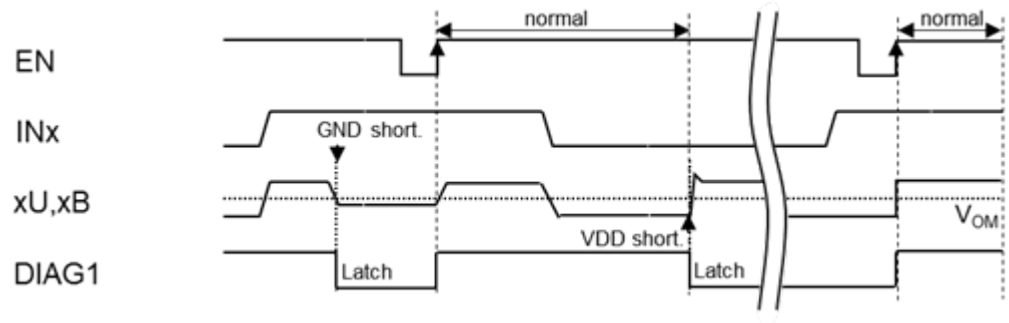


Detection and prevention of a simultaneous low-side and high-side input signal. The output will be L (NDMOS on-state) and DIAG1 will output an L (self-return upon absence of simultaneous signals)

●Abnormal of output pin.(VDD short, GND short)



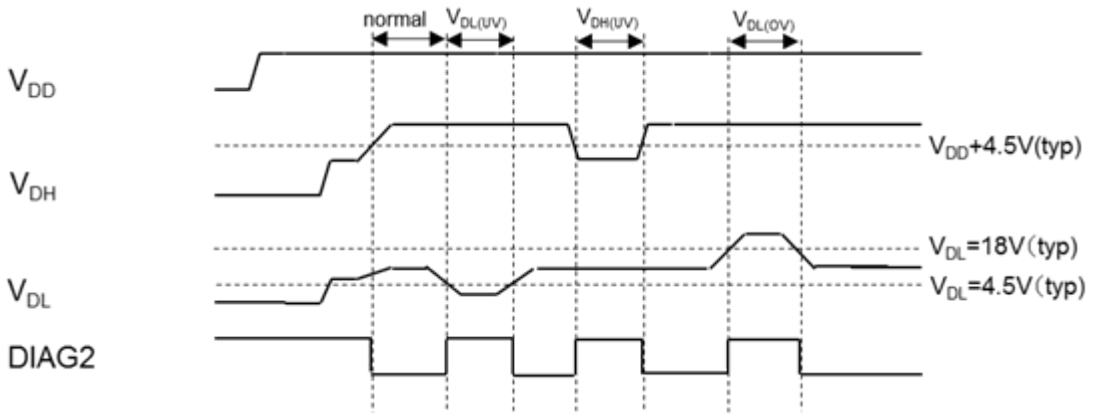
When a faulty output signal synchronizes with the input signal, the output is stopped after a mask time of 2.5μs, and outputs the DIAG1. All driver outputs are L level (Pulled-down via the 5kΩ internal resistor). DIAG1 output is latched at the L level, and then reset at the positive (return) signal of EN.



During a malfunction where an output signal is present during a stabilized input signal, the output is stopped immediately and DIAG1 is output. There is no mask time. All driver outputs are L level (Pulled-down via the 5kΩ internal resistor). DIAG1 output is latched at the L level, and reset upon the positive (return) signal of EN.

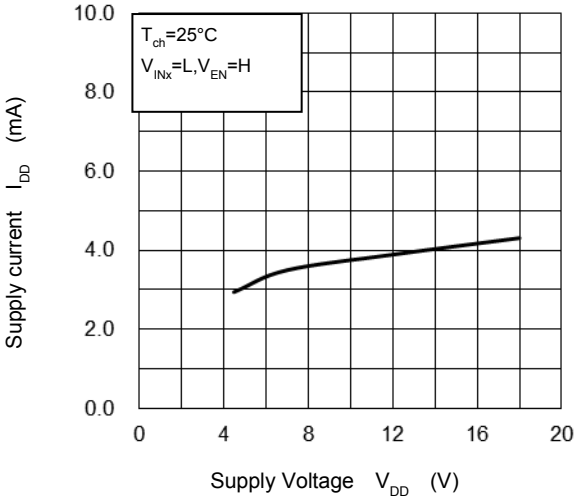
Note: INx: IN1,IN2,IN3,IN4,IN5,IN6 xU: UU,VU,WU xB: UB,VB,WB

●Diagnosis of the driver power supply voltage

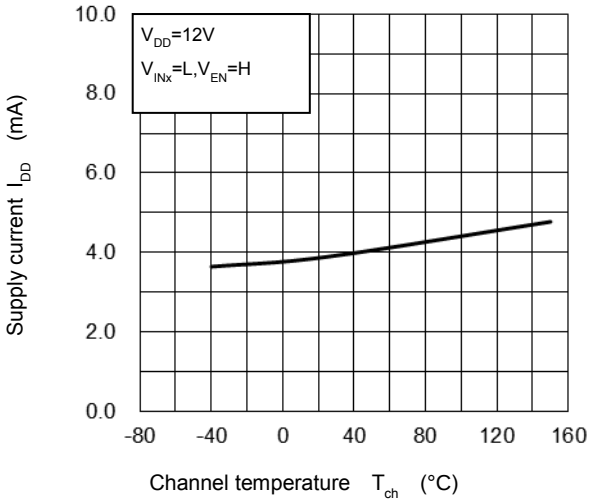


In an overvoltage condition of V_{DL}, UB, VB, WB will be the L state.

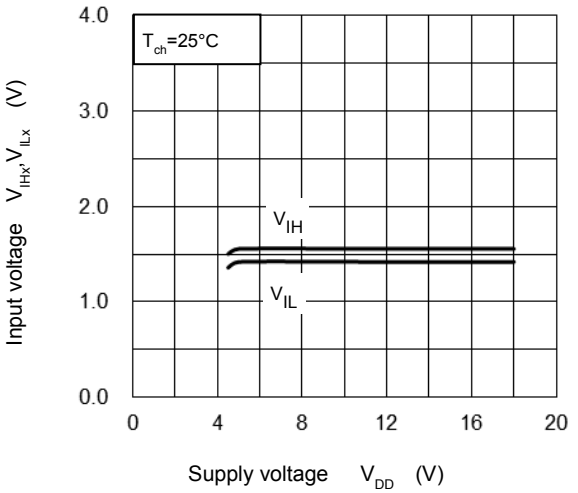
I_{DD}-V_{DD}



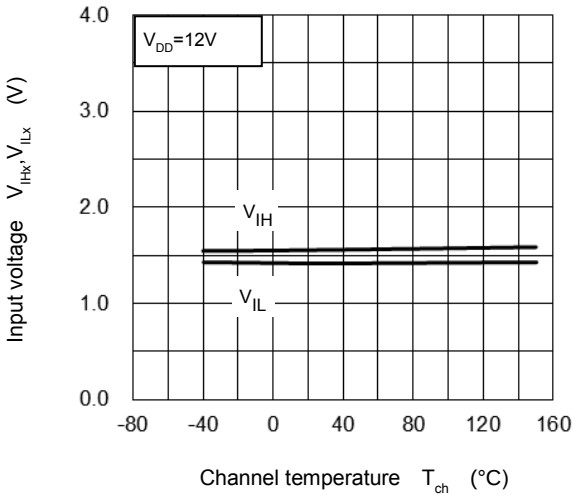
I_{DD}-T_{ch}



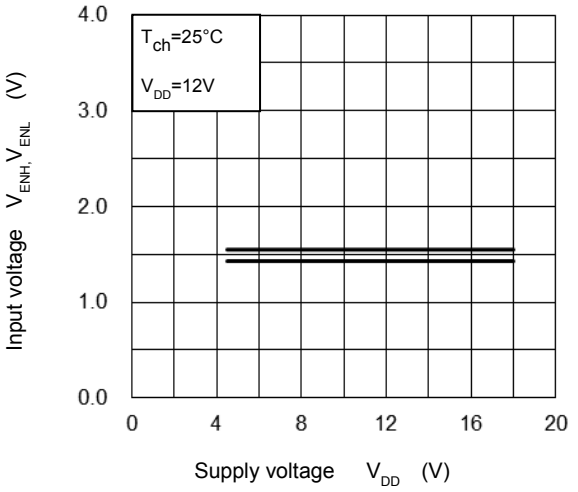
V_{IHx},V_{ILx}-V_{DD}



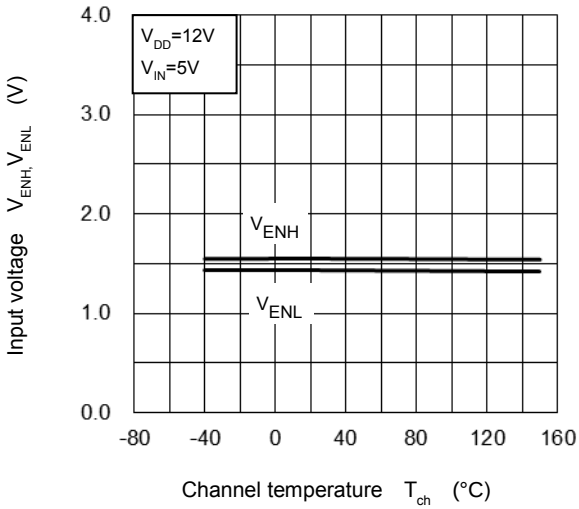
V_{IHx},V_{ILx}-T_{ch}



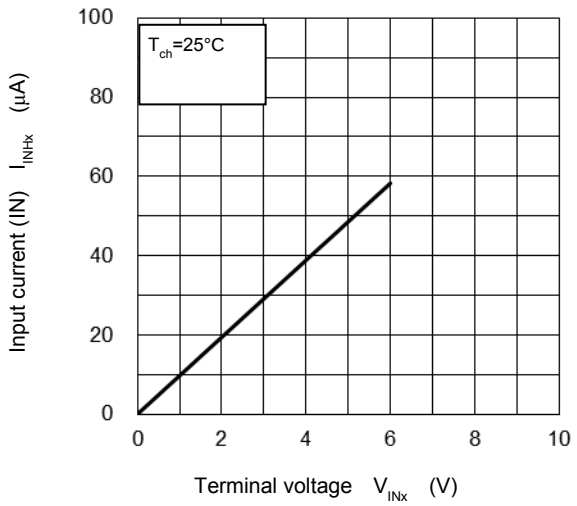
$V_{ENH,}V_{ENL}$-V_{DD}



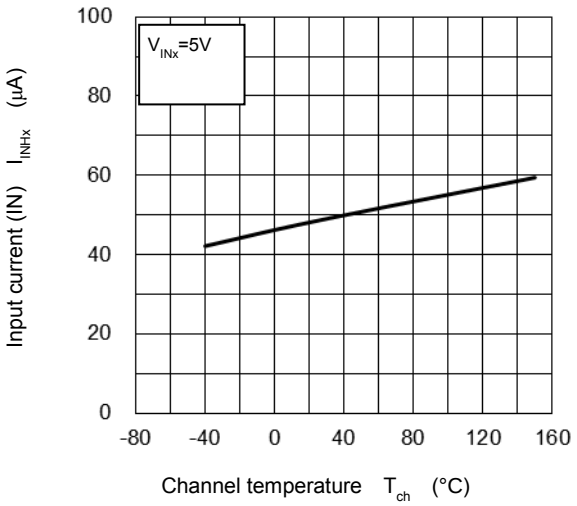
$V_{ENH,}V_{ENL}$-T_{ch}



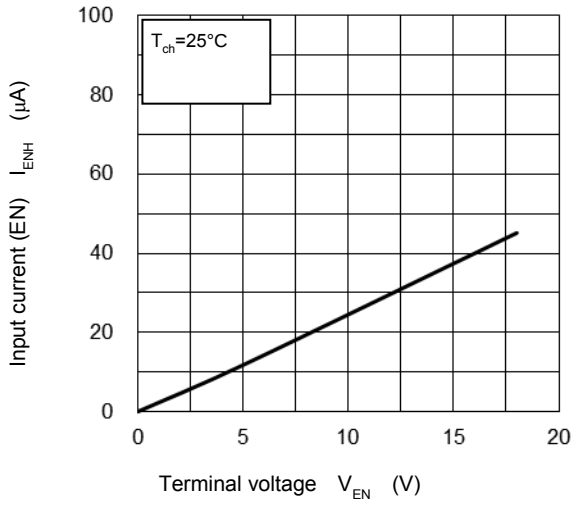
I_{INHx}-V_{INx}



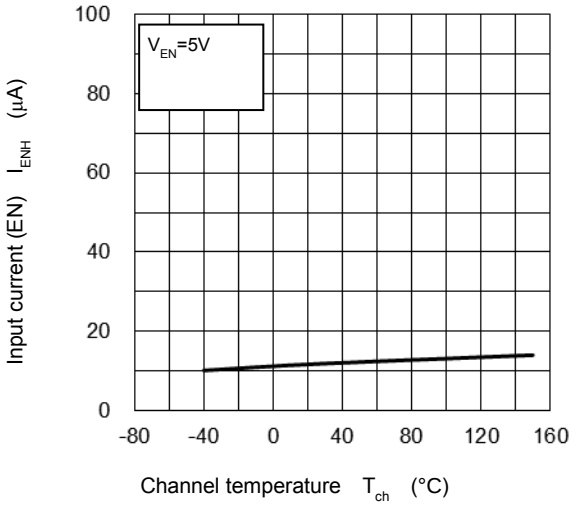
I_{INHx}-T_{ch}



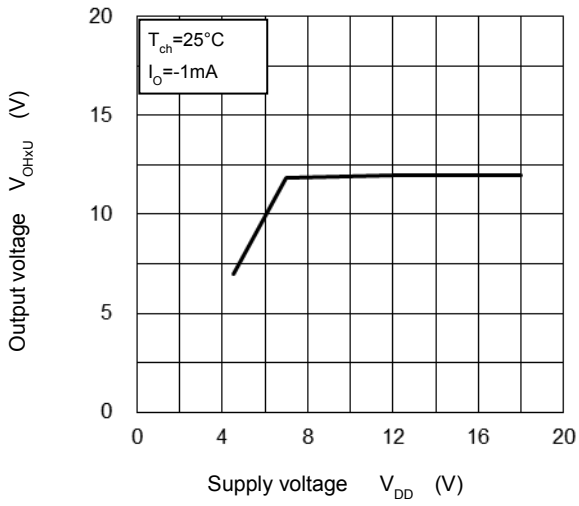
I_{ENH}-V_{EN}



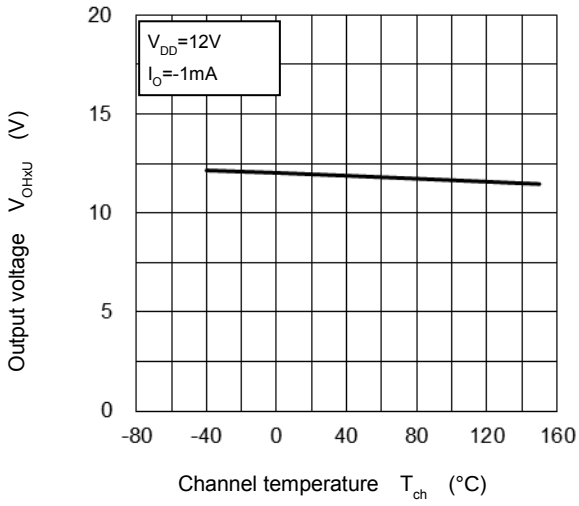
I_{ENH}-T_{ch}



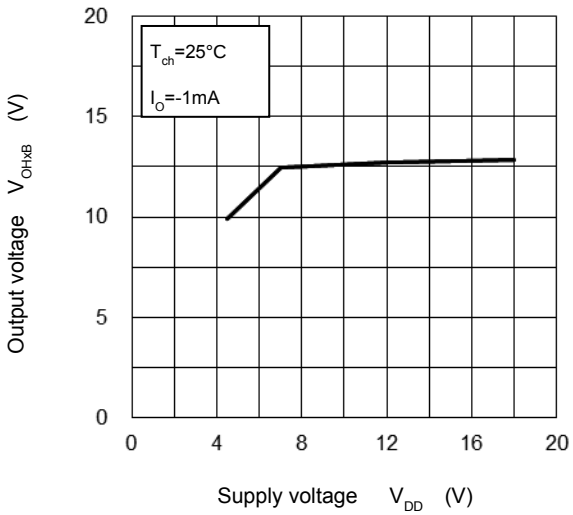
V_{OHxU}-V_{DD}



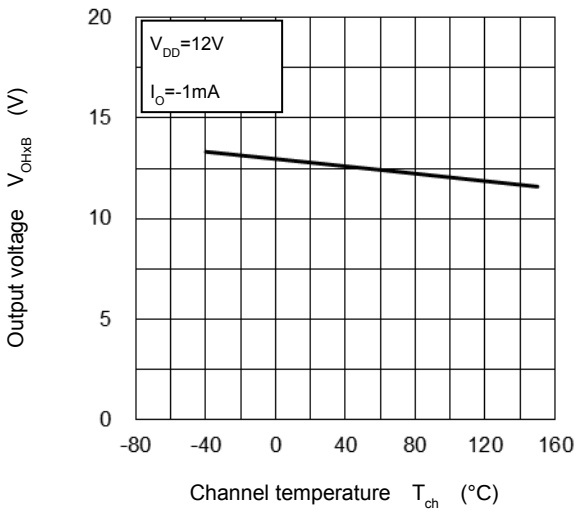
V_{OHxU}-T_{ch}



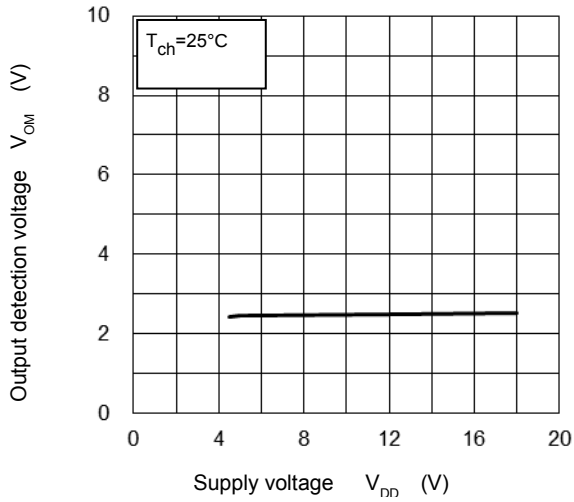
V_{OHxB}-V_{DD}



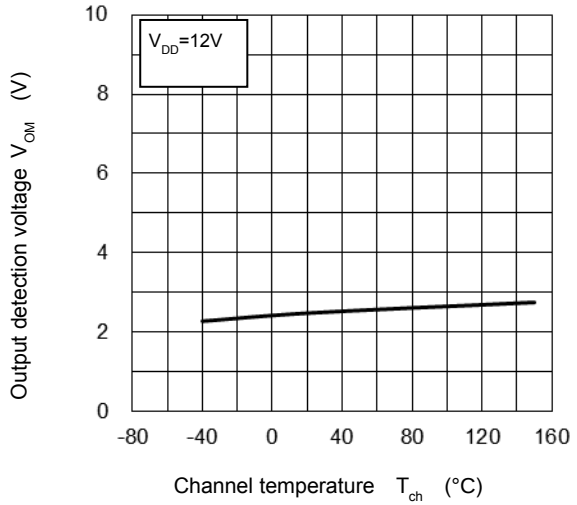
V_{OHxB}-T_{ch}



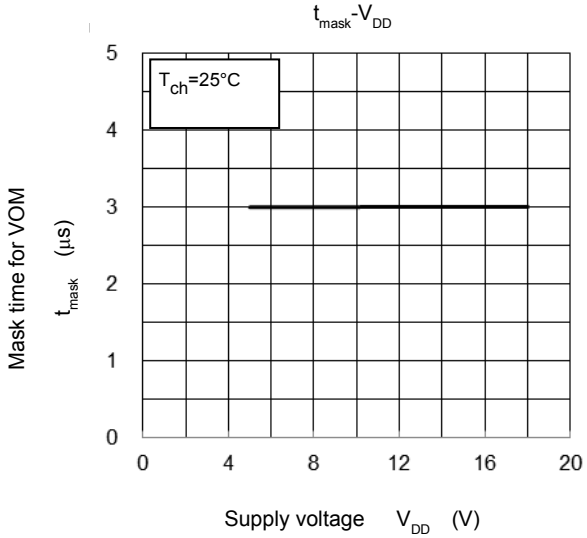
V_{OM}-V_{DD}



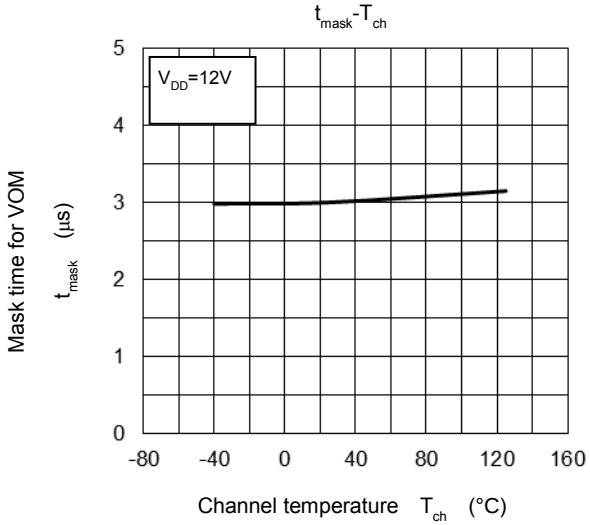
V_{OM}-T_{ch}



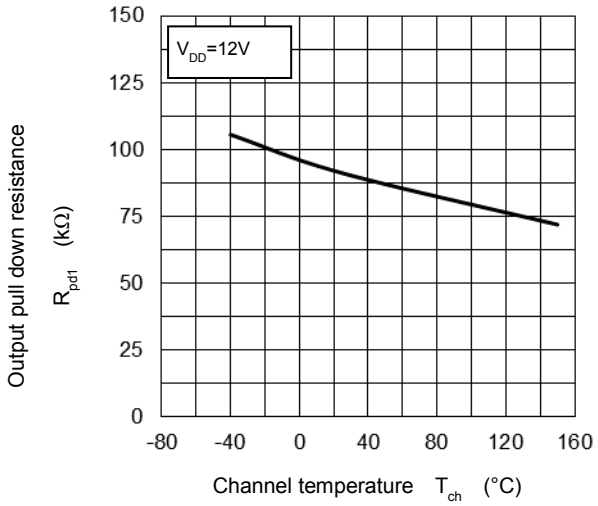
t_{mask}-V_{DD}



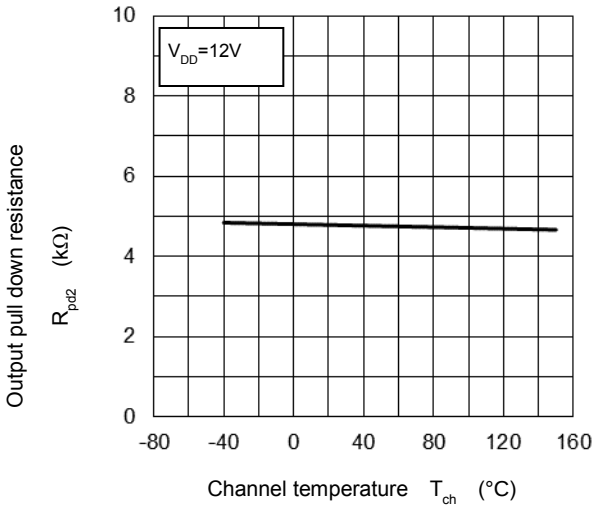
t_{mask}-T_{ch}



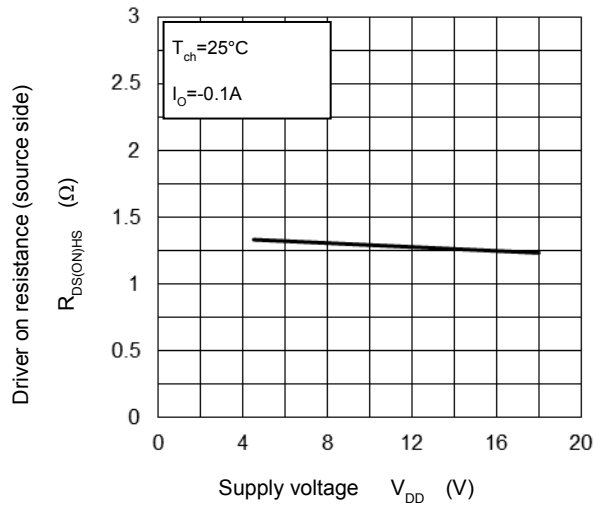
R_{pd1}-T_{ch}



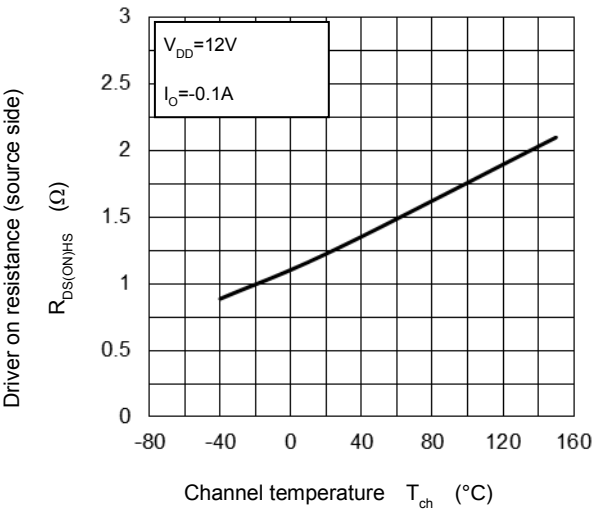
R_{pd2}-T_{ch}



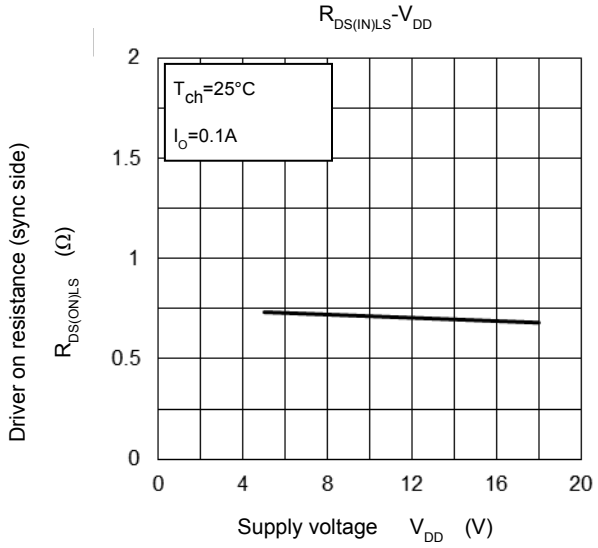
$R_{DS(ON)HS}$-V_{DD}



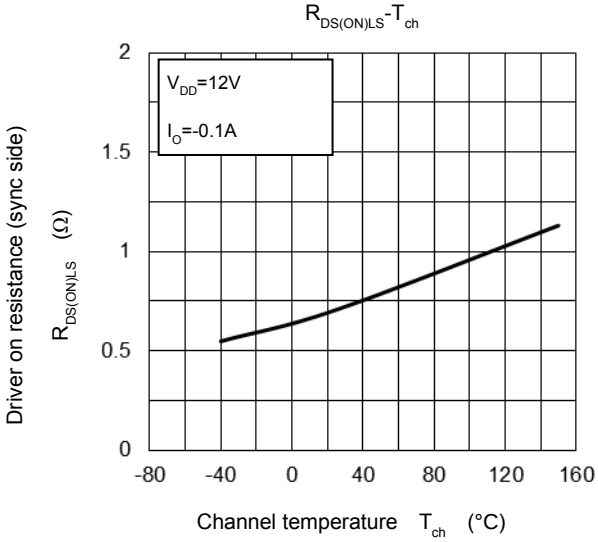
$R_{DS(ON)HS}$-T_{ch}



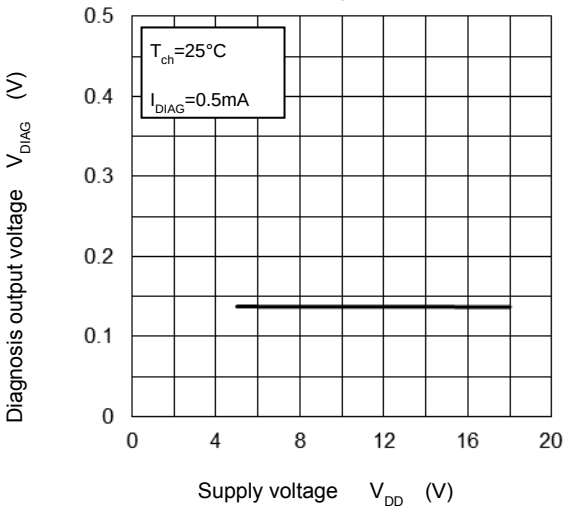
$R_{DS(IN)LS}$-V_{DD}



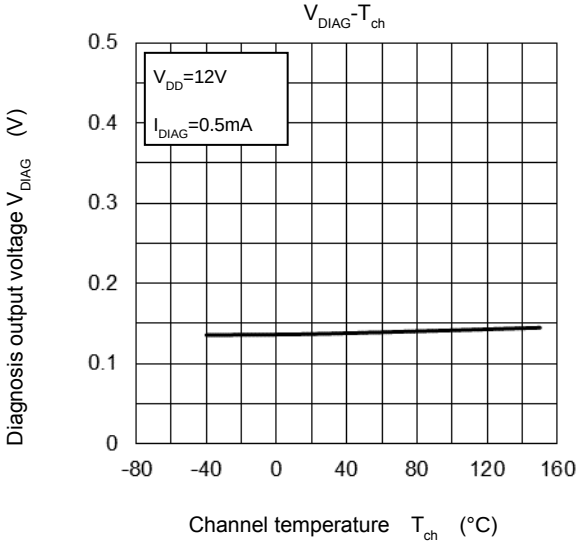
$R_{DS(ON)LS}$-T_{ch}



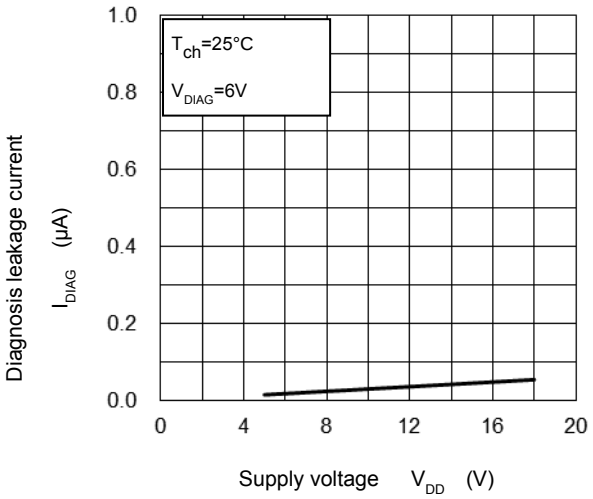
V_{DIAG}-V_{DD}



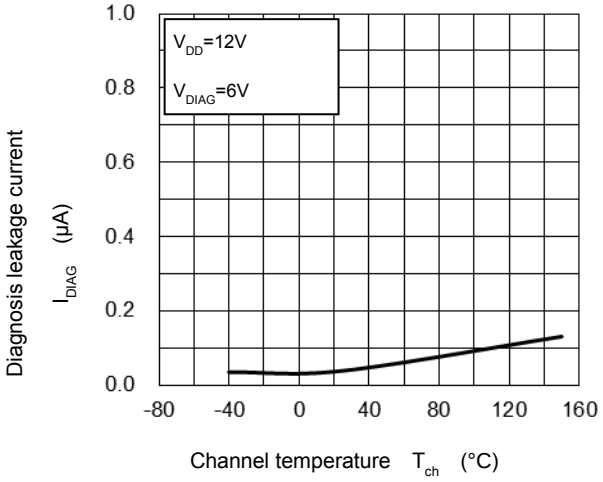
V_{DIAG}-T_{ch}



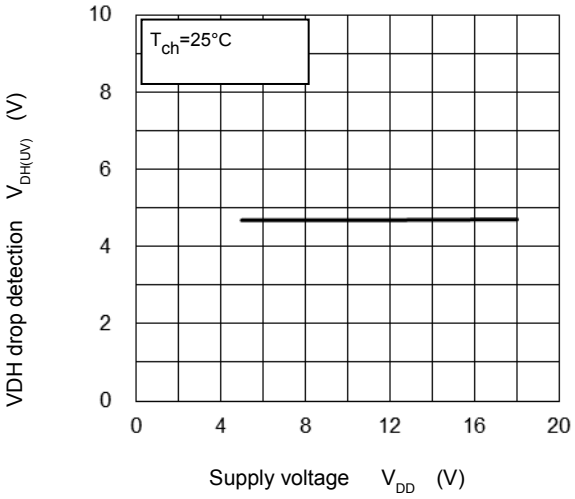
I_{DIAG}-V_{DD}



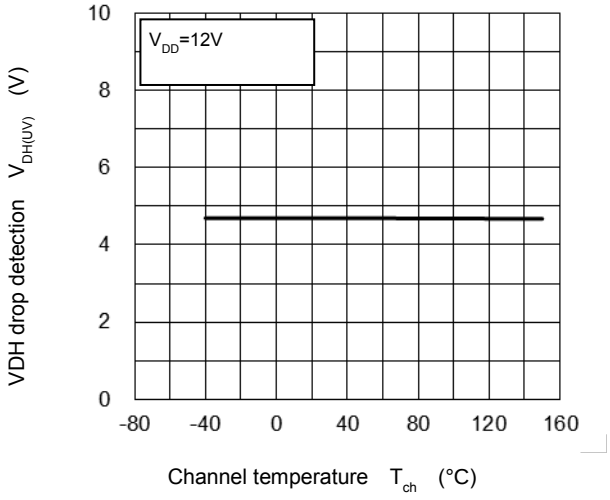
I_{DIAG}-T_{ch}



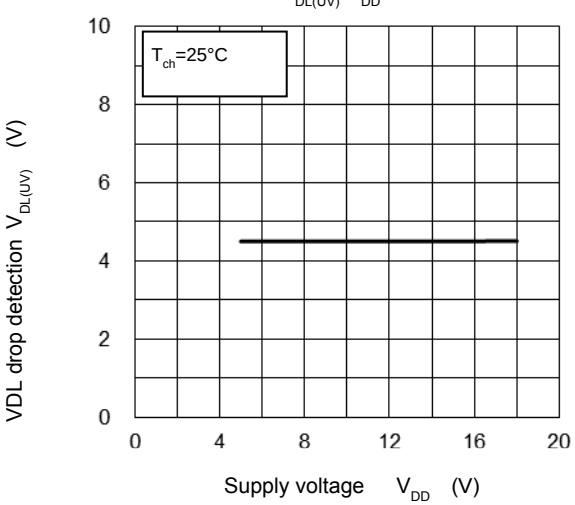
$V_{DH(UV)}$-V_{DD}



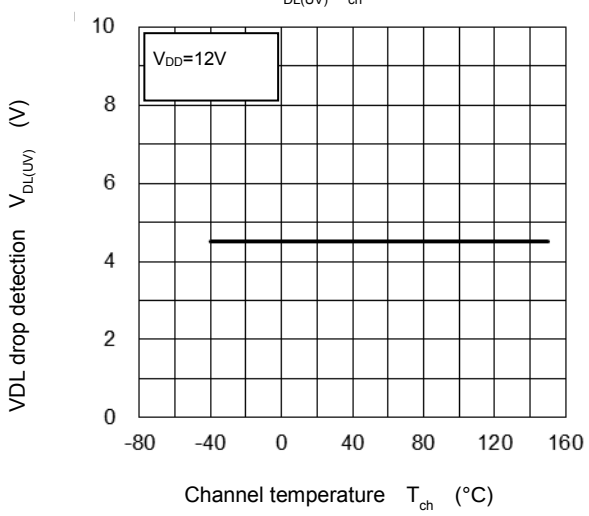
$V_{DH(UV)}$-T_{ch}



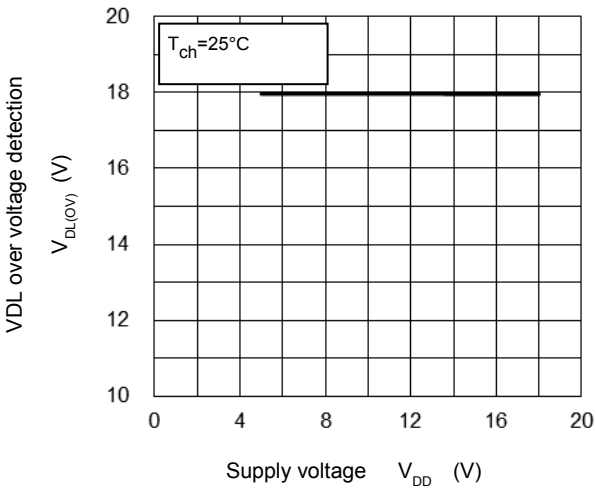
$V_{DL(UV)}$-V_{DD}



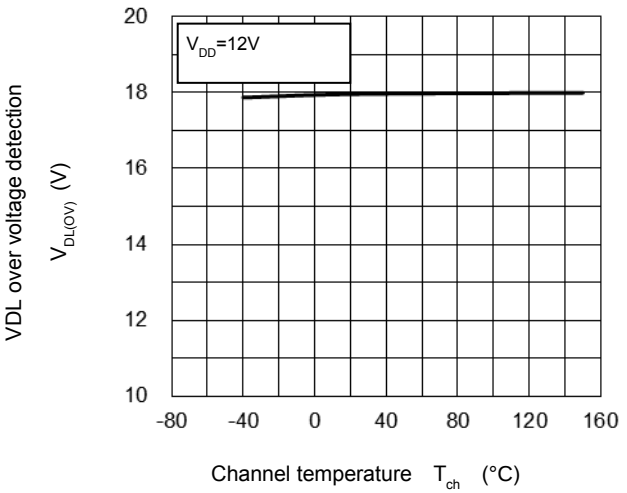
$V_{DL(UV)}$-T_{ch}



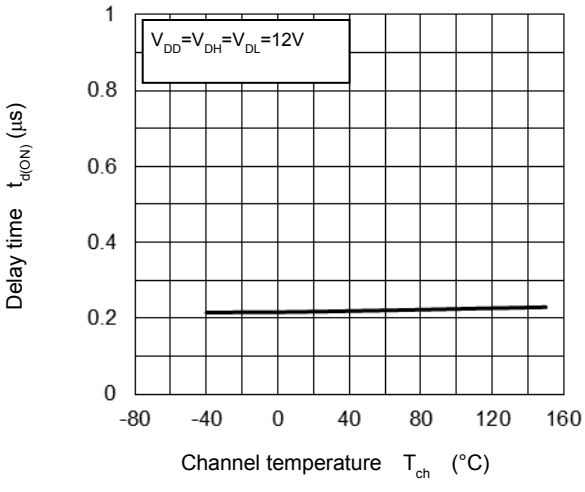
$V_{DL(OV)}$-V_{DD}



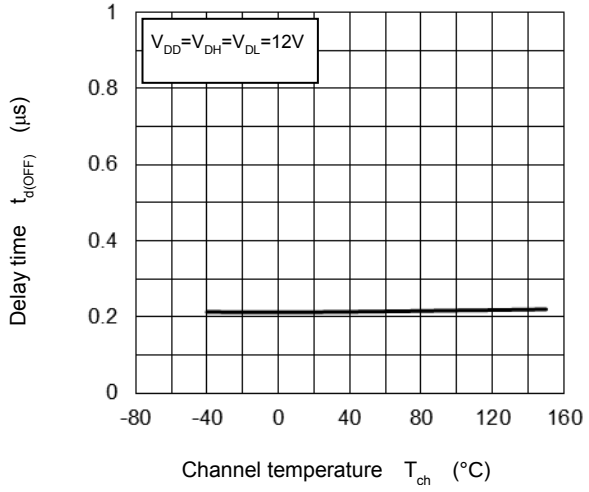
$V_{DL(OV)}$-T_{ch}



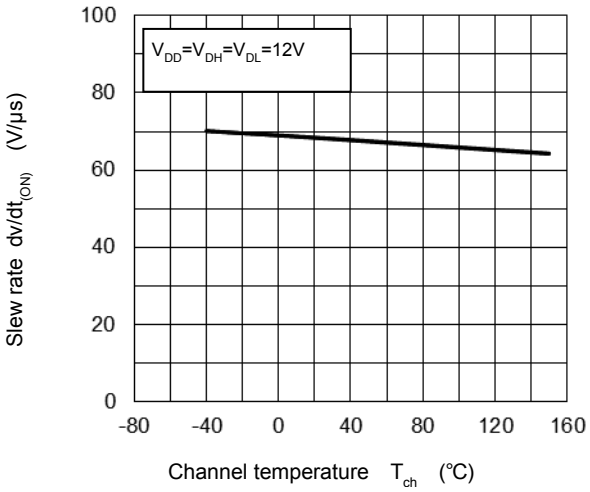
$t_{d(ON)}$-T_{ch}



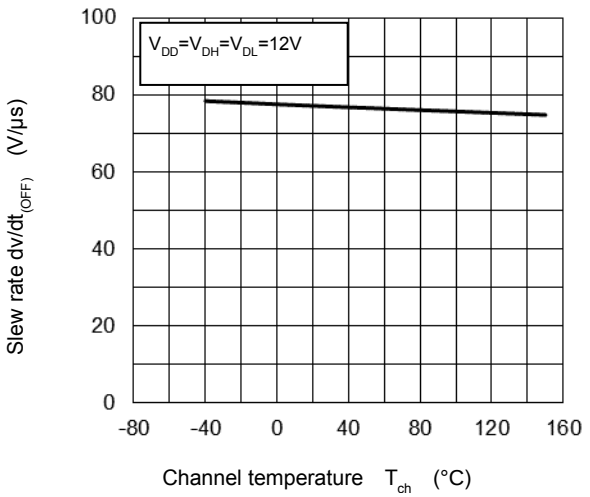
$t_{d(OFF)}$-T_{ch}



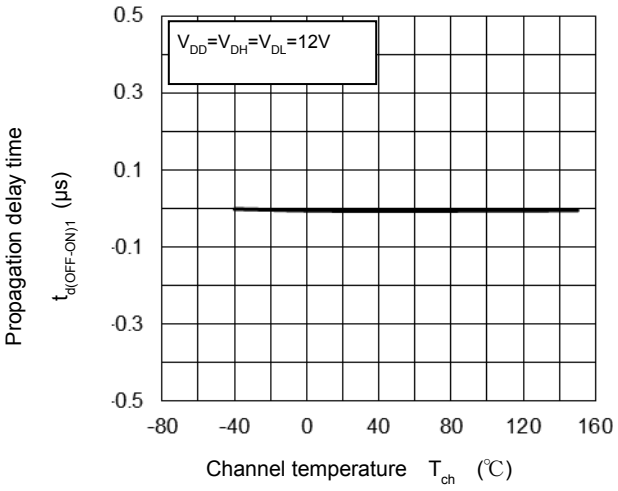
$dv/dt_{(ON)}$-T_{ch}



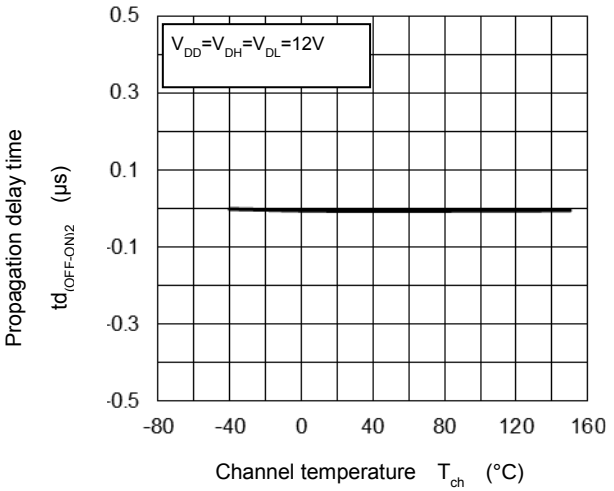
$dv/dt_{(OFF)}$-T_{ch}



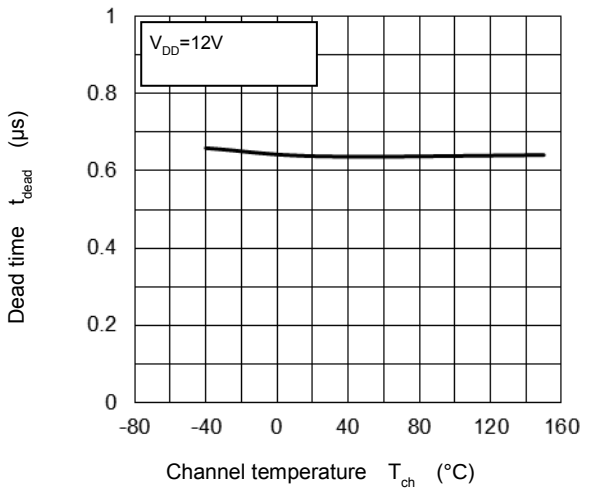
$\Delta t_{d(OFF-ON)1}$-T_{ch}

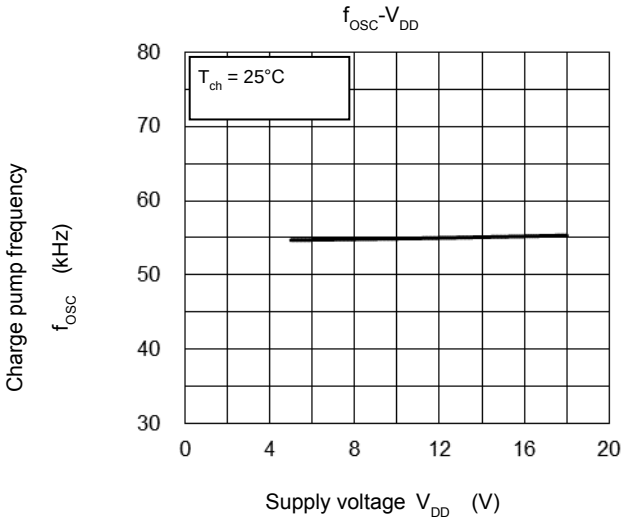


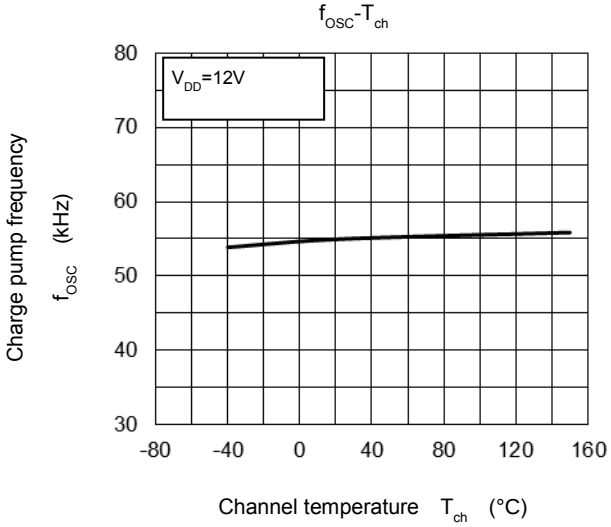
$\Delta t_{d(OFF-ON)2}$-T_{ch}



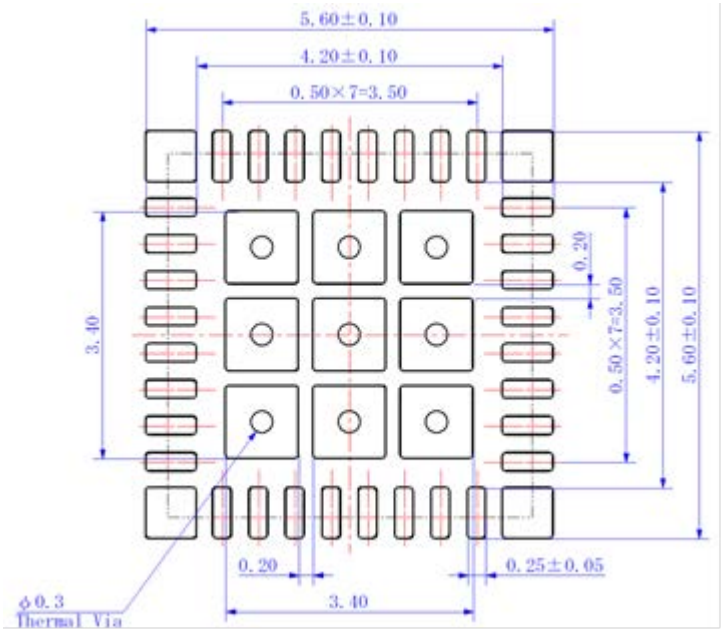
t_{dead}-T_{ch}




f_{OSC}-V_{DD}
T_{ch} = 25°C
Charge pump frequency
f_{OSC} (kHz)
80
70
60
50
40
30
0
4
8
12
16
20
Supply voltage V_{DD} (V)


f_{OSC}-T_{ch}
V_{DD}=12V
Charge pump frequency
f_{OSC} (kHz)
80
70
60
50
40
30
-80
-40
0
40
80
120
160
Channel temperature T_{ch} (°C)

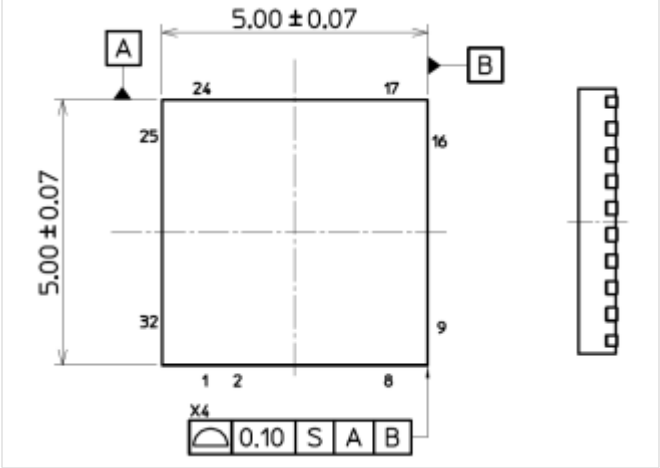
Reference land pattern

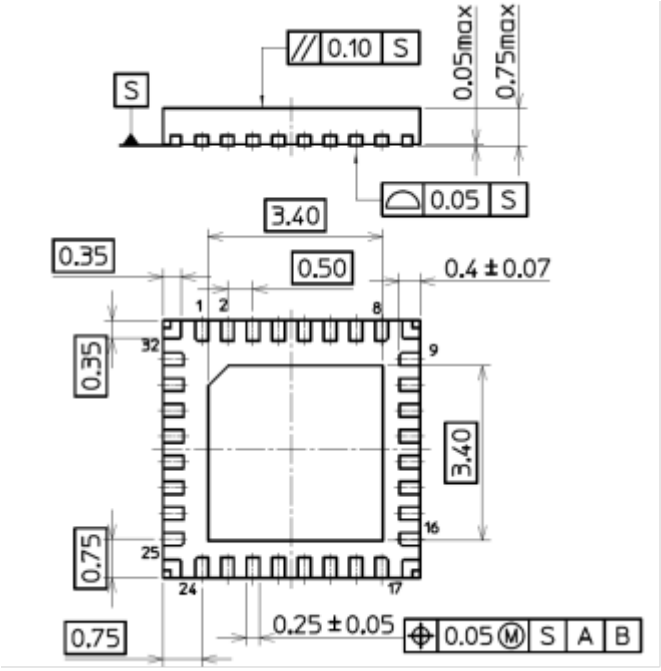


Note: Since the metal exposed area on the back of IC has a role of heat dissipation, please carry out a pattern design in consideration of a thermal design. Moreover, it recommends that an unindicated name corner pin prepares a pattern in consideration of mounting nature.
Since the metal exposed area on the back of IC is electrically connected with the chi back, please insulate or ground.

Package Dimensions

unit : mm





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