32-bit RISC Microcontroller

TXZ Family

Reference Manual
Long Term Timer
(LTTMR-A)

Revision 1.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

LTTMR	Long Term Timer

1. Outlines

Long term timer (LTTMR) is a 16-bit timer which sets an interval time to start up CPU frequently.

Function category	Function	Description
Timer	Interval timer	- Clock source: Internal High speed oscillator 2 (f_{IHOSC2} = 10 MHz) - Settable time range: 0.1 μs to 6553.5 μs - Interrupt: LTTMR interrupt generation

2. Configuration

The configuration of the long term timer is as follows.

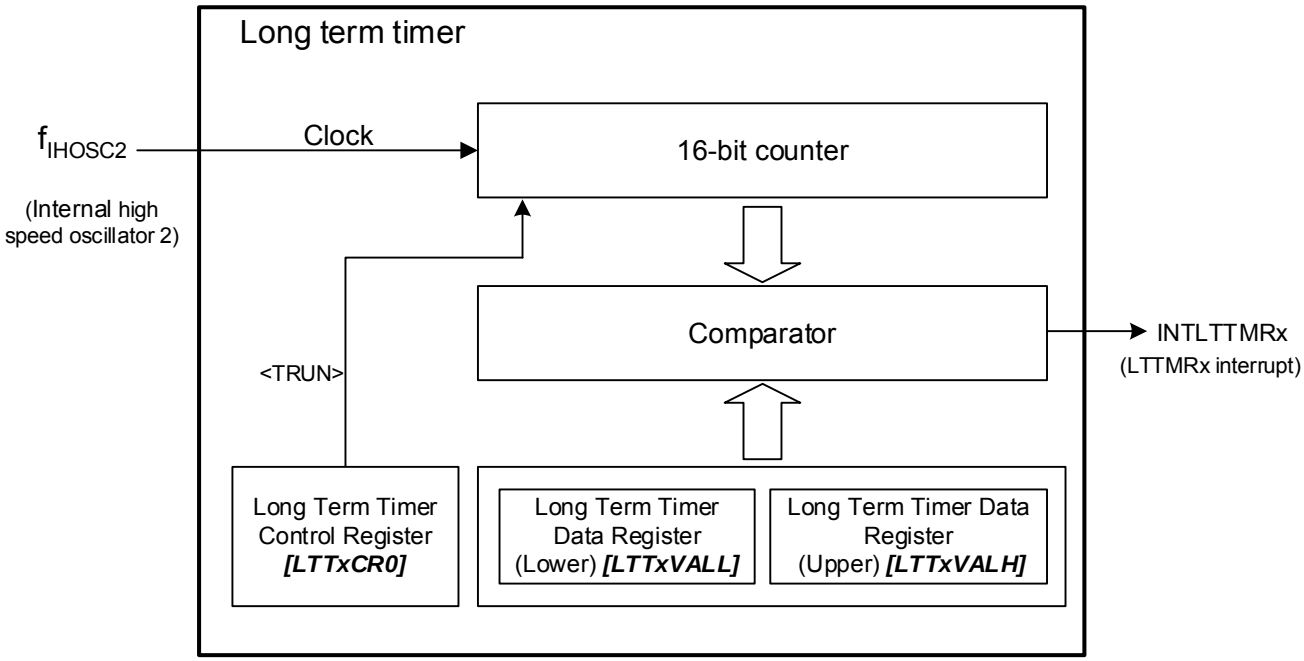

Figure 2.1 Configuration of Long term timer

Table 2.1 List of Long term timer signals

No.	Symbol	Signal name	I/O	Reference manual
1	f_{IHOSC2}	Clock of the internal high speed oscillator 2	Input	Clock Control and Operation Mode
2	INTLTTMRx	LTTMRx interrupt	Output	Exception

3. Function and Operation

The LTTMR generates an interrupt at the constant period which can be set.
The LTTMR consists of a 16-bit counter, a comparator, and a setting register, and counts up with the clock (f_{IHOSC2}) generated from the internal high speed oscillator 2.

The internal high speed oscillator 2 (IHOSC2) which connects to the count clock pin should be set to the oscillation enable.
For the details, refer to "Clock Control and Operation Mode" of Reference manual.

3.1. 16-bit Counter

The 16-bit counter operates with the clock which is generated by the internal high speed oscillator 2.

3.1.1. Strat and Stop of Counter

The 16-bit counter starts counting when ***[LTTxCR0]***<TRUN>=1, stops counting and clears the counter when ***[LTTxCR0]***<TRUN>= 0.

3.1.2. Counter Clear

The 16-bit counter is cleared by the following conditions.

(a) When the count value matches the value in the Long Term Timer Data Register (***[LTTxVALL]*** and ***[LTTxVALH]***):

If ***[LTTxCR0]***<TRUN>= 1 is set, the counter is cleared when the count value matches the value of the Long Term Timer Data Register.

(b) When the counter stops (***[LTTxCR0]***<TRUN> = 0):

If ***[LTTxCR0]***<TRUN> = 0 is set, the counter stops and it is also cleared.

Note: Before ***[LTTxCR0]***<TRUN> = 0 is set, the reception of an interrupt is disabled in NVIC.

For the details, refer to "3.4. Operation Timing".

3.2. Comparator

The comparator compares the 16-bit counter value with the value of the Long Term Timer Register (***[LTTxVALL]*** and ***[LTTxVALH]***). When these values match, INTLTTMRx (LTTMRx interrupt) is generated.

3.3. Interrupt

INTLTTMRx interrupt is generated when the 16-bit counter value matches the value of the Long Term Timer Data Register (***[LTTxVALH]*** and ***[LTTxVALL]***).

The interrupt period is set to the Long Term Timer Data Register (***[LTTxVALH]*** and ***[LTTxVALL]***). The setting value is calculated by the following formula.

- **Interrupt period = (1 / f_{IHOSC2}(10MHz)) × ((*[LTTxVALH]* × 256) + *[LTTxVALL]* + 1)**

  Note: 0x0000 is inhibited as the setting value of ***[LTTxVALH]*** and ***[LTTxVALL]***.

Examples of the setting values of the interrupt period are shown in the following table.

Table 3.1 Examples of the setting values of the interrupt period

Interrupt period (µs)	Interrupt frequency (kHz)	Long Term Timer Data Register setting value	
		[LTTxVALH]	*[LTTxVALL]*
6553.5	0.15	0xFF	0xFE
5000.0	0.20	0xC3	0x4F
4000.0	0.25	0x9C	0x3F
3000.0	0.33	0x75	0x3F
2000.0	0.50	0x4E	0x1F
1000.0	1.00	0x27	0x0F
500.0	2.00	0x13	0x87
100.0	10.00	0x03	0xE7
50.0	20.00	0x01	0xF3

3.4. Operation Timing

Figure 3.1 shows the timing where the counter value matches.
If ***[LTTxCR0]***<TRUN> = 1 is set, the 16-bit counter starts its count after 2 to 3 count clock cycles. When the count value matches the data register value (n), INTLTTMRx (LTTMRx interrupt) is generated. The 16-bit counter is cleared to "0" at the next cycle, and the count continues. After that, whenever the count value becomes "n", INTLTTMRx (LTTMRx interrupt) is generated.

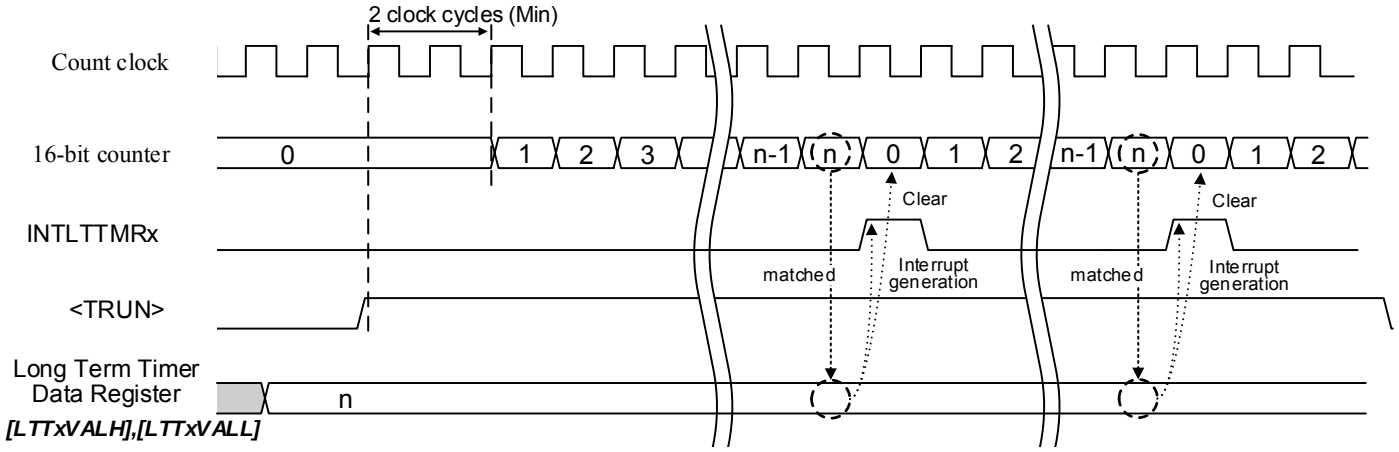

Figure 3.1 Counter value comparison procedure

Figure 3.2 shows the timing of the counter stop.
If ***[LTTxCR0]***<TRUN> = 1 is set, the 16-bit counter starts its count after 2 to 3 count clock cycles. If ***[LTTxCR0]***<TRUN> = 0 is set during the count operation, the 16-bit counter is cleared to "0" asynchronously, and the counter stops.

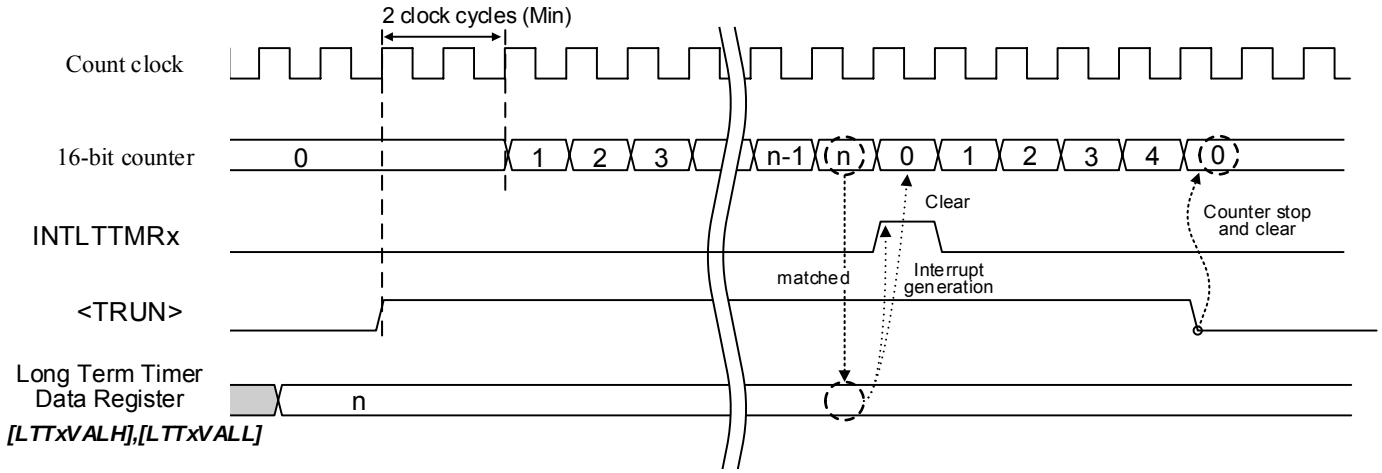

Figure 3.2 Counter stop procedure

4. Registers

4.1. List of Registers

The registers and their addresses are shown as follows.

Peripheral function		Channel/Unit	Base address
			TYPE 1
Long term timer	LTTMR	ch0	0x4003FF00

Register name		Base address (Base +)
Long Term Timer Control Register	***[LTTxCR0]***	0x0000
Long Term Timer Data Register (Lower)	***[LTTxVALL]***	0x0001
Long Term Timer Data Register (Upper)	***[LTTxVALH]***	0x0002

Note: The register access should be done with Byte unit.

4.2. *[LTTxCR0]* (Long Term Timer Control Register)

Bit	Bit Symbol	After Reset	Type	Description
7:2	-	0	R	Read as "0".
1	TRUN	0	R/W	Setting of 16-bit counter operation 0: Count stop and clear 1: Count operation
0	-	0	R/W	Write as "0".

4.3. *[LTTxVALL]* (Long Term Timer Data Register (Lower))

Bit	Bit Symbol	After Reset	Type	Description
7:0	TMRVALL[7:0]	0x00	R/W	Lower Byte which should be compared with the value of the 16-bit counter.

Note: The setting should be done during ***[LTTxCR0]***<TRUN>= 0.

4.4. *[LTTxVALH]* (Long Term Timer Data Register (Upper))

Bit	Bit Symbol	After Reset	Type	Description
7:0	TMRVALH[7:0]	0x00	R/W	Upper Byte which should be compared with the value of the 16-bit counter.

Note: The setting should be done during ***[LTTxCR0]***<TRUN>= 0.

5. Example of Usage

Examples of the usage are shown in the followings.

(1) Start-up

[CGOSCCR]		Oscillation setting of the internal high speed oscillator 2 (IHOSC2)
NVIC	CLRENA<n> = 1	LTTMR interrupt is disabled.

	7	6	5	4	3	2	1	0	
[LTTxCR0]	X	X	X	X	X	X	0	0	Up-counter stops.
[LTTxVALL]	*	*	*	*	*	*	*	*	Interval time (Lower) is set.
[LTTxVALH]	*	*	*	*	*	*	*	*	Interval time (Upper) is set.

NVIC	SETENA<n> = 1	LTTMR interrupt is enabled.

[LTTxCR0]	X	X	X	X	X	X	1	0	Up-counter starts up.

Note: X: Don't care
n: LTTMRx interrupt number

(2) Interval time change

NVIC	CLRENA<n> = 1	LTTMR interrupt is disabled.
NVIC	CLRPEND<n> = 1	Interrupt suspension is cleared.

	7	6	5	4	3	2	1	0	
[LTTxCR0]	X	X	X	X	X	X	0	0	Up-counter stops.
[LTTxVALL]	*	*	*	*	*	*	*	*	Interval time (Lower) is set.
[LTTxVALH]	*	*	*	*	*	*	*	*	Interval time (Upper) is set.

NVIC	SETENA<n> = 1	LTTMR interrupt is enabled.

[LTTxCR0]	X	X	X	X	X	X	1	0	Up-counter starts up.

Note: X: Don't care
n: LTTMRx interrupt number

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2018-01-30	First release
1.1	2018-07-30	-Conventions Modified explanation of trademark 4.1.List of Registers Deleted: "TYPE2" of Base address

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