32-Bit RISC Microcontroller

TXZ Family

Reference Manual
Voltage Detection Circuit
(LVD-C)

Revision 2.0

2018-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related Document

Document name
Exception
Product Information
Power Supply and Reset Operation

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

The Flash memory uses the Super Flash® technology under the license of Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviation

Some of abbreviations used in this document are as follows:

INT	Interrupt
LVD	Voltage Detection Circuit
POR	Power On Reset Circuit

1. Outlines

The main functions of the voltage detection circuit (LVD) are shown in the following table.

Function category	Function	Description	Note
Supply voltage detection function	Reset output	Reset is generated at the set detection voltage or less.	Selectable from the reset and an interrupt.
	Interrupt request	An interrupt request is generated at the set detection voltage or less.	
	Monitor	The status can be monitored using a status register for the voltage detection.	—
	Detected voltage selection	The selection out of 7 kinds is possible.	Supported for NORMAL/IDLE/STOP1 modes and STOP2 mode

2. Configuration

The voltage detection circuit consists of LVDN sub-circuit for NORMAL/IDLE/STOP1 modes and LVDS sub-circuit for STOP2 mode. Each sub-circuit has a reference voltage generator, a detection voltage selector, a comparator, and control registers.

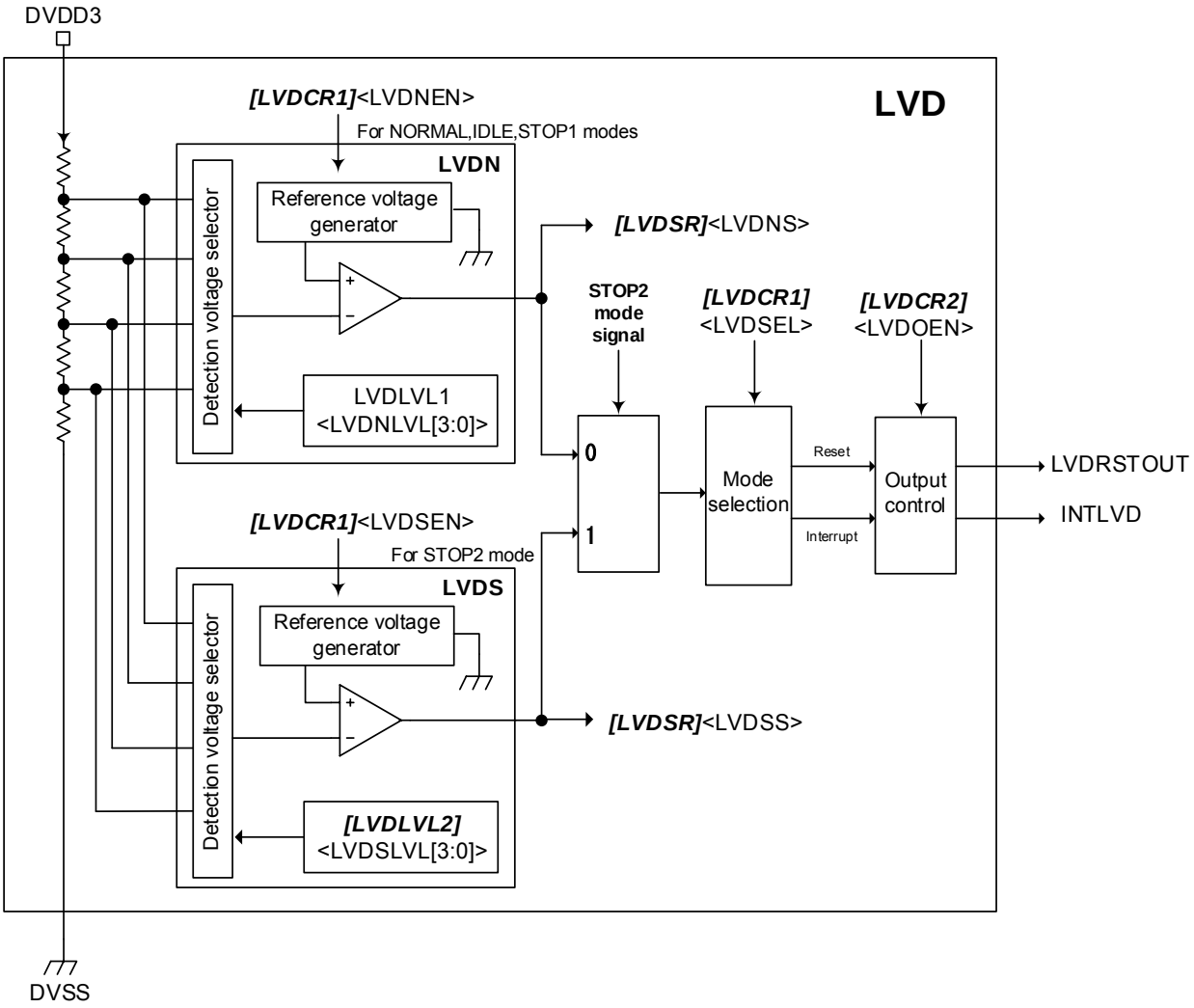


Figure 2.1 Block diagram

Table 2.1 List of signals

No.	Symbol	Signal name	I/O	Related Reference manual
1	DVDD3	Detected power supply pin	Input	Product Information
2	LVDRSTOUT	LVD reset output	Output	Power Supply and Reset Operation
3	INTLVD	LVD interrupt request signal	Output	Exception

3. Function and Operation

The voltage detection circuit observes the voltage of DVDD3 pin. It compares the reference voltage generated by the reference voltage generator and the output voltage of the detection voltage selector which selects one of the detection voltages generated by using the DVDD3 voltage. According to the comparison result, the reset or the interrupt request is generated by the output control circuit.

When the power supply starts up, the reset signal (LVDRSTOUT) is asserted while the DVDD3 voltage is lower than the reset-release voltage. After the DVDD3 voltage exceeds the reset-release voltage, the reset is deasserted.

3.1. Voltage Detection Circuit

The voltage detection circuit has LVDN circuit for NORMAL/IDLE/STOP1 modes and LVDS circuit for STOP2 mode. One circuit switches with another at the transition of the corresponding mode.

(1) LVDN

The LVDN circuit has the functions of the voltage detection and the reset release.

The voltage detection function generates the reset signal or the interrupt request according to the setting in ***[LVDCR1]***<LVDSEL> when the DVDD3 voltage decreases and becomes lower than the set value in ***[LVDLVL1]***<LVDNLVL>. The reset-release function deasserts the reset signal (when the reset signal is selected) after the voltage increases and exceeds the set voltage in ***[LVDLVL1]***<LVDNLVL>. When the interrupt request is selected, the reset-release function does not generate the interrupt request.

(2) LVDS

The LVDS circuit has the function of the voltage detection only. It does not have the reset-release function.

The voltage detection function generates the reset signal or the interrupt request according to the setting in ***[LVDCR1]***<LVDSEL> when the DVDD3 voltage decreases and become lower than the set value in ***[LVDLVL2]***<LVDSLVL>.

The status of the DVDD3 voltage can be monitored by using ***[LVDSR]***<LVDNS><LVDSS> in the voltage detection circuit, even though the generation of the reset signal or the interrupt request is disabled by ***[LVDCR2]***<LVDOEN>. Even in NORMAL mode, the status <LVDSS> of STOP2 mode can be checked.

3.2. Setting

3.2.1. Voltage Detection Control

When the voltage detection circuit is used, the bit for the voltage detection control should be set to Enable.

When LVDN is used, ***[LVDCR1]***<LVDNEN>=1 should be set. When LVDS is used, ***[LVDCR1]***<LVDSEN>=1 should be set. Also set the comparator control bit ***[LVDCR1]*** <SELVD>=1. After setting, it is necessary to wait 200μs or more to stabilize the circuit.

3.2.2. Selection of Detected Voltage

The detected voltage in LVD can be set separately for LVDN and LVDS circuits.

[LVDLVL1]<LVDNLVL> selects the detected voltage for LVDN. And ***[LVDLVL2]***<LVDSLVL> selects the detected voltage for LVDS. After setting, it is necessary to wait 200μs to stabilize the comparator circuit.

3.2.3. Selection from Interrupt and Reset

The interrupt request or the reset signal can be selected as the LVD detection output.

The interrupt request is selected by ***[LVDCR1]***<LVDSEL>=0 setting. The reset signal is selected by ***[LVDCR1]*** <LVDSEL> = 1 setting. These settings are common to LVDN and LVDS.

3.2.4. Output Control of Interrupt and Reset

The output of the interrupt request or the reset signal is controlled by ***[LVDCR2]***<LVDOEN>.

When the output is enabled, ***[LVDCR2]***<LVDOEN>=1 should be set. The setting is common to LVDN and LVDS.

3.2.5. Status Register

The status of the DVDD3 voltage can be monitored by LVD as the level equal to or more than the setting level, or less.

The status in LVDN should be monitored in ***[LVDSR]***<LVDNS>. And the status in LVDS should be monitored in ***[LVDSR]***<LVDSS>. When ***[LVDSR]***<LVDNS> or <LVDSS> is read, the read should be done more than once until the same data is read twice.

3.3. Setting Change

In case of the detected voltage is changed or the output of the selection from the reset signal and the interrupt request is changed, the output should be disabled by setting ***[LVDCR2]***<LVDOEN> to “0” at first. Then, the change should be set.

Software should manage the necessary time to change it. After that, the output should be enabled by setting ***[LVDCR2]***< LVDOEN> to “1”.

3.4. Timing for Detection and Reset Release

The following figure shows the voltage detection and the reset release operations in the voltage detection circuit.

1) Power On

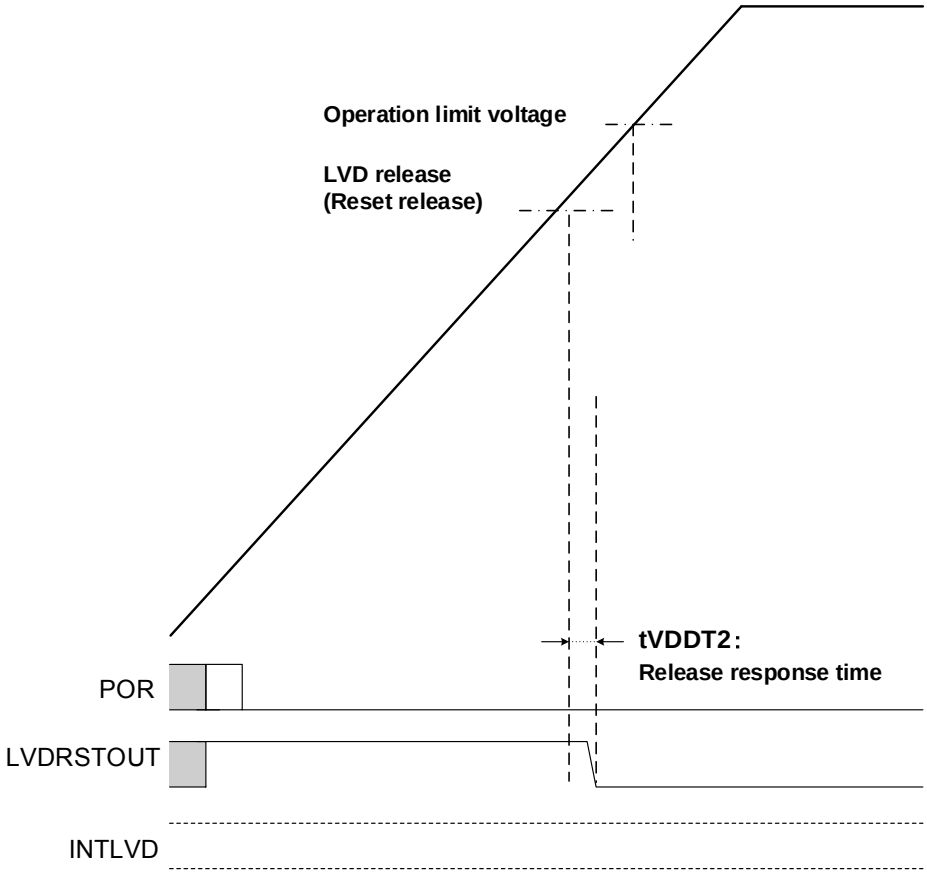


Figure 3.1 LVD release timing

2) LVD detection, Release timing

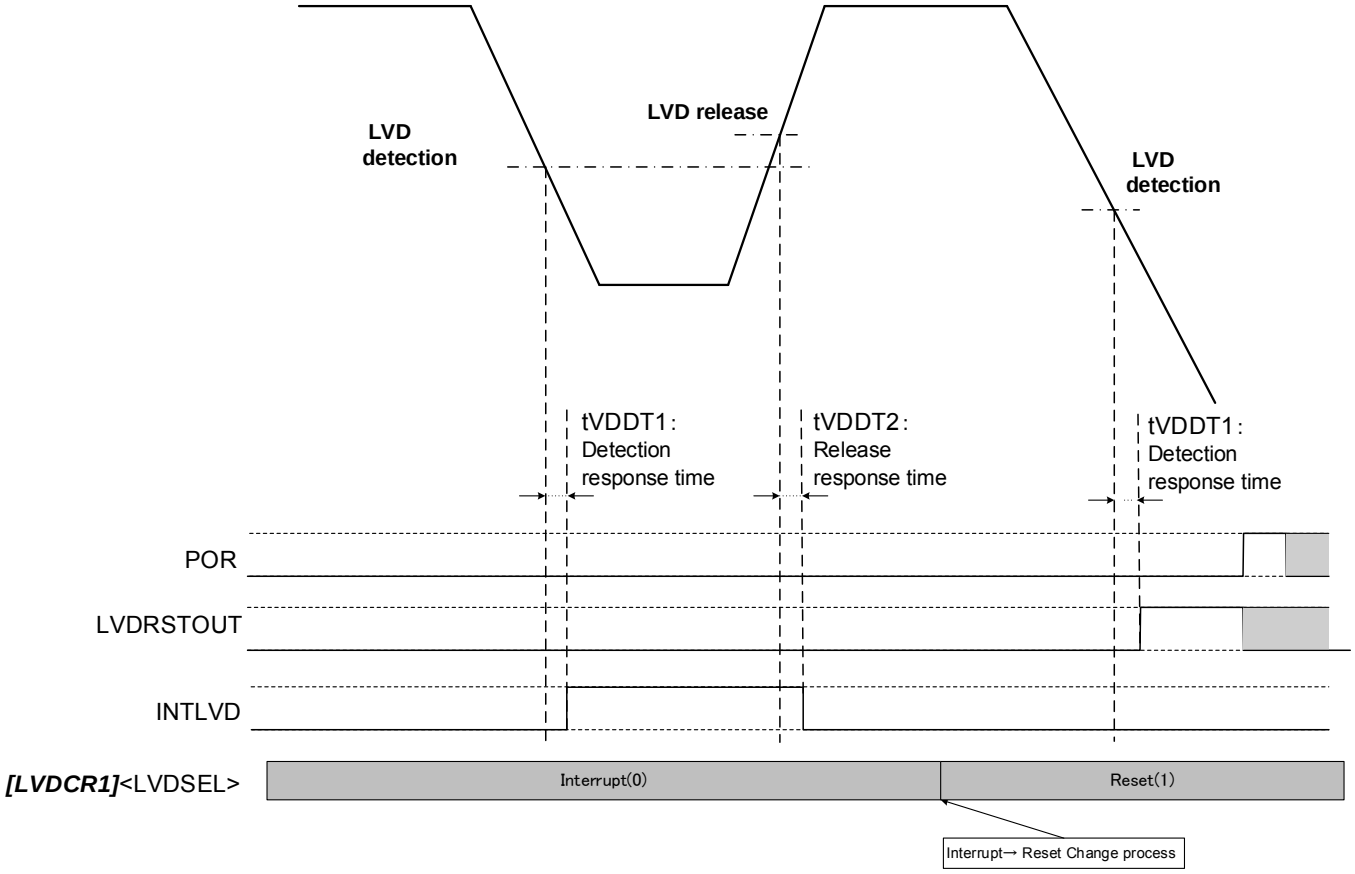


Figure 3.2 LVD detection, Release timing

3) LVD detection minimum pulse width

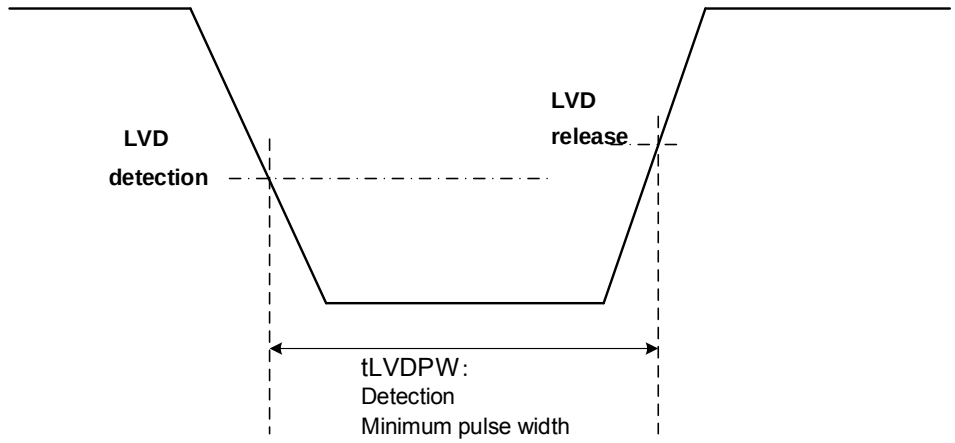


Figure 3.3 LVD detection minimum pulse width

4. Registers

4.1. List of Registers

The registers of LVD and their addresses are shown in the following tables.

Peripheral function		Channel/Unit	Base address	
			TYPE 1	TYPE 2
Voltage detection circuit	LVD	-	0x4003EC00	-

Register name		Base address (Base+)
LVD Control Register 1	***[LVDCR1]***	0x0000
LVD Control Register 2	***[LVDCR2]***	0x0001
LVD Detected Voltage Selection Register 1	***[LVDLVL1]***	0x0002
LVD Detected Voltage Selection Register 2	***[LVDLVL2]***	0x0003
LVD Status Register	***[LVDSR]***	0x0004

Note1: The bit-band-access is prohibitted. Only Byte access is permission.
Note2: The voltage detection circuit can be initialized by Power On Reset or the external reset pin (RESET_N).

4.1.1. *[LVDCR1]* (LVD Control Register 1)

Bit	Symbol	After Reset	Type	Description
7	SELVD	0	R/W	LVDS comparator control 0: Stop 1: Operating
6:5	–	0	R	Read as “0”.
4	LVDSEL	1	R/W	Selection from Interrupt request and Reset signal 0: Interrupt request (INTLVD) 1: Reset signal(LVDRSTOUT)
3:2	–	0	R	Read as “0”.
1	LVDSEN	0	R/W	Operation control of the voltage detection in LVDS (for STOP2) 0: Disabled. 1: Enabled.
0	LVDNEN	1	R/W	Operation control of the voltage detection in LVDN (for NORMAL, IDLE, and STOP1) 0: Disabled. 1: Enabled.

4.1.2. *[LVDCR2]* (LVD Control Register 2)

Bit	Symbol	After Reset	Type	Description
7:1	–	0	R	Read as “0”.
0	LVDOEN	1	R/W	Output control of Interrupt request or Reset signal. 0: Disabled. 1: Enabled.

4.1.3. *[LVDLVL1]* (LVD Detected Voltage Selection Register 1)

Bit	Symbol	After Reset	Type	Description
7:4	—	0	R	Read as “0”.
3:0	LVDNLVL [3:0]	0110	R/W	Voltage selection for LVDN Detected Voltage / Reset release voltage 0000: 3.100 V / 0000: 3.150 V 0001: 3.000 V / 0001: 3.050 V 0010: 2.900 V / 0010: 2.950 V 0011: 2.800 V / 0011: 2.850 V 0100: 2.700 V / 0100: 2.750 V 0101: 2.600 V / 0101: 2.650 V 0110: 2.500 V / 0110: 2.550 V Setting 0111 to 1111 is prohibited.

4.1.4. *[LVDLVL2]* (LVD Detected Voltage Selection Register 2)

Bit	Symbol	After Reset	Type	Description
7:4	—	0	R	Read as “0”.
3:0	LVDSLVL [3:0]	0000	R/W	Voltage selection for LVDS Detected voltage 0000: 3.100 V 0001: 3.000 V 0010: 2.900 V 0011: 2.800 V 0100: 2.700 V 0101: 2.600 V 0110: 2.500 V Setting 0111 to 1111 is prohibited.

Note: LVDS does not have the reset-release function using the voltage detection.

4.1.5. *[LVDSR]* (LVD Status Register)

Bit	Symbol	After Reset	Type	Description
7:2	—	0	R	Read as “0”.
1	LVDSS	Undefined.	R	Detection status for LVDS 0: Equal to or more than the set voltage 1: Less than the set voltage
0	LVDNS	Undefined.	R	Detection status for LVDN 0: Equal to or more than the set voltage 1: Less than the set voltage

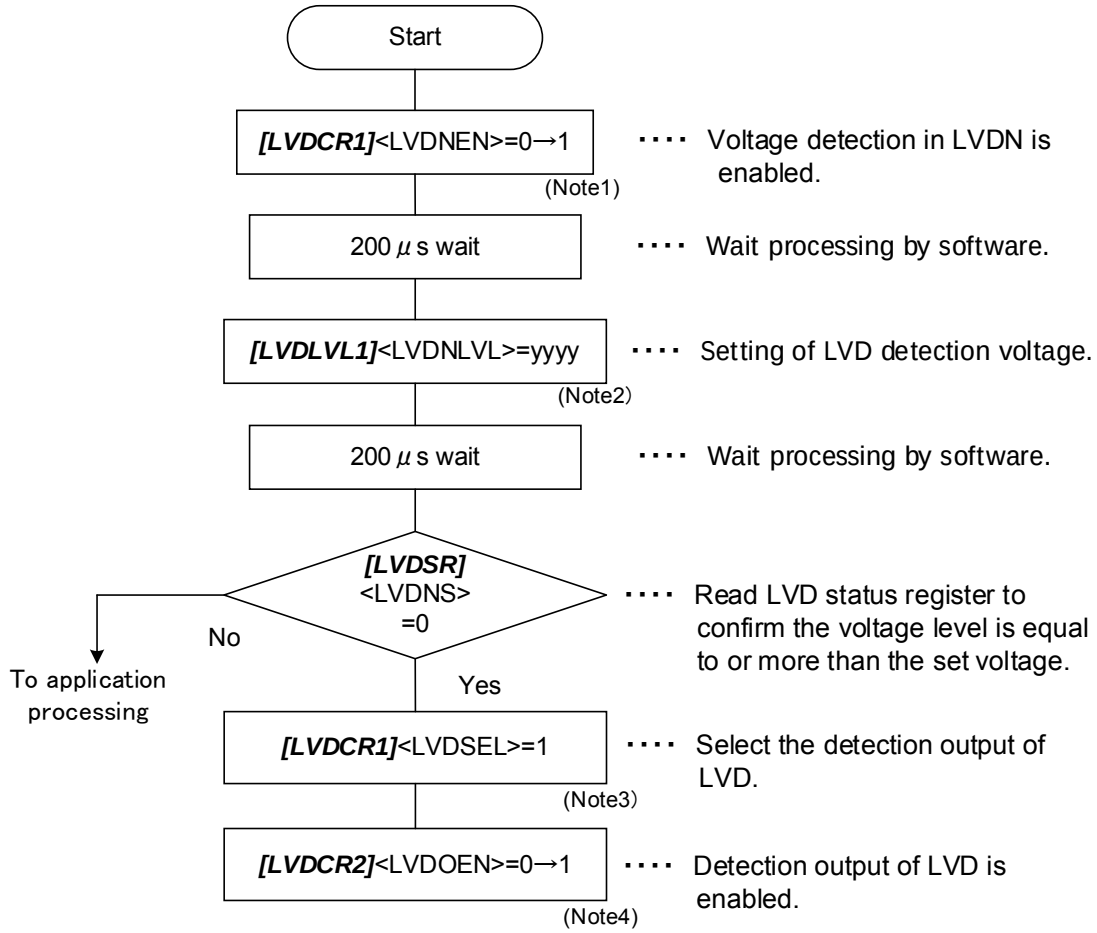
Note: The comparator of LVDN is different from the comparator of LNDS. So, the status of their circuits may not be the same even if the same detected voltage is set to the circuits.

5. Programming

Examples of the programming flow are shown in this section.

For the setting conditions, refer to Section "5.7. Voltage Waveform".

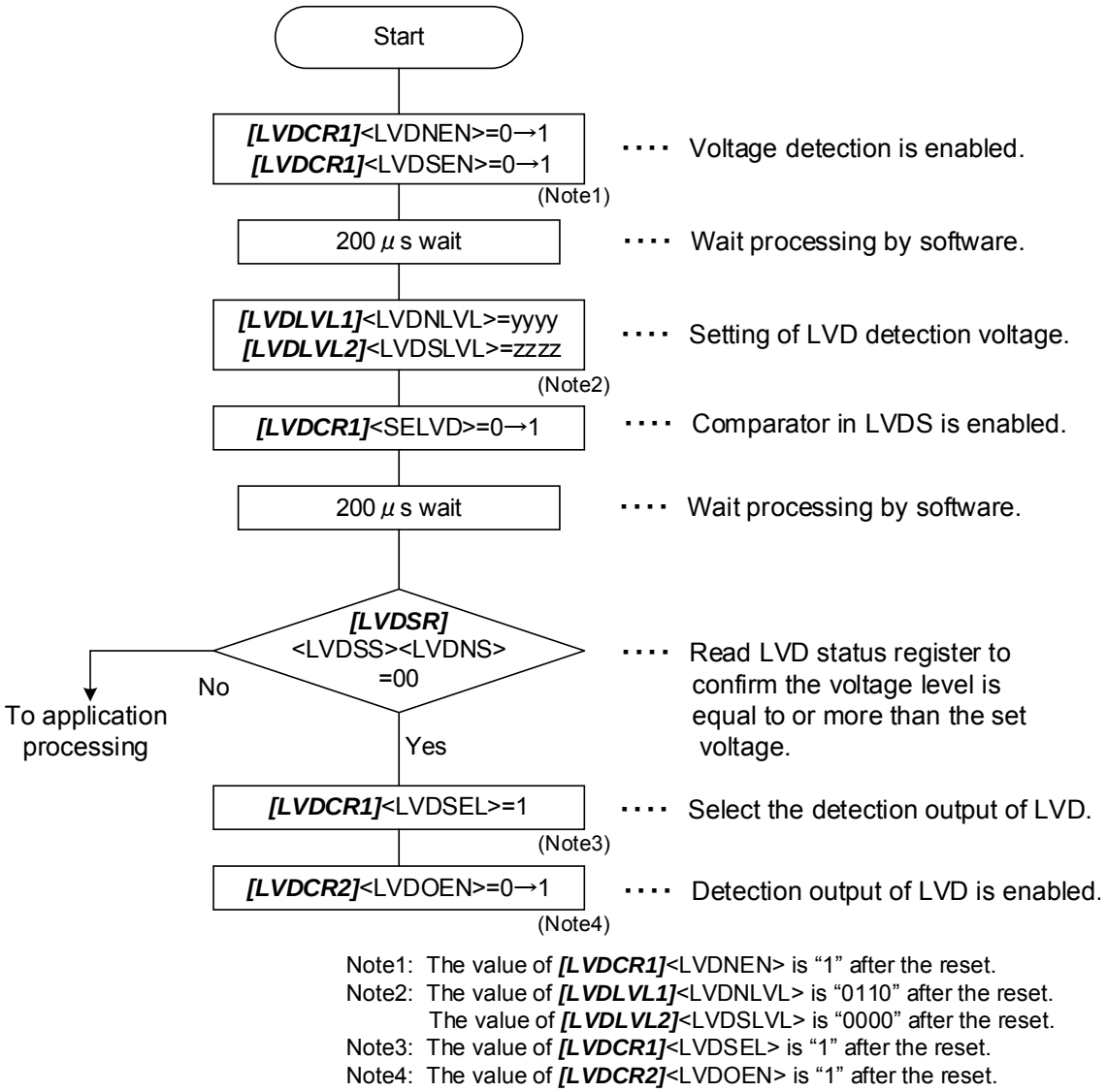
5.1. Initial Setting for LVDN … (1) Flow



Note1: The value of ***[LVDCR1]***<LVDNEN> is "1" after the reset.
Note2: The value of ***[LVDLVL1]***<LVDNLVL> is "0110" after the reset.
Note3: The value of ***[LVDCR1]***<LVDSEL> is "1" after the reset.
Note4: The value of ***[LVDCR2]***<LVDOEN> is "1" after the reset.

Figure 5.1 Initial setting for LVDN ((1) flow)

5.2. Initial Setting for LVDN and LVDS … (2) Flow



Note1: The value of ***[LVDCR1]***<LVDNEN> is "1" after the reset.
Note2: The value of ***[LVDLVL1]***<LVDNLVL> is "0110" after the reset.
The value of ***[LVDLVL2]***<LVDSLVL> is "0000" after the reset.
Note3: The value of ***[LVDCR1]***<LVDSEL> is "1" after the reset.
Note4: The value of ***[LVDCR2]***<LVDOEN> is "1" after the reset.

Figure 5.2 Initial setting for LVDN and LVDS ((2) flow)

5.3. Setting to Change Level

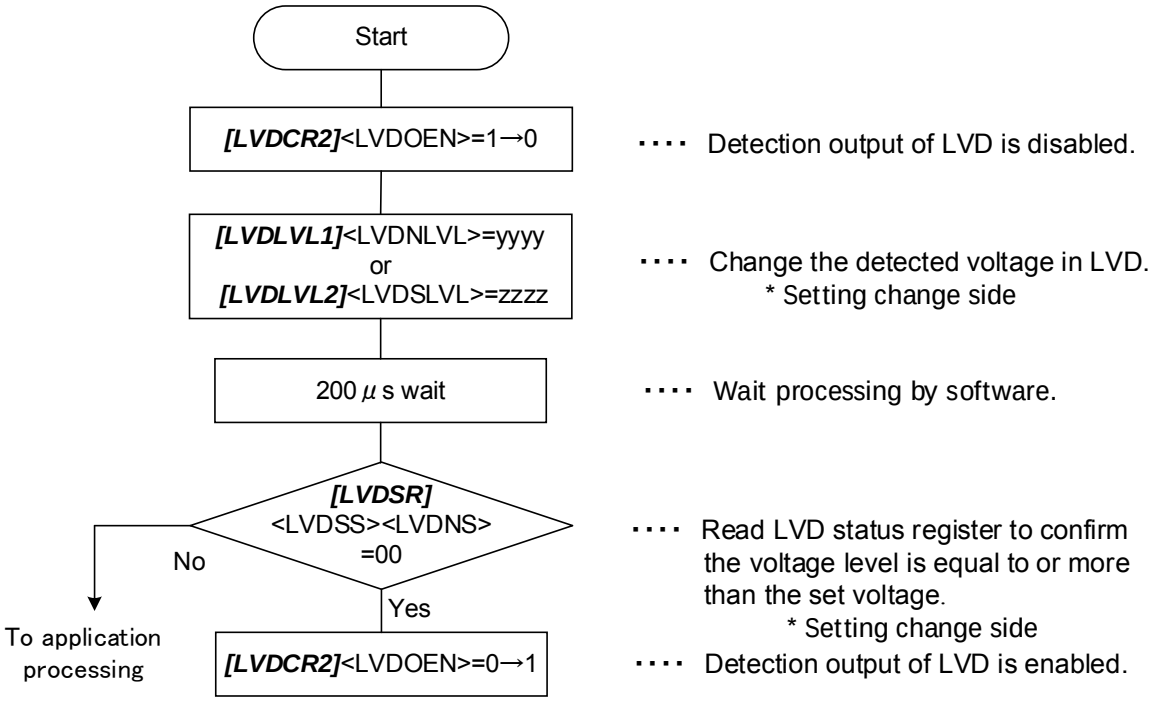


Figure 5.3 Example of the setting flow to change the level

5.4. Setting to from LVDN Enable State to LVDS Enable State

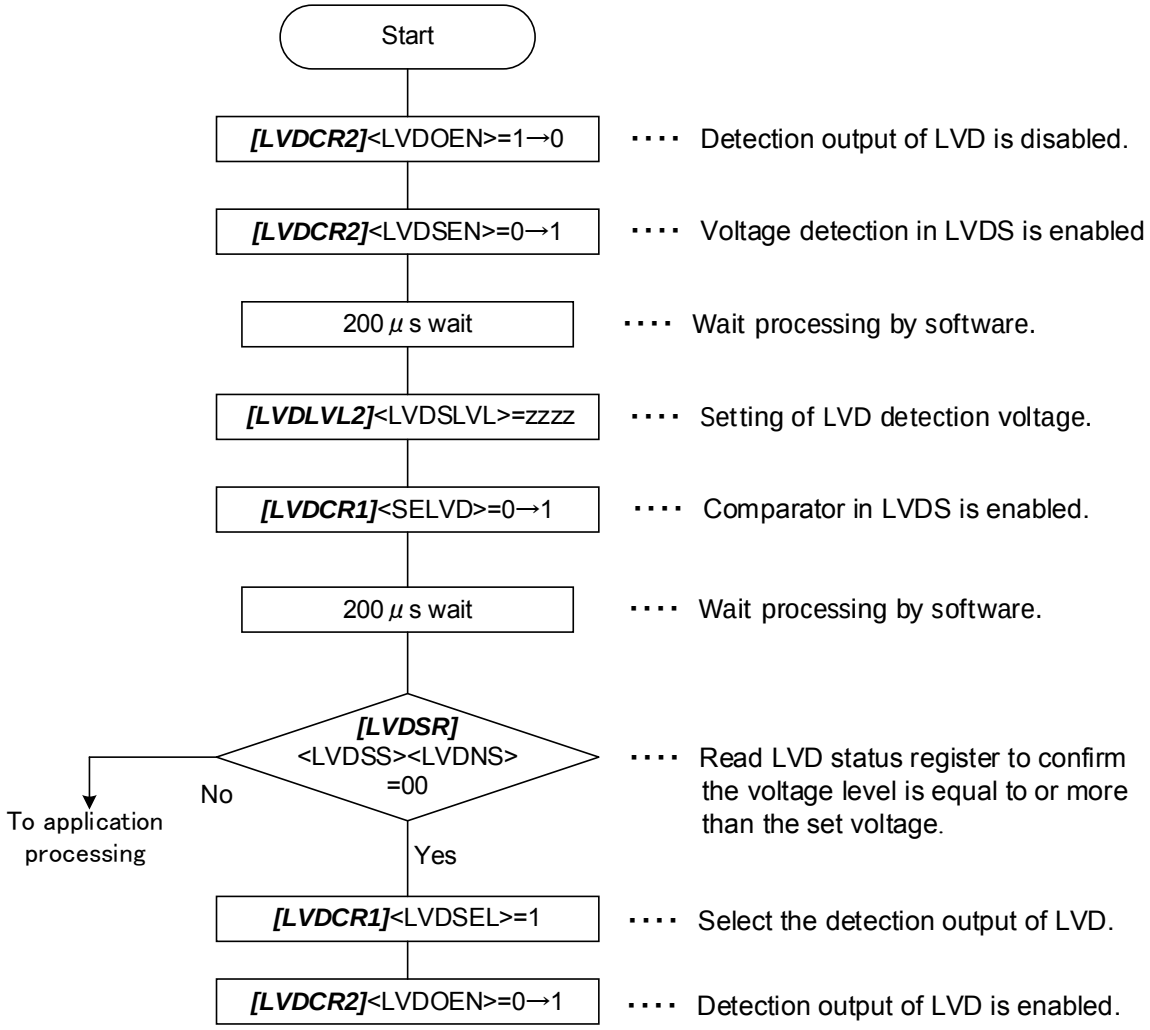


Figure 5.4 Example of the setting flow from LVDN enable state to LVDS enable state

5.5. Setting from LVDN and LVDS Enable State to LVDS disable state

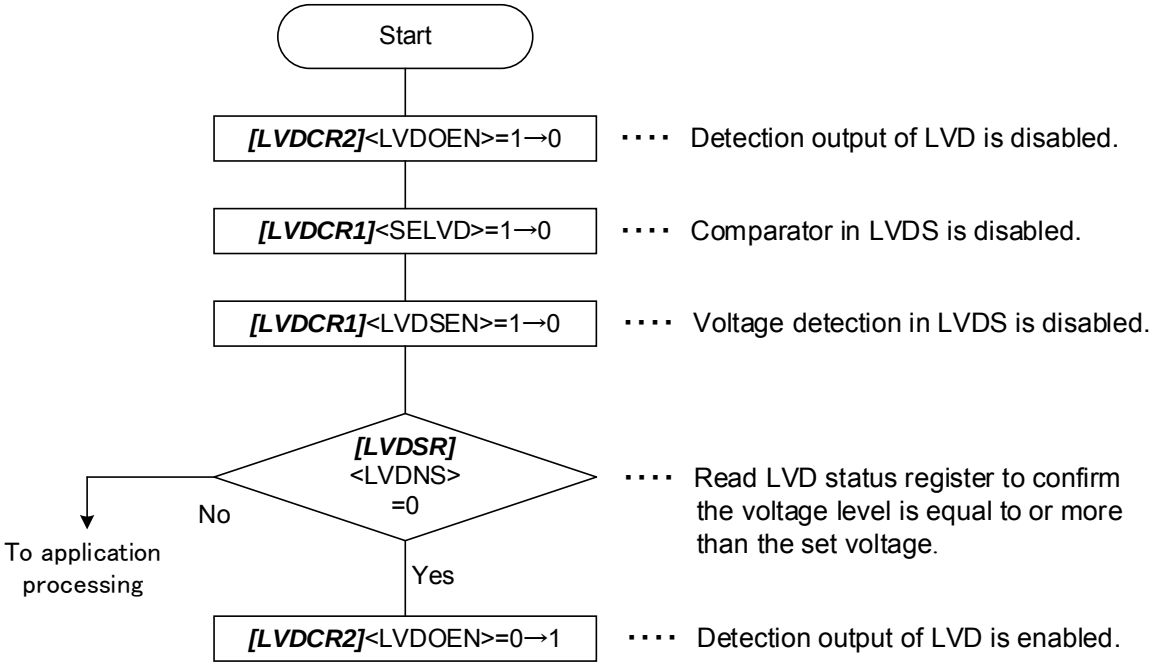


Figure 5.5 Example of the setting flow from LVDS enable state to LVDN and LVDS enable state

5.6. Setting from LVDN and LVDS Enable State to LVD disable state

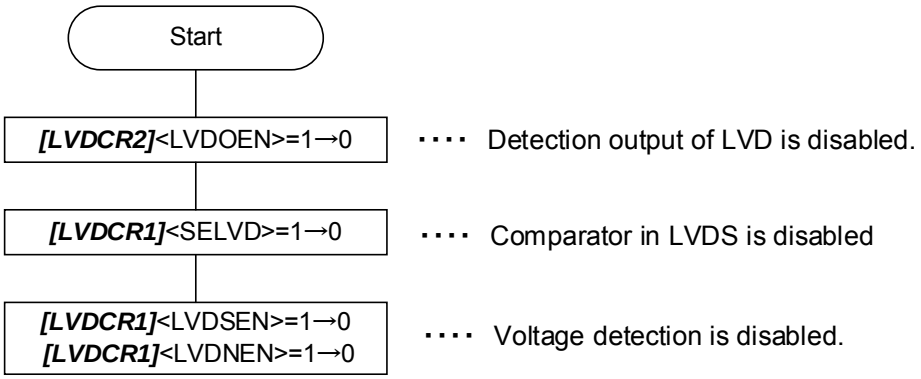


Figure 5.6 Example of the setting from LVDN and LVDS enable state to LVD disable state

5.7. Voltage Waveform

Voltage waveforms are shown in this section.

1) Example using LVDN

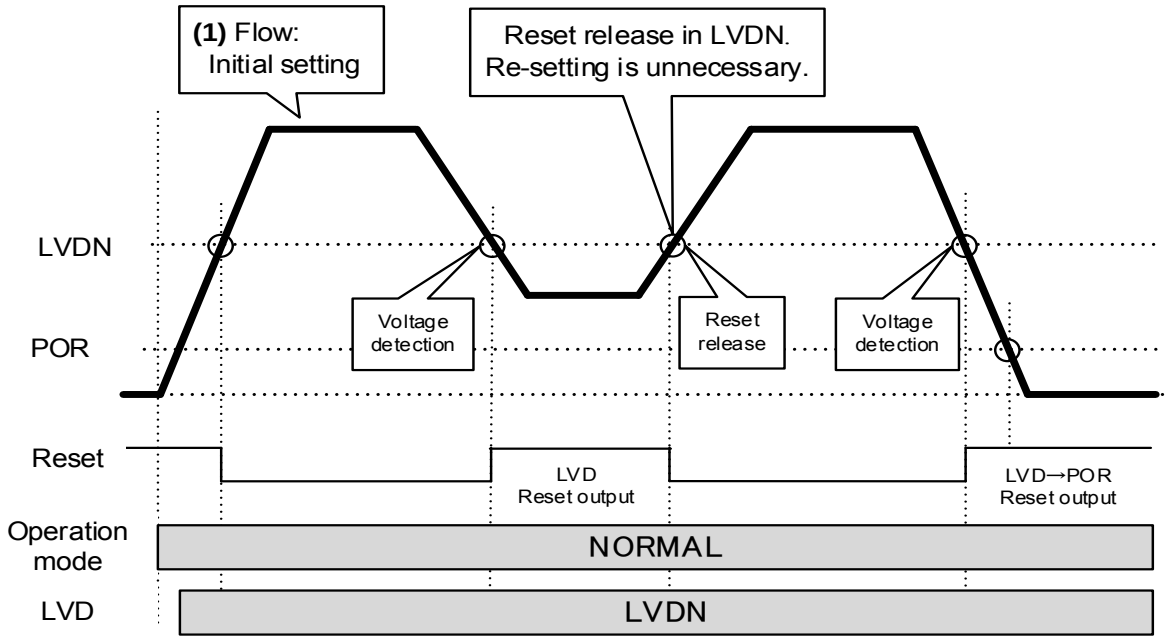


Figure 5.7 Example using LVDN

2) Example using LVDN and LVDS

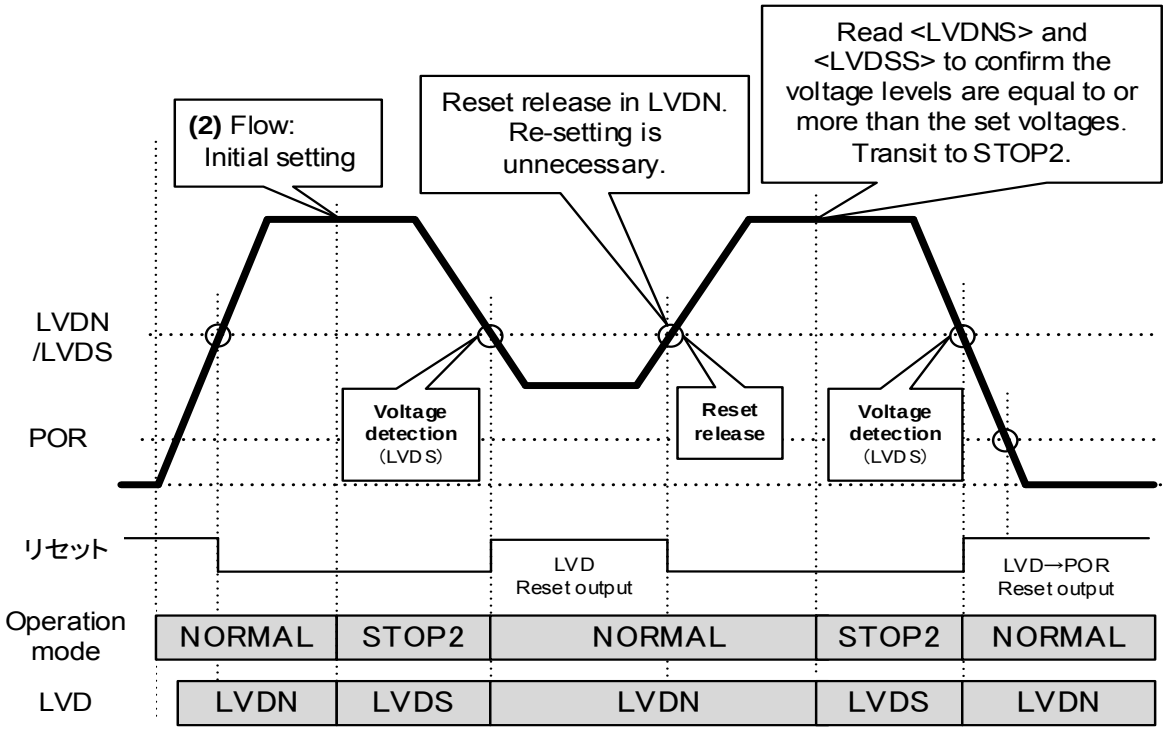


Figure 5.8 Example using LVDN and LVDS

6. Revision History

Table 6.1 Revision history

Revision	Date	Description
1.0	2017-12-26	First release
2.0	2018-02-20	2.Configuration Corrected : Figure 2.1. 3.4. Timing for Detection and Reset Release Corrected : Figure 3.1. Added : 1) Power On 2) LVD detection, Release timing 3) LVD detection minimum pulse width Added : Figure 3.2、Figure 3.3. 4.1.1 [LVDCR1] <LVDSEL> of Description is modified. 5.4. Setting to from LVDN Enable State to LVDS Enable State Corrected : Figure 5.4

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**