Toshiba CMOS Integrated Circuit Silicon Monolithic

TC7717FTG

Residential & Commercial Renewable Energy System (up to 1000 V AC or 1500 V DC) DC-AC control interface IC

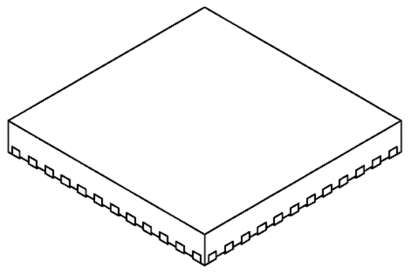
General outline

The TC7717FTG is a DC-AC control interface IC. It is used for photovoltaic system power conditioner.
This device incorporates input and output pins of controller signal, 12-bit ADC, differential circuit for detection, S/P interface, and Boost-IC[Note1] interface.

Features

- Process: C-MOS
- Internal reference power supply: 1.5 V (typ.) and 3.0 V (typ.)
- Input voltage
  AVDD and DVDD: 3.3 V±0.3 V
  ADVREF: 3.0 V (typ.)
- UVLO function by AVDD pin: Malfunction prevention in under voltage
  Release: 2.7 V (max)
  Stop: 2.2 V (min)
- Built-in 12-bit SAR AD converter (ADC core0 and core1)
  Operation of 3.3 V single power supply, conversion time 1 μs
  Main CLK: 40 MHz (typ.), External CLK of PLL reference: 10 MHz (typ.)
- Sampling function
  AC current (AIN0 core0), DC voltage (AIN0 core1)
  System voltage VU-VO (AIN1 core0), VW-VO (AIN1 core1)
- Detection function
  AC/DC current component detection (IDCERR), system voltage detection (VUO_OUT)
  System zero cross detection (L_HZO)
  DC current detection (I_INV)
- Analog (comparator detection threshold) monitor function
- S/P interface input (slave side)
  Comparator threshold correction (±10 %)
    DC over current (DC_OC_REF), DC over voltage (DC_OV_REF)
    AC over current (AC_OC_REF), AC limit current (AC_CL_REF)
  Analog (comparator detection threshold) monitor selection
    DC over current (DC_OC), DC over voltage (DC_OV)
    AC over current (AC_OC), AC limit current (AC_CL)
- Boost-IC interface (target device T5DK1FG, master side)
  ADC start signal (ADST), data transfer clock (ADCLK)
  ADC sampling data signal (DOUT0 and DOUT1)
- External reset input pin: C-MOS input
- Package QFN40 (6.0 mm × 6.0 mm, 0.5 mm Pitch)

Note 1: "Boost-IC": Dedicated controller (T5DK1FG)



P-VQFN40-0606-0.50-001

Weight 97.6 mg (typ.)

This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

Pin assignment (Top View)

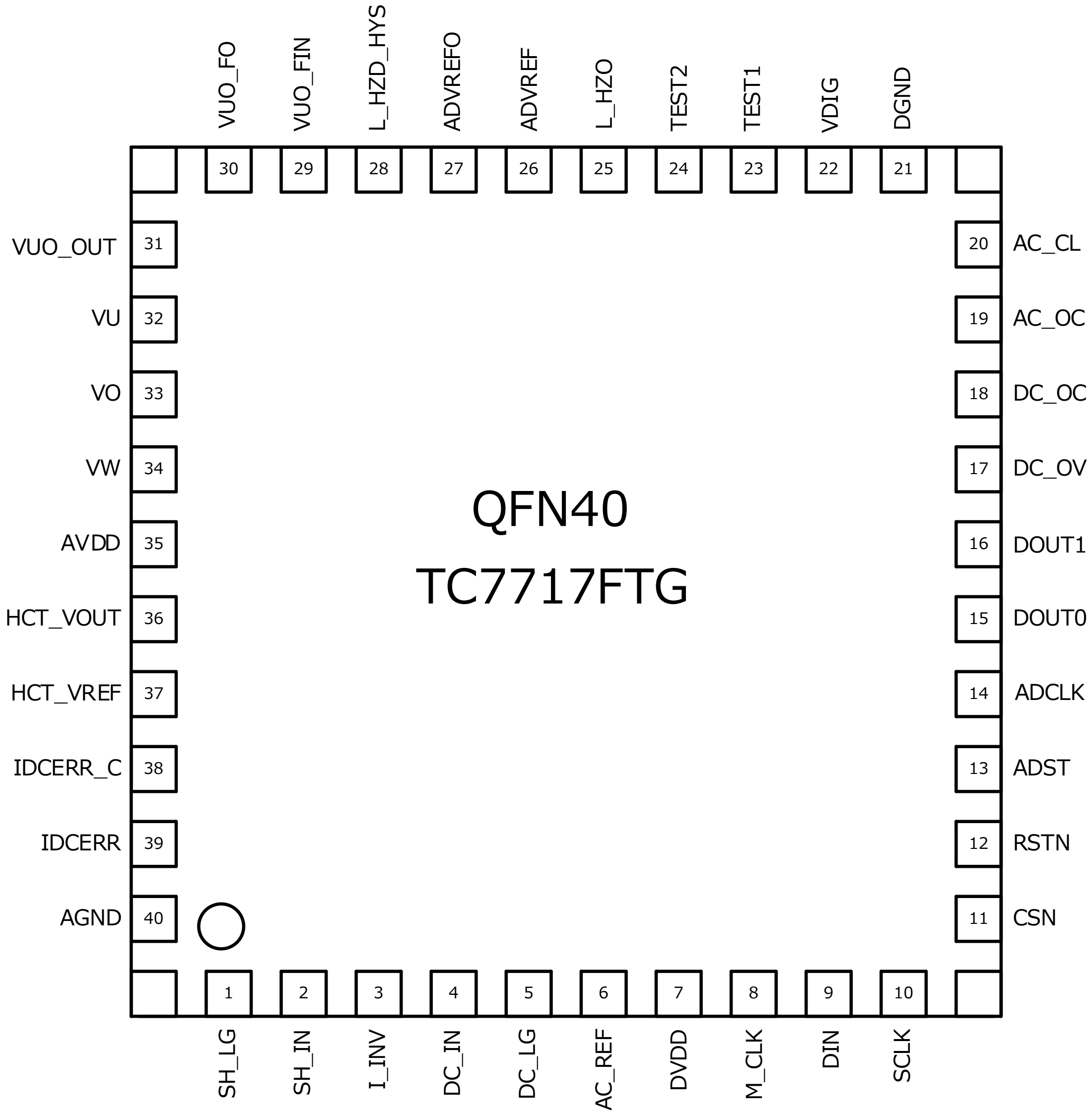


Figure-1

*: Corner PAD and back-surface of heat dissipating PAD of QFN package should be connected to GND of the board.

*: Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Pin functions (1)

Table-1 (1)

Pin No.	Pin name	I/O	Descriptions	Pull-Up/Pull-Down External resistor (≥10kΩ)
1	SH_LG	A/I	Non-Inverting input pin of DC current detection amplifier GND side of the board of the shunt resistance (GND of DC voltage) is connected. SH_LG, DGND, DC_LG, and AGND should be short-circuited externally as a GND of the board.	—
2	SH_IN	A/I	Inverting input pin of DC current detection amplifier Inverter bridge side of the shunt resistance is connected. Protection diode should be connected between SH_IN (cathode) and SH_LG (anode).	—
3	I_INV	L/O A/O	Output (inverting amplifier signal) pin of DC current detection amplifier PLL lock flag is outputted in startup and reset (RSTN=Low). Analog internal signal can be monitored by S/P interface setting.	—
4	DC_IN	A/I	Inverting input pin of DC voltage detection amplifier Resistive-divided DC voltage (about 0.4212 %) is connected. Protection diode should be connected between DC_IN (cathode) and DC_LG (anode).	—
5	DC_LG	A/I	Non-Inverting input pin of DC voltage detection amplifier GND side of DC voltage is connected. SH_LG, DGND, DC_LG, and AGND should be short-circuited externally as a GND of the board.	—
6	AC_REF	A/O	Output pin for reference voltage of system (AC) voltage detection Lower-side voltage of resistive-divided voltage (VU, VO, and VW) is connected to this pin. (1.5 V)	—
7	DVDD	P/I	Input pin for 3.3 V-power supply of logic circuit DVDD and AVDD should be short-circuited externally.	—
8	M_CLK	L/I	Input pin for external reference clock of PLL 3.3 V-reference clock signal (10 MHz) is input from MCU.	Pull-Down
9	DIN	L/I	Input pin for serial data of S/P interface 3.3 V-data signal is input from MCU. It is only for slave side.	Pull-Up
10	SCLK	L/I	Input pin for transmitting clock of S/P interface 3.3 V-data transmitting clock signal is input from MCU.	Pull-Down
11	CSN	L/I	Input pin for start signal of S/P interface 3.3 V-signal is input from MCU. Low=setting data input	Pull-Up
12	RSTN	L/I	Input pin for IC reset It input the result of external power supply monitoring. High=normal operation, Low=initialization (same as UVLO in startup)	Pull-Down
13	ADST	L/I	Input pin in starting ADC sampling trigger of Boost IC interface ADC starts sampling by triggering this High pulse. ADC output is activated by S/P interface setting.	Pull-Down
14	ADCLK	L/O	Output pin for ADC sampling data transmitting clock of Boost IC interface It outputs ADC sampling data from DOUT0 or DOUT1 in synchronizing with this clock.	Pull-Down
15	DOUT0	L/O	Output pin for ADC sampling data of Boost IC interface (ADC-0, AIN0: AC current, AIN1: system AC voltage U-O)	Pull-Down
16	DOUT1	L/O	Output pin for ADC sampling data of Boost IC interface (ADC-1, AIN0: DC voltage, AIN1: system AC voltage W-O)	Pull-Down
17	DC_OV	L/O	Output pin for the result of over voltage (OV) detection comparator of DC voltage. High=normal operation, Low=detection	Pull-Up
18	DC_OC	L/O	Output pin for the result of over current (OC) detection comparator of DC voltage. High=normal operation, Low=detection	Pull-Up
19	AC_OC	L/O	Output pin for the result of over current (OC) detection comparator of AC current. High=normal operation, Low=detection	Pull-Up
20	AC_CL	L/O	Output pin for the result of limit current (CL) detection comparator of AC current. High=normal operation, Low=detection	Pull-Up

I/O: A/I=Input analog circuit, A/O=Output analog circuit, L/I=Input logic circuit, L/O=Output logic circuit, P/I=Input operation power supply, P/O=Output operation power supply

Remarks: Logic circuit output (L/O) is indefinite in startup. It becomes initial value after the reset signal (RSTN) is input low. The logic output is as same logic level as Pull-Up/Pull-Down resistance in the normal operation.
(Ex: Pull-Up="High", Pull-Down="Low")

Pin function (2)

Table-1 (2)

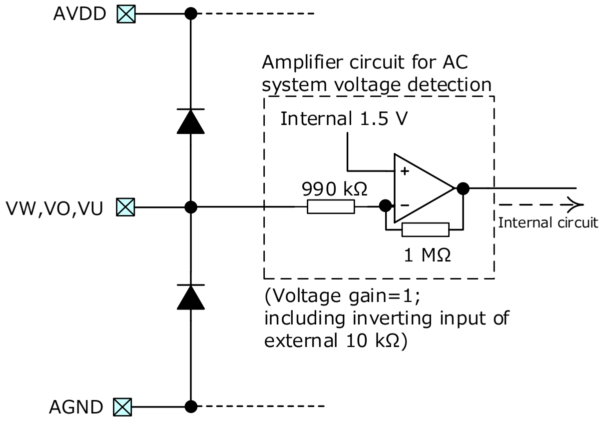
Pin No.	Pin name	I/O	Descriptions	Pull-Up/Pull_Down External resistor (≥10kΩ)
21	DGND	P/I	Ground pin for digital circuit SH_LG, DGND, DC_LG, and AGND should be short-circuited externally as a GND of the board.	—
22	VDIG	P/O	Pin for monitor and for connecting decoupling capacitor of 1.5 V-internal power supply for digital circuit Connect decoupling capacitor of 0.1 μF between this pin and GND of the board.	—
23	TEST1	L/I	Vendor usage pin Normal mode: Low input. Connect to GND.	Built-in Pull-down of 100kΩ
24	TEST2	L/I		
25	L_HZO	L/O	Output pin of zero cross detection comparator (Note)	Pull-Down
26	ADVREF	P/I	Input pin of reference power supply for ADC (3.0 V) (Note)	—
27	ADVREFO	P/O	Internal generation pin of reference power supply for ADC (3.0 V) When external power supply is used, it is set open.	—
28	L_HZD_HYS	A/I	Hysteresis set pin of zero cross detection comparator (Note)	—
29	VUO_FIN	A/I	Prefilter input pin of zero cross detection comparator (Note)	—
30	VUO_FO	A/O	Prefilter output pin of zero cross detection comparator (Note)	—
31	VUO_OUT	A/O	Output pin for system AC voltage detection amplifier (phase U-O) (Note)	—
32	VU	A/I	Input pin for system AC voltage (phase U) Resistive divided voltage (about 0.37 %) between system AC voltage (phase U) and the pin number 6 is input. Connect protection diode between VU (cathode) and GND of the board (anode).	—
33	VO	A/I	Input pin of system AC voltage (phase O) Resistive divided voltage (about 0.37 %) between system AC voltage (phase O) and the pin number 6 is input. Connect protection diode between VO (cathode) and GND of the board (anode).	—
34	VW	A/I	Input pin of system AC voltage (phase W) Resistive divided voltage (about 0.37 %) between system AC voltage (phase W) and the pin number 6 is input. Connect protection diode between VW (cathode) and GND of the board (anode).	—
35	AVDD	P/I	Input pin for analog circuit of 3.3 V-main power supply DVDD and AVDD should be short-circuited externally.	—
36	HCT_VOUT	A/I	Non-inverting input pin of AC current detection amplifier Connect output pin of the current transducer.	—
37	HCT_VREF	A/I	Inverting input pin of AC current detection amplifier Connect reference voltage output pin of the current transducer.	—
38	IDCERR_C	A/O	Filter set pin of AC/DC current component detection amplifier The capacitor (0.68 μF) for low pass filter that decreases the frequency of 50Hz to 2.6/100 is connected between this pin and GND of the board.	—
39	IDCERR	A/O	Output pin of AC/DC current component detection amplifier. It outputs the DC current component (IDCERR_C voltage) of AC by amplifying to 26 times. It is recommended to apply the notch filter to derive DC component after this output.	—
40	AGND	P/I	Ground pin for analog circuit SH_LG, DGND, DC_LG, and AGND should be short-circuited externally as a GND of the board.	—

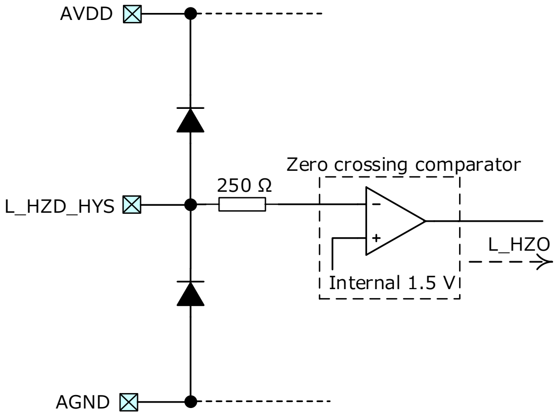
Note: As for the connection to each pin, refer to page 11, 20 or 21 because there are two or more parts.
I/O: A/I=Input analog circuit, A/O=Output analog circuit, L/I=Input logic circuit, L/O=Output logic circuit, P/I=Input operation power supply, P/O=Output operation power supply

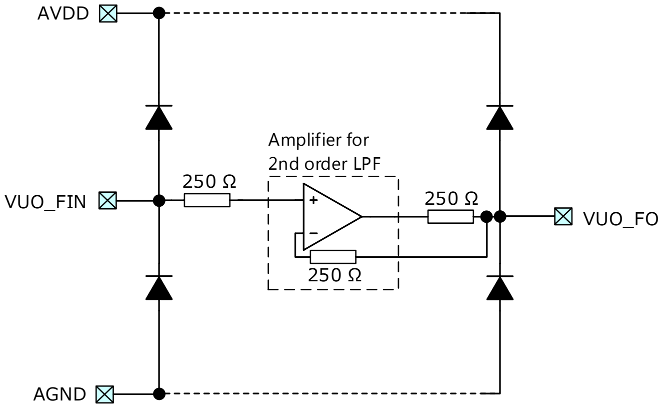
Remarks: Logic circuit output (L/O) is indefinite in startup. It becomes initial value after the reset signal (RSTN) is input low. The logic output is as same logic level as Pull-Up/Pull-Down resistance in the normal operation
(Ex: Pull-Up="High", Pull-Down="Low").

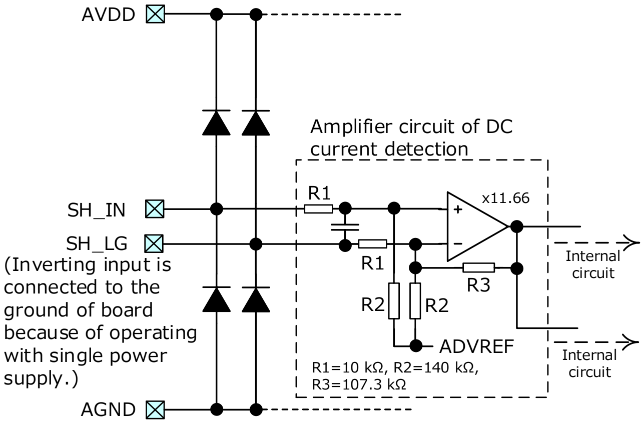
I/O equivalent circuit (1)

Table-2 (1)

<table>
<tr><th>Pin name</th><th>I/O equivalent circuit</th></tr>
<tr><td>VW,VO,VU</td><td>


</td></tr>
<tr><td>L_HZD_HYS</td><td>


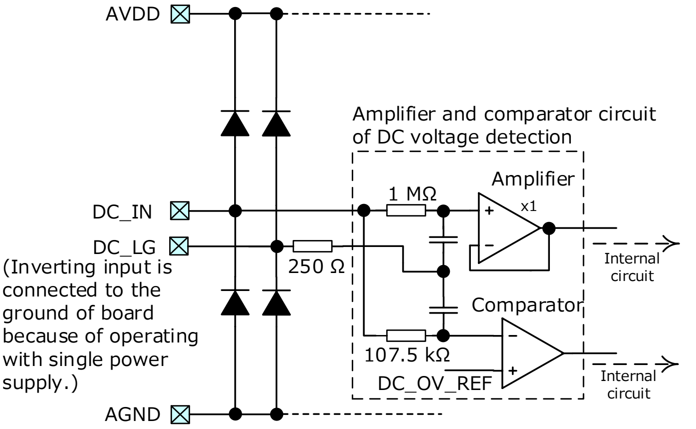
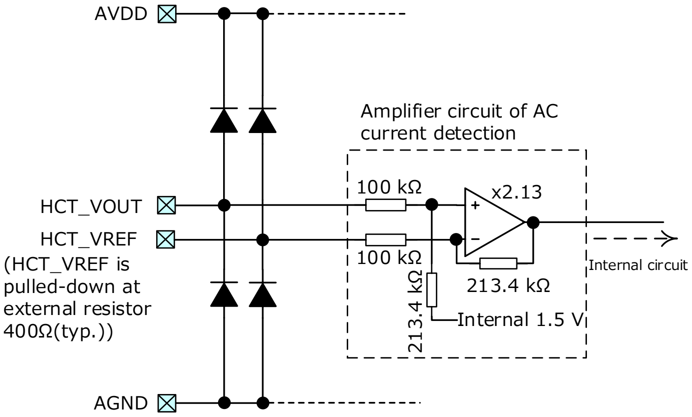
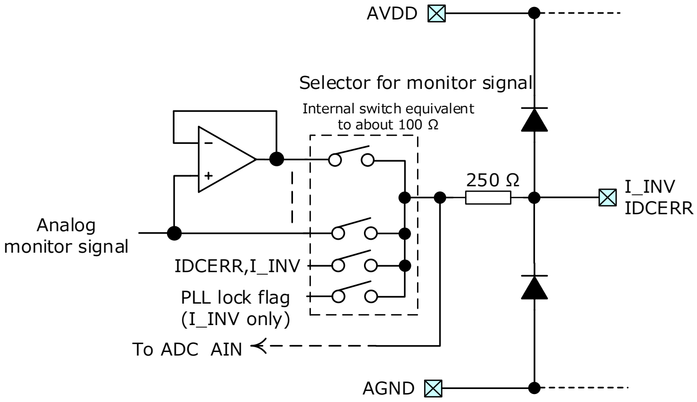
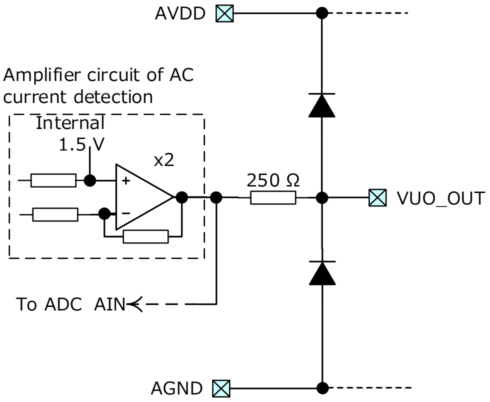
</td></tr>
<tr><td>VUO_FIN, VUO_FO</td><td>


</td></tr>
<tr><td>SH_LG,SH_IN</td><td>


</td></tr>
</table>

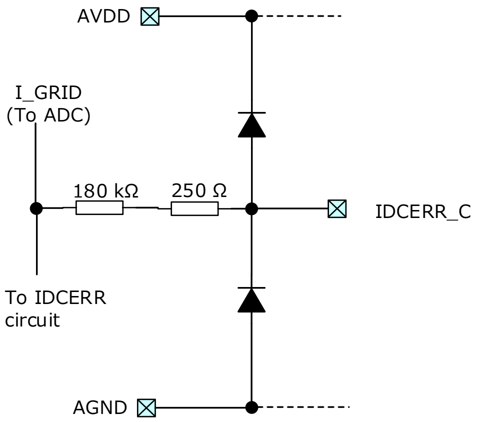
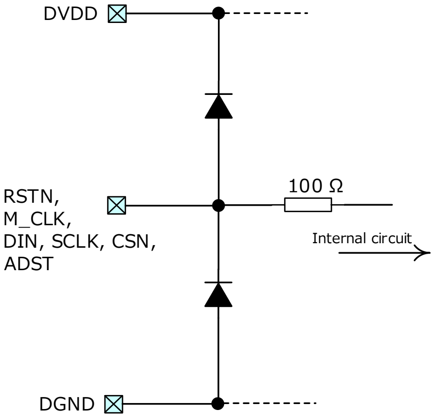
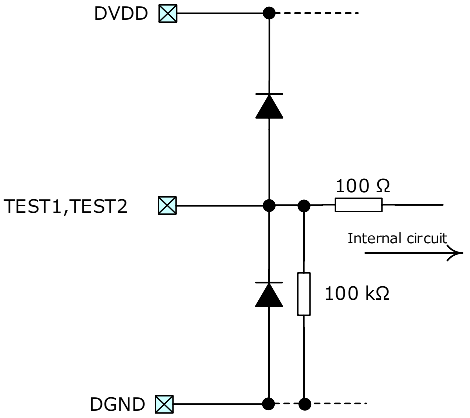
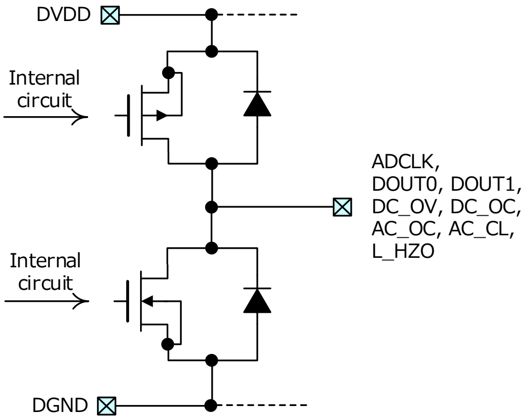
I/O equivalent circuit (2)

Table-2 (2)

Pin name	I/O equivalent circuit
DC_LG, DC_IN	 (Inverting input is connected to the ground of board because of operating with single power supply.)
HCT_VOUT, HCT_VREF	 (HCT_VREF is pulled-down at external resistor 400Ω(typ.))
I_INV IDCERR	
VUO_OUT	

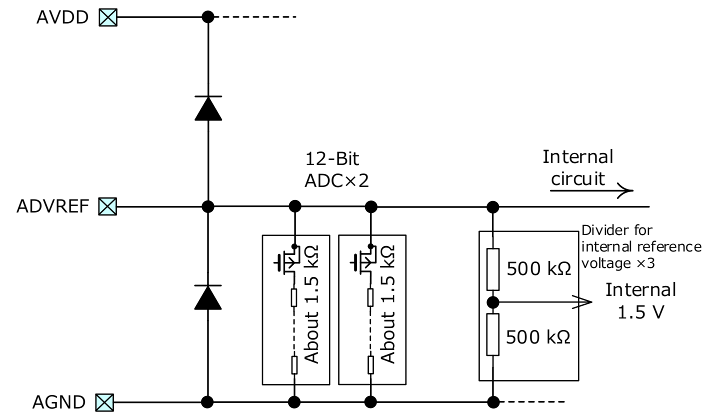
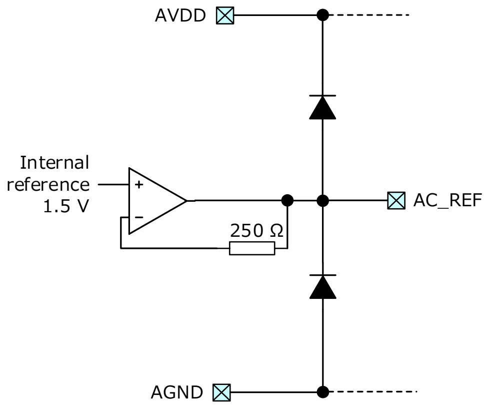
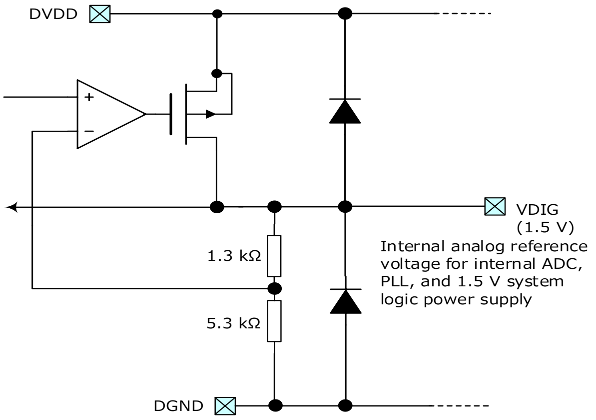
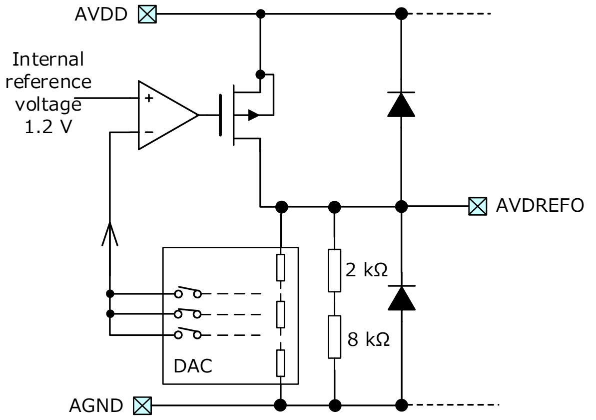
I/O equivalent circuit (3)

Table-2 (3)

Pin name	I/O equivalent circuit
IDCERR_C	
RSTN, M_CLK, DIN, SCLK, CSN, ADST	
TEST1,TEST2	
ADCLK, DOUT0,DOUT1, DC_OV,DC_OC, AC_OC,AC_CL, L_HZO	

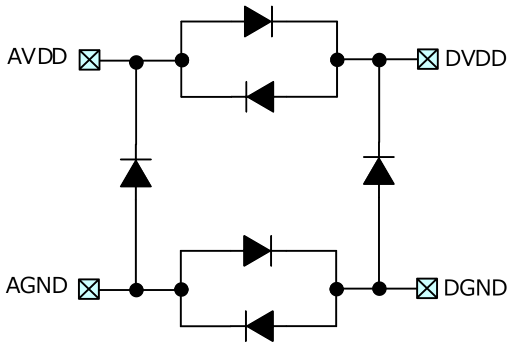
I/O equivalent circuit (4)

Table-2 (4)

Pin name	I/O equivalent circuit
ADVREF	
AC_REF	
VDIG	
ADVREFO	

I/O equivalent circuit (5)

Table-2 (5)

Pin name	I/O equivalent circuit
AVDD, DVDD AGND, DGND	

Block diagram of the entire solar power conditioner system

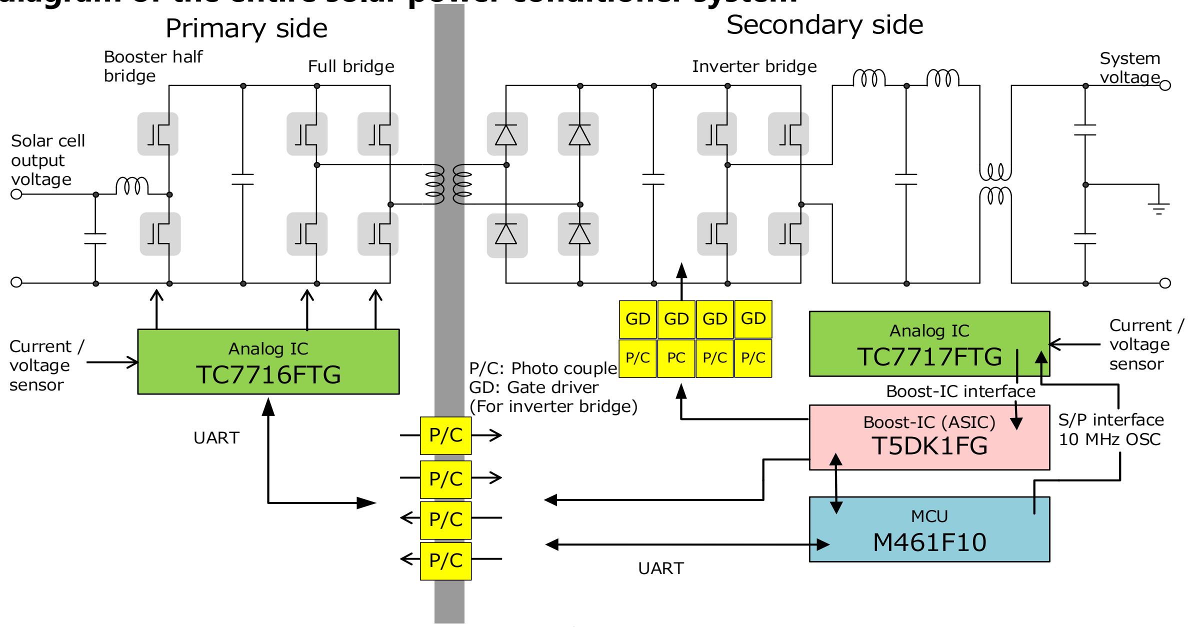


Figure-2

Example of application circuit:

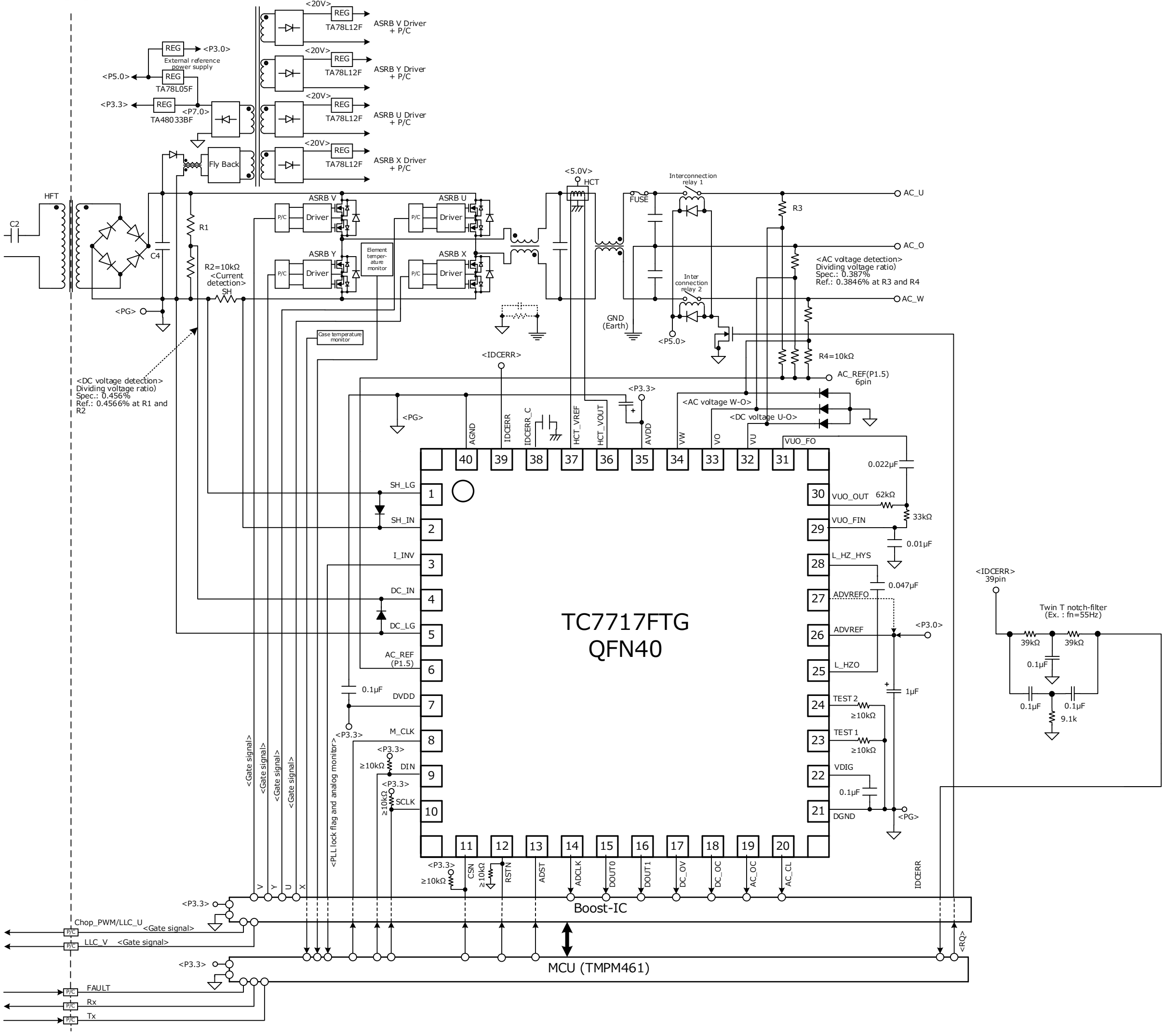


Figure-3

*: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Providing these application circuit examples does not grant a license for industrial property rights.

Inverter / system block:

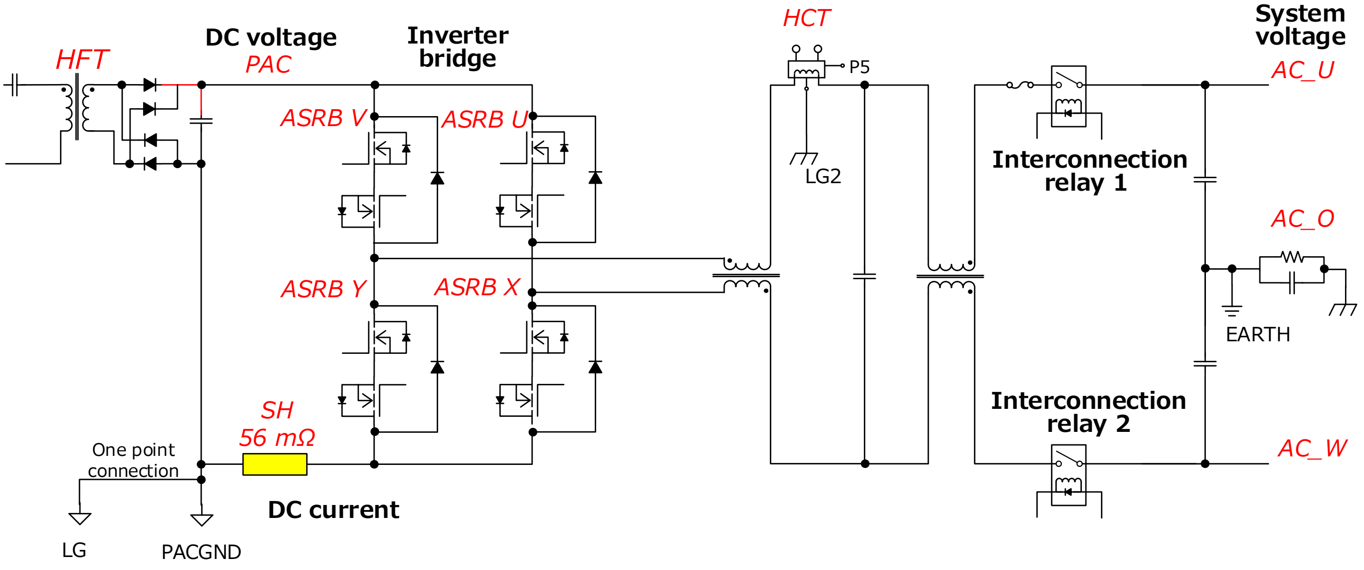


Figure-4

*: System block diagram may be omitted or simplified for explanatory purposes.

Block diagram:

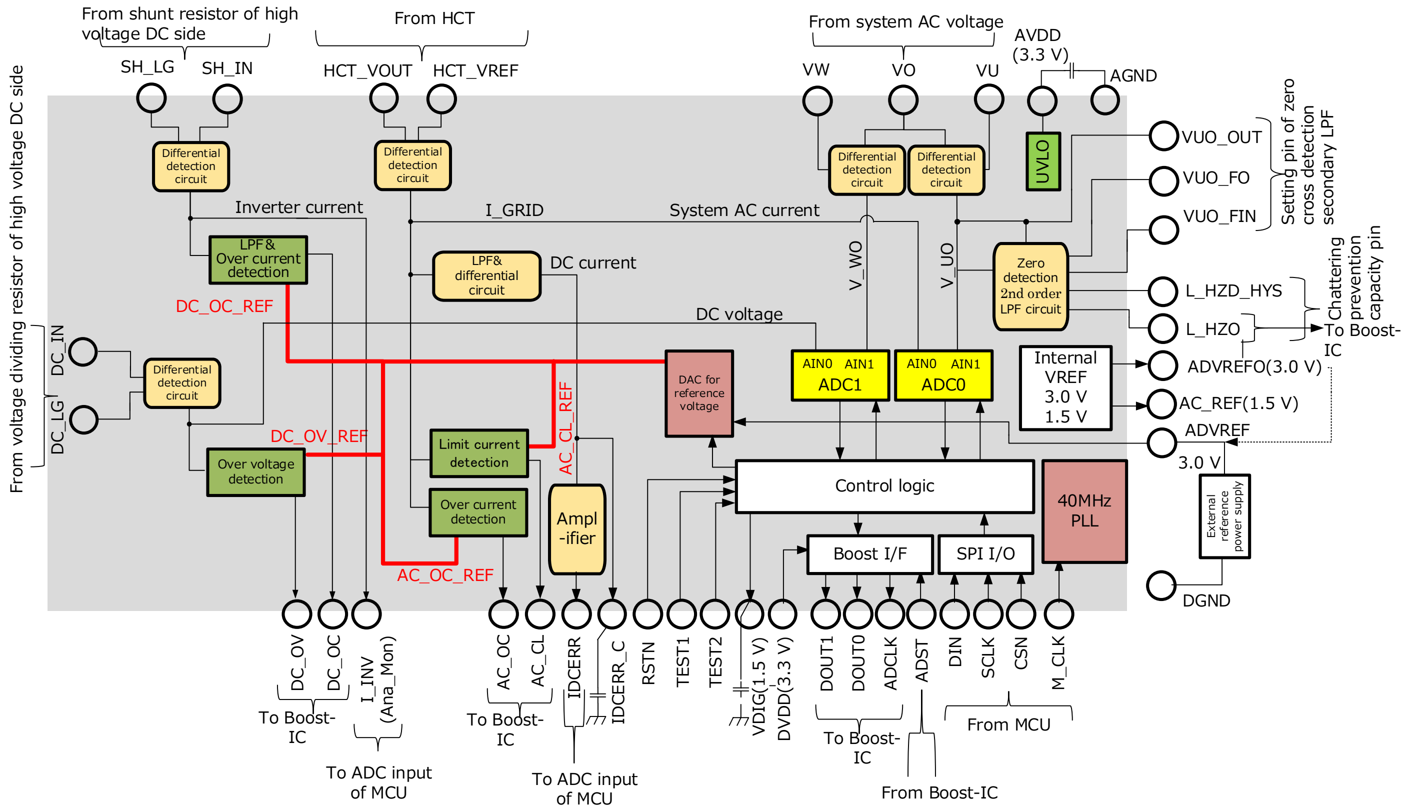


Figure-5

*: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Absolute maximum ratings (Unless otherwise specified, Ta=25 °C)

Table-3

Characteristics	Symbol	Rating	Unit
Power supply voltage	AVDD,DVDD	3.7	V
Power supply voltage	V_ADVREF	3.7	V
Apply voltage of analog and logic input pins	Vih	(*1) Refer to the following table	V
	Vil	AGND,DGND-0.3 (*2)	V
Power dissipation (*3)	P_D	3716	mW
Operating temperature	T_{opr}	-40 to 85	°C
Storage temperature	T_{stg}	-55 to 125	°C
Junction temperature	T_j	125	°C

*1: Maximum applied voltage for each pin (Do not exceed over 3.7 V.)

Table-4

Pin No.	Symbol	Rating	Unit		Pin No.	Symbol	Rating	Unit
1	SH_LG	AVDD+0.3	V		21	DGND	—	V
2	SH_IN	AVDD+0.3			22	VDIG	(*4)	
3	I_INV	(*5)			23	TEST1	—	
4	DC_IN	AVDD+0.3			24	TEST2	—	
5	DC_LG	AVDD+0.3			25	L_HZO	DVDD+0.3	
6	AC_REF	VDIG+0.3			26	ADVREF	3.7	
7	DVDD	3.7			27	ADVREFO	(*4)	
8	M_CLK	DVDD+0.3			28	L_HZD_HYS	AVDD+0.3	
9	DIN	DVDD+0.3			29	VUO_FIN	AVDD+0.3	
10	SCLK	DVDD+0.3			30	VUO_FO	(*5)	
11	CSN	DVDD+0.3			31	VUO_OUT	AVDD+0.3	
12	RSTN	DVDD+0.3			32	VU	AVDD+0.3	
13	ADST	DVDD+0.3			33	VO	AVDD+0.3	
14	ADCLK	DVDD+0.3			34	VW	AVDD+0.3	
15	DOUT0	DVDD+0.3			35	AVDD	3.7	
16	DOUT1	DVDD+0.3			36	HCT_VOUT	AVDD+0.3	
17	DC_OV	DVDD+0.3			37	HCT_VREF	AVDD+0.3	
18	DC_OC	DVDD+0.3			38	IDCERR_C	(*5)	
19	AC_OC	DVDD+0.3			39	IDCERR	(*5)	
20	AC_CL	DVDD+0.3			40	AGND	—	

*2: Each pin commonness, AGND and DGND should be connected on the board.

*3: Board conditions: □76-1.6t-4 layer FR-4 board, internal layer 100 %, external layer 3.5 % (only pin assignment) When Ta is 25 °C or more, 29.7 mW decreases from absolute maximum rating per 1 °C rise.

*4: Do not apply voltage externally.

*5: Only for output pin

*6: “—”: Connecting to GND

* The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

Package power dissipation

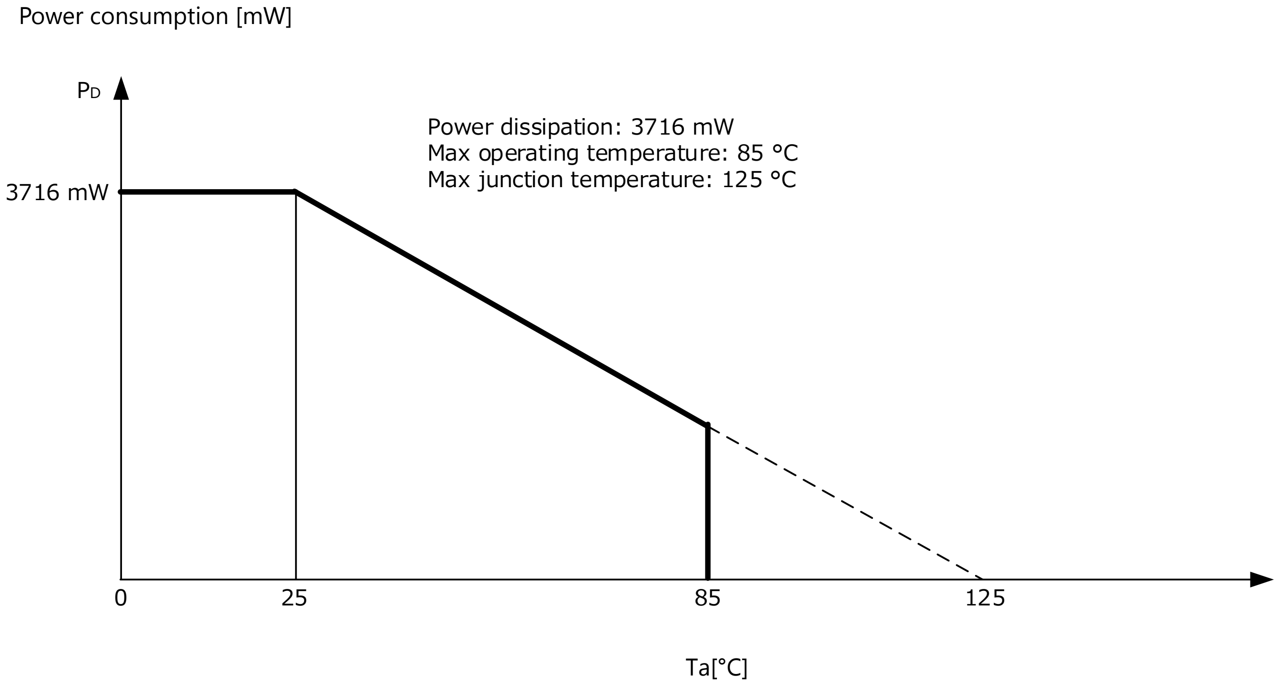


Figure-6

Operating condition (Ta =25 °C)

Table-5

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Power supply voltage	AVDD	—	3.0	3.3	3.6	V
	DVDD	—				
	V_ADVREF	Input external power supply	2.7	3.0	3.3	
Rising time of power supply	tr_AVDD tr_DVDD	Normal operation: Input external power supply 0 V to 0.8 V *AVDD and DVDD	100	—	—	μs
Falling time of power supply	tf_AVDD tf_DVDD	Normal operation: Input external power supply 3.3 V to 0.2 V *AVDD and DVDD	100	—	—	μs

Reference power supply and UVLO characteristics (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-6

Reference power supply and UVLO (Malfunction prevention in under voltage)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Reference power supply for AC voltage detection	V_acref	Only for resistive-divided voltage for AC detection	1.48	1.5	1.52	V
Consumption current	Idd_ana	M_CLK=10 MHz, ADC active	—	10	25	mA
	Idd_advref	—	—	2	5	
Startup voltage (UVLO release voltage)	Vstr	Only for AVDD	—	—	2.7	V
UVLO operation voltage	Vuvlo	Only for AVDD	2.2	—	—	
Operation power supply pin for logic circuit (built-in)	Vdig	For external decoupling	1.35	1.5	1.65	

Changeable reference power supply for internal ADC

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Output voltage	V_advrefo	ADREFTMP[2:0]=011 ADREFT[4:0]=10010	2.9	3.0	3.1	V

<Operation description>

UVLO function: Malfunction is prevented when the voltage of AVDD pin is low.

When AVDD voltage is 2.2 V (min) or less, internal circuit is initialized (reset) to prevent malfunction.
When it is 2.7 V (max) or more, reset of the internal circuit is released to resume the operation.

Operation of internal 3 V power supply (ADVREFO pin)

It incorporates 3 V reference power supply and it outputs from ADVREFO pin. The voltage can be configured by S/P interface input and register set.

Equivalent circuit>

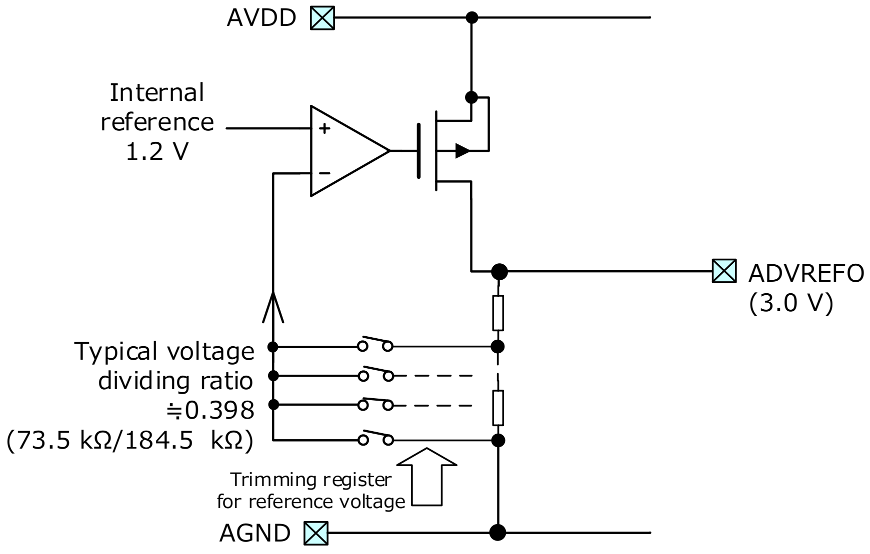


Figure-7

Digital I/O characteristics (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-7

IC reset pin

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Release reset (high level) input voltage	Vporoff	Input from external power supply monitor IC, Schmitt trigger input	0.7*DVDD	—	—	V
Reset (low level) input voltage	Vporon	—	—	—	0.3*DVDD	V
High level input current	Iihrstn	RSTN	—	—	1.0	μA
Low level input current	Iilrstn	RSTN	—	—	1.0	μA

S/P interface block input

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
High level input voltage	Vihspi	DIN, SCLK, CSN, M_CLK Schmitt trigger input	0.7*DVDD	—	—	V
Low level input voltage	Vilspi	DIN, SCLK, CSN, M_CLK Schmitt trigger input	—	—	0.3*DVDD	V
High level input current	Iihspi	DIN, SCLK, CSN, M_CLK	—	—	1.0	μA
Low level input current	Iilspi	DIN, SCLK, CSN, M_CLK	—	—	1.0	μA

Boost-IC interface block I/O

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
High level input voltage	Vihbst	ADST, Schmitt trigger input	0.7*DVDD	—	—	V
Low level input voltage	Vilbst	ADST, Schmitt trigger input	—	—	0.3*DVDD	V
High level input current	Iihbst	ADST	—	—	1.0	μA
Low level input current	Iilbst	ADST	—	—	1.0	μA
High level output voltage	Vhobst	ADCLK, DOUT0, DOUT1, Isource=-0.33 mA	0.7*DVDD	—	—	V
Low level output voltage	Vlobst	ADCLK, DOUT0, DOUT1, Isink =+0.33 mA	—	—	0.3*DVDD	V

Comparator output

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
High level output voltage	Vho_comp	DC_OC, DC_OV, AC_OC, AC_CL Isource=-0.33 mA	0.7*DVDD	—	—	V
Low level output voltage	Vlo_comp	DC_OC, DC_OV, AC_OC, AC_CL Isink =+0.33 mA	—	—	0.3*DVDD	V

DC current detection (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-8

DC current detection amplifier block (Shunt resistance (56 mΩ (typ.)) between SH_IN and SH_LG pins))

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Output voltage of detection signal	V_i-inv	Level shift voltage when V_sh-in=0 V.	0.14	0.200	0.26	V
		V_sh-in=99.8 mV	1.257	1.367	1.477	V
		V_sh-in=229.5 mV	2.765	2.875	2.985	V
Detection circuit gain	Av_sh-in	Ex.)130.3 kΩ/7.5 kΩ	11.42	11.66	11.90	—
Input offset voltage	ΔV_i-inv	Between SH_IN and SH_LG pins Input voltage V_sh-in=0 V	-5	—	+5	mV
Flow current of input pin	I_shin		-50	-20	—	μA

Comparator block of DC current detection: Detection target of the comparator is V_i-inv written above

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
DC_OC operating input voltage	V_dcocref	SH_IN voltage -> V_dcoc=High to Low	190	200	210	mV
Detection time	t_dcoc	Threshold is default of DAC Input voltage: Changeable from Rating to FS	—	—	5	μs

<Operation description>DC current detection

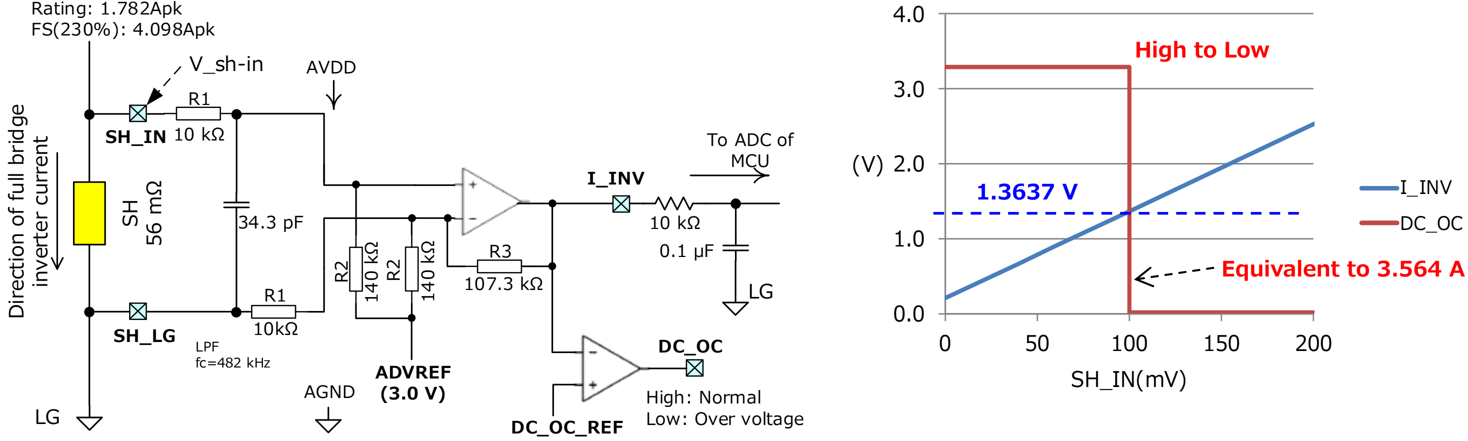
DC current detection circuit is shown in Figure-8. It monitors the DC current of the inverter bridge as voltage.

It constructs the low pass filter by the external parts (C×1 and R×1) to I_INV pin.

The difference voltage (0 to 229.5 mV) of shunt resistance between SH_IN and SH_LG pins is amplified (11.66 times) and the amplified voltage is outputted from I_INV pin.

When this voltage of I_INV pin is compared to the reference voltage (DC_OC_REF) by the comparator circuit and detected, the output voltage of DC_OC pin changes from High to Low.

Initial reference voltage of the comparator (DC_OC_REF) is 2.531 V (typ.@default). In this time, cutoff frequency of the amplifier is 482 kHz (typ.) and input offset voltage of the comparator is ±10 mV (max).


Equivalent circuit>

Values of internal resistance and capacitor are typical.

Comparator of DC over current detection (DC_OC)>

Figure-8

Table-9

Level of DC over current detection (typ.)

Level	Detection current		Input voltage V_sh-in	Output voltage V_i-inv
	%	A	mV	V
Zero	0	0	0	0.20
Rating	100	1.782	99.8	1.3637
OC	200	3.564	199.6	2.5273
FS	230	4.098	229.5	2.8759

Approximate equation is as follows;
Ex.) FS(230 %):
Input voltage V_sh-in
=Detection current (A)× shunt resistance
56(mΩ)=4.098(A)×56(mΩ)≈229.5(mV)
Output voltage V_i-inv
=V_sh-in(V)× amplifier circuit gain 11.66+ level shift
0.2(V)≈229.5(mV)×11.66+0.2=2.8759(V)
Output offset voltage Vls=ADVREF×R1/(R1+R2)=0.20 V
Amplifier circuit gain=R2/(R1+R2)+R3/R1≈11.66
In this time, R1:R2:R3=1:14:10.73

DC voltage detection (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3V, ADVREF=3.0V, AGND=DGND=DC_LG=SH_LG=0V)

Table-10

DC voltage detection amplifier block - Supply to internal ADC data -

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Detection signal output voltage	V_ain0_core1	V_dcin=0.125 V	0.115	0.125	0.135	V
		V_dcin=1.403 V	1.393	1.403	1.413	V
		V_dcin=2.875 V	2.865	2.875	2.885	V
Detection circuit gain	Av_dcov	V_dcin=0.125 to 1.519 V	0.99	1	1.01	—
Input pin leakage current	I_dcin	—	—	—	±1	μA

Comparator block of DC voltage detection

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Voltage of DC_OV pin	V_dcov_on	When internal DC_OV_REF voltage is default	2.264	2.297	2.330	V
Input pin leakage current	I_dcin	—	—	—	±1	μA
Detection time	t_dcov	Threshold: Default of DAC Input voltage: Changeable from Rating to FS	—	—	5	μs

<Operation description> DC voltage detection

DC voltage detection circuit is shown in Figure-9. It monitors the DC voltage of the inverter bridge as a value of voltage. The input voltage (0.125 to 2.875 V) which is divided to 0.4212 % from high voltage (PAC) for the resistance (10kΩ) between DC_IN and DC_LG, is input to the internal ADC (AIN0 core1) through the buffer circuit (×1).

Input offset voltage of this amplifier is ±15mV which is 1 % of input voltage (rating: 333 V).

When this internal voltage is compared to the reference voltage (DC_OV_REF) and detected by the comparator circuit, the output voltage of DC_OV pin changes from High to Low.

Initial reference voltage of the comparator (DC_OC_REF) is 2.297 V (typ.).

In this time, cutoff frequency of the amplifier is 2.97 kHz (typ.), cutoff frequency of the comparator is 482kHz(typ.), and input offset voltage of the comparator is ±10 mV (max).

Equivalent circuit>

Values of internal resistance and capacitor are typical.

Comparator of DC over voltage detection (DC_OV)>

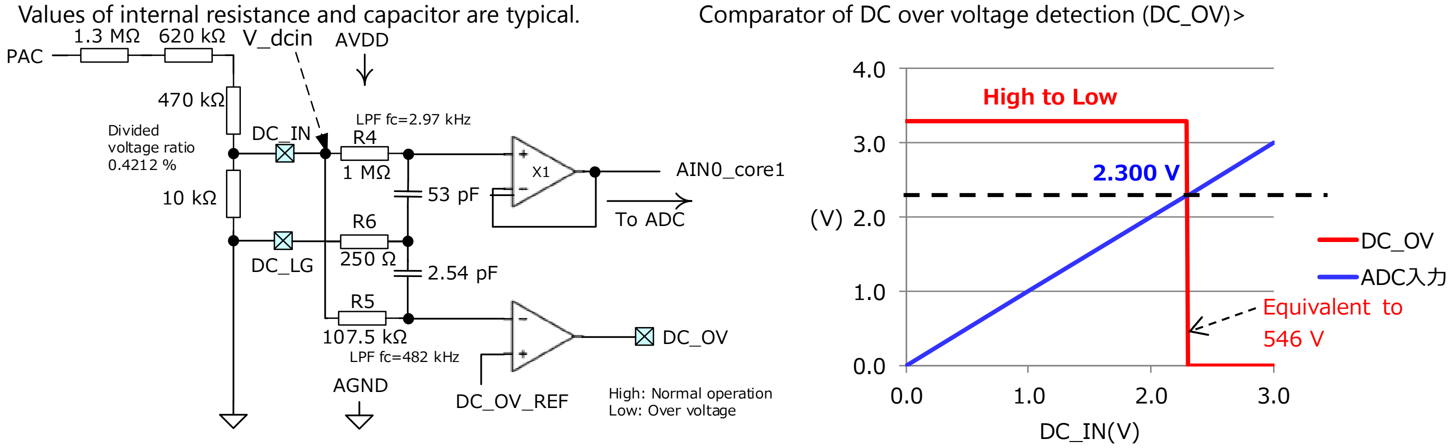


Figure-9

Partial resistances of 1.3 MΩ, 620 kΩ, 470 kΩ (upper side) are reference data. The recommended resistance between DC_IN and DC_LG is 10 kΩ. Ratio of this divided voltage is 0.418 % in this combination. Values of internal resistance and capacitor are typical.

Table-11

Level of DC over voltage detection (typ.)

Level	Detection voltage		Input voltage V_dcin	Output voltage V_ain0_core1
	%	V	V	V
0 -	—	—	Out of operating range	
Min	—	—	0.125	0.125
UV	—	50	0.211	0.211
Rating	—	333	1.403	1.403
	100	455	1.917	1.917
OV	120	546	2.300	2.300
FS	150	682.5	2.875	2.875

Approximate equation is as follows;
Ex.) FS (150 %):
Input voltage V_dcin
=Detection voltage (V)× Resistive-divided voltage
0.4212 %=682.5(V)×0.4212/100
≈2.875(V)
Output voltage V_ain0_core1= V_dcin(V)×Detection circuit gain 1
≈2.875×1.0=2.875(V)
In this time, voltage of less than 0.125 V is out of operation guarantee range.

AC current detection (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-12

AC current detection amplifier block - Supply to internal ADC data -

Characteristics	Symbol	Test conditions		Min	Typ.	Max	Unit
Output voltage of detection signal	V_ain0_core0	HCT_VREF =0.934 V	HCT_VOUT=0.285 V	0.096	0.116	0.136	V
			HCT_VOUT=0.934 V	1.480	1.500	1.520	V
			HCT_VOUT=1.583 V	2.860	2.879	2.900	V
Detection circuit gain	Av_hctin	HCT_VOUT=0.285 to 1.583 V		2.110	2.133	2.150	—
Input offset voltage	ΔV_hctin	HCT_VOUT=HCT_VREF=0.934 V		-10	—	+10	mV
Flow current of input pin	I_hctin	Input voltage=1.5 V		—	—	±5	μA

Comparator block of AC current detection

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Input voltage of AC_CL operation	V_acclref_h	Equivalent to current ±1.960 A	1.31	1.346	1.38	V
	V_acclref_l		0.485	0.522	0.56	V
Input voltage of AC_OC operation	V_acocref_h	Equivalent to current ±2.316 A	1.38	1.417	1.455	V
	V_acocref_l		0.415	0.451	0.495	V
Detection time	t_accl t_acoc	Threshold: Default of DAC Input voltage: Rating -> FS, Including amplifier block	—	—	5	μs

<Operation description>AC current detection

AC current detection circuit is shown in Figure-10. It monitors the output current of the inverter bridge as a value of voltage.
Input voltage (0.285 to 1.583 V) of HCT_VOUT pin is amplified to 2.13 times and input to the internal ADC (AIN0 core0).
To match the input range of ADC, it treats level shift of 1.5 V.
In this time, cutoff frequency of the amplifier circuit is 300 kHz (typ., carrier frequency to 100 kHz), and input offset voltage of the comparator is ±10 mV (max).
Figure-11 shows the monitoring behavior of the logic signal that is output from AC_OC and AC_CL pins.

Equivalent circuit>
Values of internal resistance and capacitor are typical.

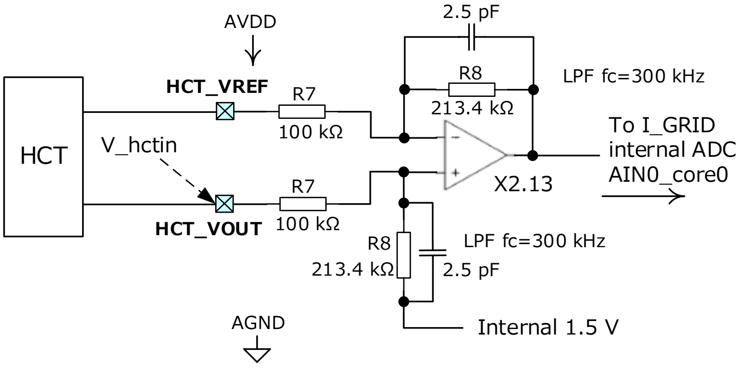


Figure-10

AC current detection and ccomparator outputs (AC_OC and AC_CL)

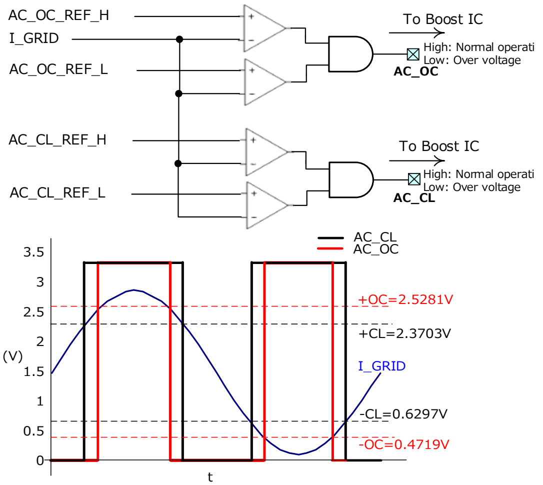


Figure-11

Level of AC current detection (typ.)>

Table-13

Level	Detection current		Input voltage V_hctin	Output voltage V_ain0_core0
	%	A_peak	V	V
-FS	-175	-3.118	0.285	0.1157
-OC	-130	-2.316	0.452	0.4719
-CL	-110	-1.960	0.526	0.6297
-Rating	-100	-1.782	0.563	0.7087
Zero	0	0	0.934	1.5000
Rating	100	+1.782	1.305	2.2913
CL	110	+1.960	1.342	2.3703
OC	130	+2.316	1.416	2.5281
FS	175	+3.118	1.583	2.8843

Approximate equation is as follows;
I/V conversion constant of HCT: 208(mV/A)
Ex.) FS (+175 %):
Input rating 1.26(Arms) -> 100 %: √2 times 1.782(A_peak)
Input voltage V_hctin
=Detection current (A_peak)×208(mV/A)+Level shift voltage (V)
=3.118(A_peak)×208(mV/A)+0.934(V) ≈ 1.583(V_peak)
Output voltage V_ain0_core0
= (V_hctin(V_peak)-Input level shift (V))×Detection circuit gain 2.133+Output level shift (V)
=(1.583-0.934)×2.133+1.5≈2.8843(V)

AC/DC currrent component detection (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-14

Amplifier block of AC/DC current component detection (to IDCERR pin)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Detection circuit gain	Av_idcerr	—	25.3	26	26.7	—

<Operation description> AC/DC current component detection

AC/DC current component detection circuit is shown in Figure-12. It monitors DC component (±2 %) of the output current of the inverter bridge as a value of voltage.

AC current detection voltage (V_ain0_core0) described above is decreased to 2.6/100(-31.7 dB) and reduced by IDCERR_C pin (0.68 µF) and the low pass filter of the internal resistance (180 kΩ (typ.)).

The rest DC component is amplified to 26 times, the rest AC component is cut off by twin T notch filter again, and it is input to the external ADC. In this time, cutoff frequency of amplifier is 1.30Hz (typ., 0.68 µF) and input offset voltage of the amplifier is ±4 mV (max).

Equivalent circuit>

Values of internal resistance and capacitor are typical.

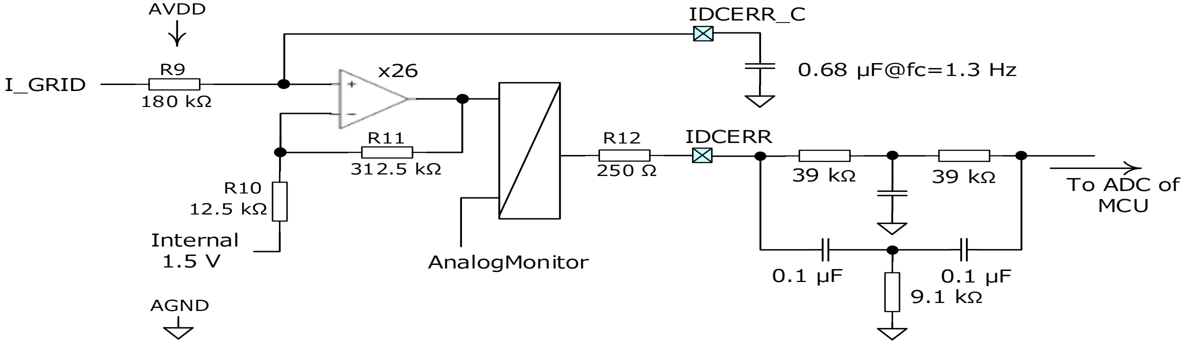


Figure-12

Detection level (typ.) of AC/DC current components

Table 15

Level	Detection current		Detection circuit gain of the prior step	CR(LPF) Decay rate	Detection circuit gain of DC component	Output voltage	Twin-T notch filter	
	%	A_peak				V_idcerr	Decay rate	Output voltage
-FS	-2	-0.0356	2.13	2.6/100	26	0.1535	1/100	1.0798
Rating-1 %	-1	-0.0178				0.3589		1.2852
Zero	0	0				0.5644		1.4906
Rating+1 %	1	0.0178				2.6411		1.7148
+FS	2	0.0356				2.8465		1.9202

Definition of AC/DC current component and approximate equation are as follows;

Input AC rating±1.26 Arms -> Detecting 2 % of ±1.7819 (A_peak) ≈ ±0.0356 (A_peak)

HCT conversion constant: 208(mV/A), First detection circuit gain of G1:2.13 times, decaying AC component by IDCERR_C pin:2.6/100(-31.7 dB)

Detection circuit gain of DC component G2: 26 times

+FS side)

Output voltage V_idcerr= (DC component)+(AC component FS)+Level shift voltage
=Detection current (A_peak)×HCT conversion constant×First detection circuit gain×DC component circuit gain
+AC amplitude×First detection circuit gain×CR decay rate×Latter detection circuit gain+Level shift voltage
=0.0356(A_peak)×208.4(mV/A)×2.13×26+3.118(A_peak)×208.4(mV/A)×2.13×(2.6/100)×26+1.5
=2.8465(V)

-FS side)

Output voltage V_idcerr= (DC component)+(AC component)+Level shift voltage
=(-1)×0.0356(A)×208.4(mV/A)×2.13×26+(-1)×3.118(A_peak)×208.4(mV/A)×2.13*(2.6/100)*26+1.5
=0.1535(V)

Output voltage after passing twin T notch filter is as follows;

Decay rate: When 1/100(-40 dB), "AC component" of second term is 1/100,

+FS side) Output voltage=(DC component)+(AC component)*(1/100)+Level shift voltage=1.9202(V).

-FS side) Output voltage=1.0798(V)

System (AC) voltage detection (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0V)

Table-16

Amplifier block of system (AC) voltage detection

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Output voltage of detection signal	V_vuout V_vwout	V_vuoin=V_vwoin=0.813 V, VO=1.5 V	—	0.125	—	V
		V_vuoin=V_vwoin=VO=1.5 V	1.480	1.500	1.520	V
		V_vuoin=V_vwoin=2.188 V, VO=1.5 V	—	2.875	—	V
Detection circuit gain	Av_uo	Total gain of buffer of the prior step and detection of the latter step	2.00	2.02	2.04	—
Flow current of input pin	I_vuin I_voin I_vwin	VU=VO=VW=1.5 V	—	—	±5	μA

<Operation description> AC voltage detection

AC voltage detection circuit is shown in Figure-13. It monitors the system AC voltage as the value of voltage.
The voltage of AC_U/AC_O/AC_W is divided to 0.37 % (0.125 to 2.875 V) for the resistance of 10kΩ (between VU, VO, and VW pin and AC_REF), and is inputted to buffer circuit (1.01 times). Then, each detection voltage between U and O, and between W and O is amplified to twice by detection circuit and input to internal ADC.
The detection voltage between U and O is outputted to VUO_OUT pin.
In this time, the output voltage offset is ±10 mV (max) under the condition that offset/gain of buffer circuit of the prior step is ±3 mV/1.01 times and offset/gain of detection circuit of the latter step is ±3 mV/2 times.
Cut off frequency of detection circuit of the latter step is 3.4 kHz (typ.).

Equivalent circuit>
The values of internal resistance and capacitor are typical.

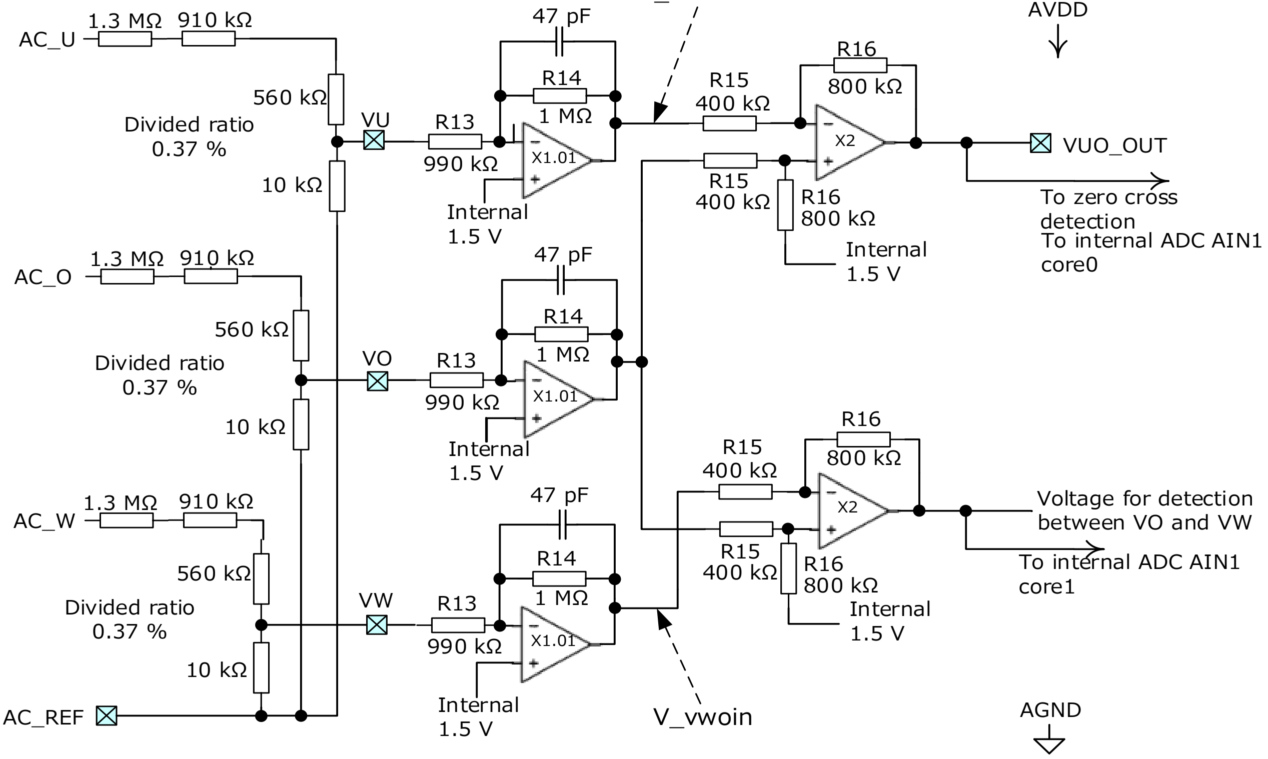
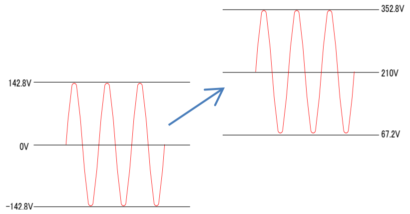


Figure-13

As shown in Figure-14, the center voltage of the detection signal of the AC voltage shifts from 0 V to the middle voltage of the DC voltage before and after the system combination. So, the voltage is amplified twice internally by setting the rate of the AC_U/AC_O/AC_W voltage to 0.37 %.



(Shift of center voltage before and after combination)

Figure-14

Detection level of system (AC) voltage (typ.)>

Table-17

Level	Detection voltage		Input voltage V_vuoin V_vwoin	Output voltage V_ain0_core0 V_ain0_core1
	%	V_peak	V_dc	V_dc
-FS	-130	-185.69	0.813	0.125
-OV	-120	-171.40	0.866	0.231
-Rating	-100	-142.84	0.972	0.442
Zero	0	0	1.500	1.500
Rating	100	142.84	2.029	2.558
OV	120	171.40	2.135	2.769
FS	130	185.69	2.188	2.875

Approximate equation is as follows;
Ex.) FS (130 %):
Rating voltage 101(Vrms) -> 100 %: ×√2= 142.8(V)
Input voltage V_vuoin
=Detection voltage (V_dc)×rate of resistive dividing 0.37 %+level shift
=185.69(V_dc)×(0.37/100)+1.5(V_dc)≈2.187 V
Output voltage V_ain0_core0
= (V_vuoin(V_dc)-Input offset)×Circuit gain+Output offset
≈(2.187-1.5)×2+1.5≈2.875(V)
Relation of input voltage V_vwoin and output voltage (V_ain0_core1) is as same as above equation.

Zero cross detection (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-18

Comparator block of zero cross detection

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Input offset voltage	ΔV_vuofo	Voltage of VUO_FO pin -1.5 V	-20	—	+20	mV

<Operation description>Zero cross detection circuit, second order Sallen-Key type LPF

As shown in Figure-15, Zero cross of AC voltage of the system is detected.
Second order Sallen-Key type LPF is applied for the buffer circuit in the IC (between VUO_FIN pin and VUO_FO pin) and the comparator (between L_HZD_HYS pin and L_HZO pin).
Cut off frequency is set by the external parts (C0, C1, R0, and R1), and the hysteresis of avoiding chattering is set by the external parts (C2, R2, R3, R4, and R5).

Equivalent circuit>

The values of internal resistance and capacitor are typical.

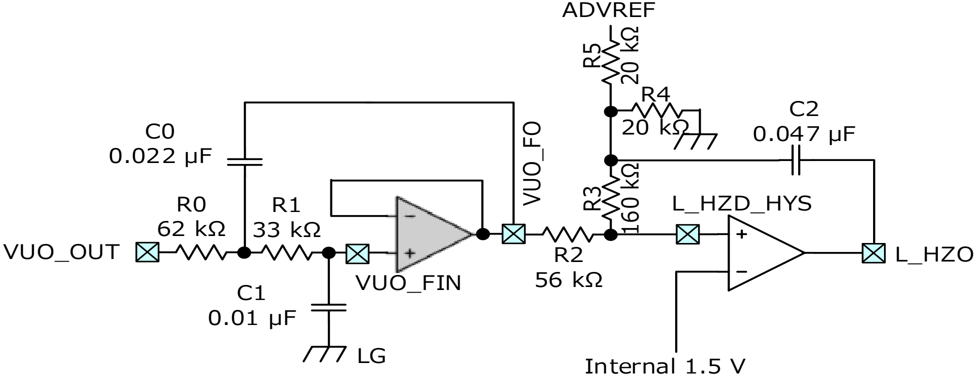


Figure-15

Operation waveform>

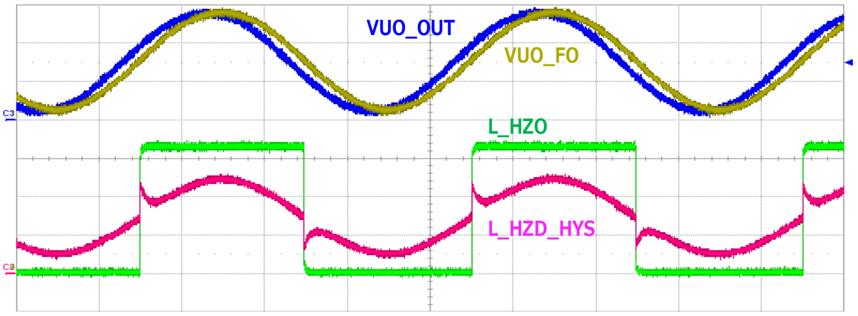


Figure-16

Setting threshold for comparator DAC (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-19

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
DC over current detection level	DC_OC_REF	1Step=0.18 A	3.283	3.570	3.839	A
DC over voltage detection level	DC_OV_REF	1Step=2.58 V	500.8	545.3	587.1	V
AC over current detection level	AC_OC_REF	1Step=0.026 A	±1.901	±2.323	±2.719	A
AC limit current detection level	AC_CL_REF	1Step=0.026 A	±1.558	±1.980	±2.376	A

<Operation description> Setting threshold for comparator DAC

Threshold values of over current detection and over voltage detection (DC_OC, DC_OV, AC_CL, and AC_OC) are configured.
The setting voltage can be monitored by I_INV pin by setting S/P interface.

Block diagram>

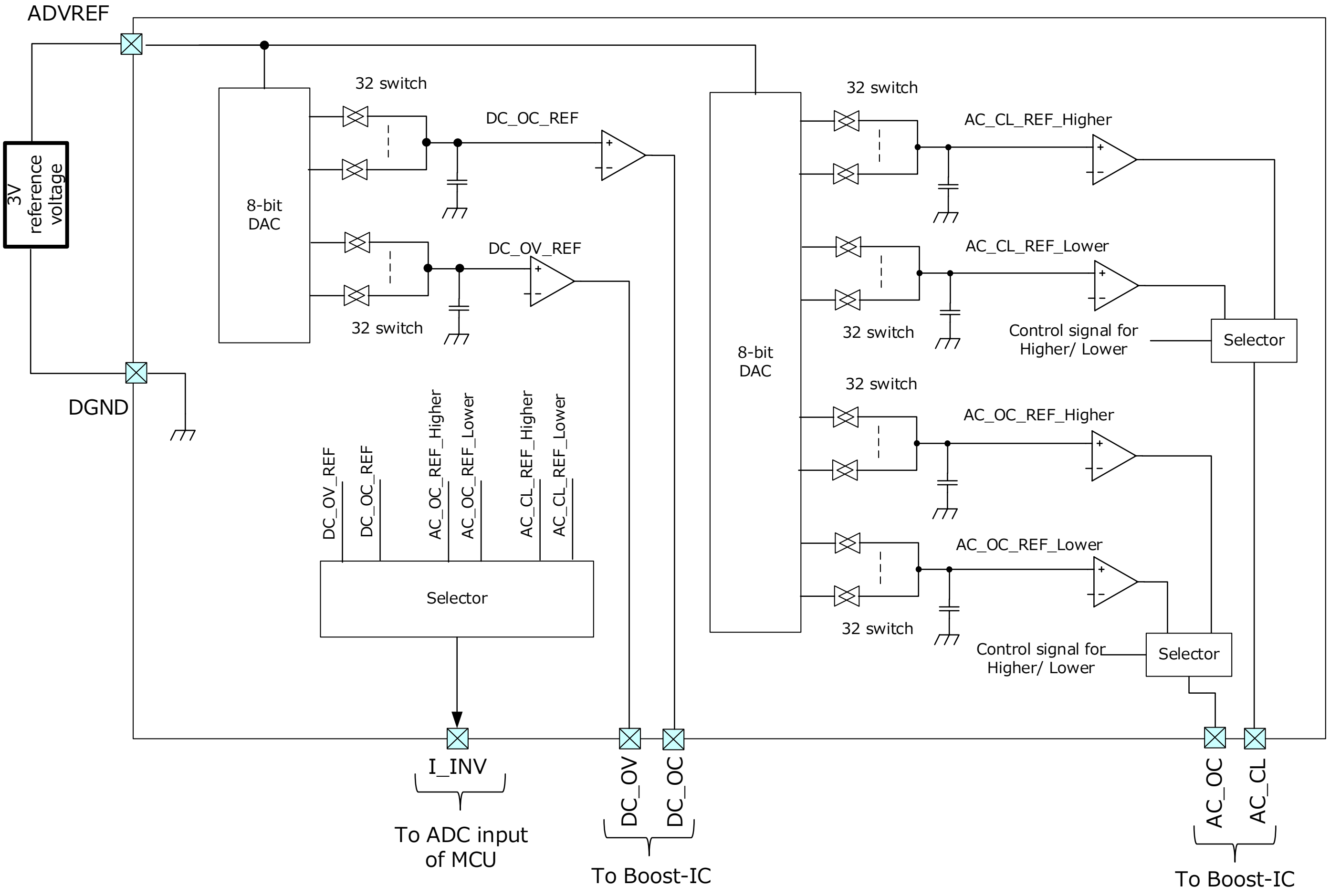


Figure-17

Setting value of threshold (DAC) for comparator (reference)>

DC over current Detection level setting range: Default setting=Setting 16>

Table-20

Setting		DC_OC_REF	Detection current
DEC	BIN	V_dc	A_dc
0	00000	2.344	**3.283**
1	00001	2.355	3.301
2	00010	2.367	3.319
3	00011	2.379	3.337
4	00100	2.391	3.355
5	00101	2.402	3.373
6	00110	2.414	3.391
7	00111	2.426	3.409
8	01000	2.438	3.427
9	01001	2.449	3.445
10	01010	2.461	3.463
11	01011	2.473	3.481
12	01100	2.484	3.498
13	01101	2.496	3.516
14	01110	2.508	3.534
15	01111	2.520	3.552
16	**10000**	**2.531**	**3.570**
17	10001	2.543	3.588
18	10010	2.555	3.606
19	10011	2.566	3.624
20	10100	2.578	3.642
21	10101	2.590	3.660
22	10110	2.602	3.678
23	10111	2.613	3.696
24	11000	2.625	3.714
25	11001	2.637	3.732
26	11010	2.648	3.750
27	11011	2.660	3.768
28	11100	2.672	3.786
29	11101	2.684	3.804
30	11110	2.695	3.822
31	11111	2.707	**3.839**

DC over voltage Detection level setting range: Default setting= Setting 16>

Table-21

Setting		DC_OV_REF	Detection voltage
DEC	BIN	V_dc	V_dc
0	00000	2.109	**500.8**
1	00001	2.121	503.6
2	00010	2.133	506.4
3	00011	2.145	509.1
4	00100	2.156	511.9
5	00101	2.168	514.7
6	00110	2.180	517.5
7	00111	2.191	520.3
8	01000	2.203	523.1
9	01001	2.215	525.8
10	01010	2.227	528.6
11	01011	2.238	531.4
12	01100	2.250	534.2
13	01101	2.262	537.0
14	01110	2.273	539.8
15	01111	2.285	542.5
16	**10000**	**2.297**	**545.3**
17	10001	2.309	548.1
18	10010	2.320	550.9
19	10011	2.332	553.7
20	10100	2.344	556.4
21	10101	2.355	559.2
22	10110	2.367	562.0
23	10111	2.379	564.8
24	11000	2.391	567.6
25	11001	2.402	570.4
26	11010	2.414	573.1
27	11011	2.426	575.9
28	11100	2.438	578.7
29	11101	2.449	581.5
30	11110	2.461	584.3
31	11111	2.473	**587.1**

AC over current Detection level setting range: Default setting=Setting 16>

Table-22

Setting		AC_OC_REF		Detection current	
		Higher	Lower	Higher	Lower
DEC	BIN	V_dc	V_dc	A_peak	A_peak
0	00000	2.344	0.656	**1.901**	**-1.901**
1	00001	2.355	0.645	1.927	-1.927
2	00010	2.367	0.633	1.954	-1.954
3	00011	2.379	0.621	1.980	-1.980
4	00100	2.391	0.609	2.006	-2.006
5	00101	2.402	0.598	2.033	-2.033
6	00110	2.414	0.586	2.059	-2.059
7	00111	2.426	0.574	2.086	-2.086
8	01000	2.438	0.563	2.112	-2.112
9	01001	2.449	0.551	2.138	-2.138
10	01010	2.461	0.539	2.165	-2.165
11	01011	2.473	0.527	2.191	-2.191
12	01100	2.484	0.516	2.218	-2.218
13	01101	2.496	0.504	2.244	-2.244
14	01110	2.508	0.492	2.270	-2.270
15	01111	2.520	0.480	2.297	-2.297
16	**10000**	**2.531**	**0.469**	**2.323**	**-2.323**
17	10001	2.543	0.457	2.350	-2.350
18	10010	2.555	0.445	2.376	-2.376
19	10011	2.566	0.434	2.402	-2.402
20	10100	2.578	0.422	2.429	-2.429
21	10101	2.590	0.410	2.455	-2.455
22	10110	2.602	0.398	2.482	-2.482
23	10111	2.613	0.387	2.508	-2.508
24	11000	2.625	0.375	2.534	-2.534
25	11001	2.637	0.363	2.561	-2.561
26	11010	2.648	0.352	2.587	-2.587
27	11011	2.660	0.340	2.614	-2.614
28	11100	2.672	0.328	2.640	-2.640
29	11101	2.684	0.316	2.666	-2.666
30	11110	2.695	0.305	2.693	-2.693
31	11111	2.707	0.293	**2.719**	**-2.719**

AC limit current Detection level setting range: Default setting=Setting 16>

Table-23

Setting		AC_CL_REF		Detection current	
		Higher	Lower	Higher	Lower
DEC	BIN	V_dc	V_dc	A_peak	A_peak
0	00000	2.191	0.809	**1.558**	**-1.558**
1	00001	2.203	0.797	1.584	-1.584
2	00010	2.215	0.785	1.610	-1.610
3	00011	2.227	0.773	1.637	-1.637
4	00100	2.238	0.762	1.663	-1.663
5	00101	2.250	0.750	1.690	-1.690
6	00110	2.262	0.738	1.716	-1.716
7	00111	2.273	0.727	1.742	-1.742
8	01000	2.285	0.715	1.769	-1.769
9	01001	2.297	0.703	1.795	-1.795
10	01010	2.309	0.691	1.822	-1.822
11	01011	2.320	0.680	1.848	-1.848
12	01100	2.332	0.668	1.874	-1.874
13	01101	2.344	0.656	1.901	-1.901
14	01110	2.355	0.645	1.927	-1.927
15	01111	2.367	0.633	1.954	-1.954
16	**10000**	**2.379**	**0.621**	**1.980**	**-1.980**
17	10001	2.391	0.609	2.006	-2.006
18	10010	2.402	0.598	2.033	-2.033
19	10011	2.414	0.586	2.059	-2.059
20	10100	2.426	0.574	2.086	-2.086
21	10101	2.438	0.563	2.112	-2.112
22	10110	2.449	0.551	2.138	-2.138
23	10111	2.461	0.539	2.165	-2.165
24	11000	2.473	0.527	2.191	-2.191
25	11001	2.484	0.516	2.218	-2.218
26	11010	2.496	0.504	2.244	-2.244
27	11011	2.508	0.492	2.270	-2.270
28	11100	2.520	0.480	2.297	-2.297
29	11101	2.531	0.469	2.323	-2.323
30	11110	2.543	0.457	2.350	-2.350
31	11111	2.555	0.445	**2.376**	**-2.376**

12-bit ADC and Boost-IC interface (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-24

12-bit SAR AD converter

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Integral non-linearity error	INL	—	-11	—	11	LSB
Differential non-linearity error	DNL					
<Reference value>						
Integral non-linearity error	INL	Mounted on board	-5	—	5	LSB
Differential non-linearity error	DNL		-4	—	4	LSB

Internal PLL

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Internal main clock	f_asclk	External clock f_mclk=10 MHz	38	40	42	MHz

<Operation description> 12-bit ADC and Boost-IC interface

System AC voltage (W-O side, U-O side), AC current, and DC voltage are sampled by two ADC cores (core0 and core1).

- Core0 outputs sampling data of AC current to system AC voltage (U-O side) from DOUT0 continually.
- Core1 outputs sampling data of DC voltage to system AC voltage (W-O side) from DOUT1 continually.

Connection of AD converter and each analog input>

Table-25

ADC core	Input AIN0	Input AIN1
0	System AC current	System AC voltage (U-O side)
1	DC voltage	System AC voltage (W-O side)

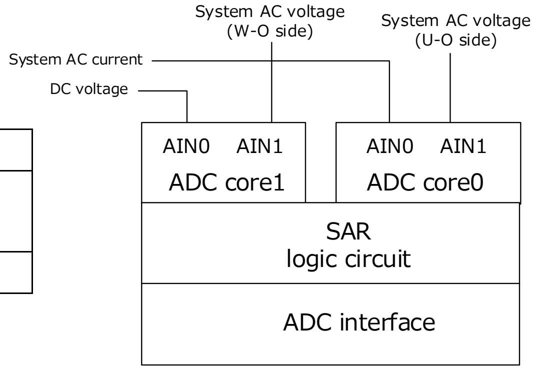


Figure-18

AD converter Output table of DOUT0 and DOUT1>

Table-26

DOUTn	Setting function	Setting description
ADF	AD converter / Identification flag	0=ADC0, 1=ADC1
D[11:0]	Sampling data (MSB fast, 24-bit data)	DOUT0=AC current (HCT) -> system AC voltage (U-O side)
		DOUT1= DC voltage -> System AC voltage (W-O side)

Input timing>

Recommended timing of ADST pin that is a trigger of starting ADC is as follows;
Input S/P interface waveform which matches this timing.

Table-27

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
External clock	f_mclk	—	—	10	—	MHz
Pulse width of ADC start trigger	tadst	From rising edge of ADST to falling edge of ADST	71.2	—	210	ns

Output timing>

Output I/F of ADC generates internal main clock (f_asclk=40 MHz) from the frequency of 10 MHz to the external reference clock (f_mclk) as IP and operates at the following output timing. Detail timing chart is shown in the next page.

Table-28

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
ADC transfer clock High level time	thadclk	ADCLK	23.8	25	26.3	ns
ADC transfer clock Low level time	tladclk	ADCLK	23.8	25	26.3	ns
ADC sampling hold time	tadsh	—	238	250	272	ns
ADC data delay time	tsu	ADCLK to DOUT0 and DOUT1	0	—	20	ns
Conversion time	tconv	ADC internal clock 40 MHz±5 %	0.879	0.925	1.07	µs
	tconvall		1.76	1.85	1.94	µs

Boost-IC interface timing chart>

The sampling result of each AD convertor is outputted from DOUT0 and DOUT1 in synchronization with ADCLK by triggering High level pulse of ADST pin.

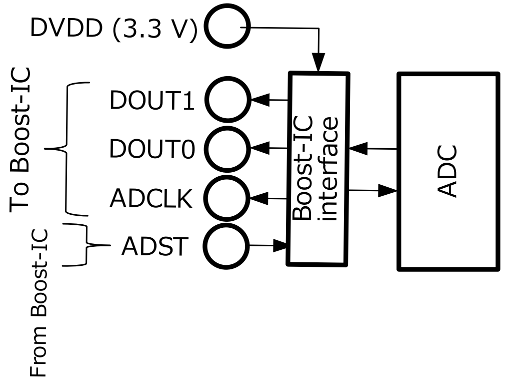


Figure-19

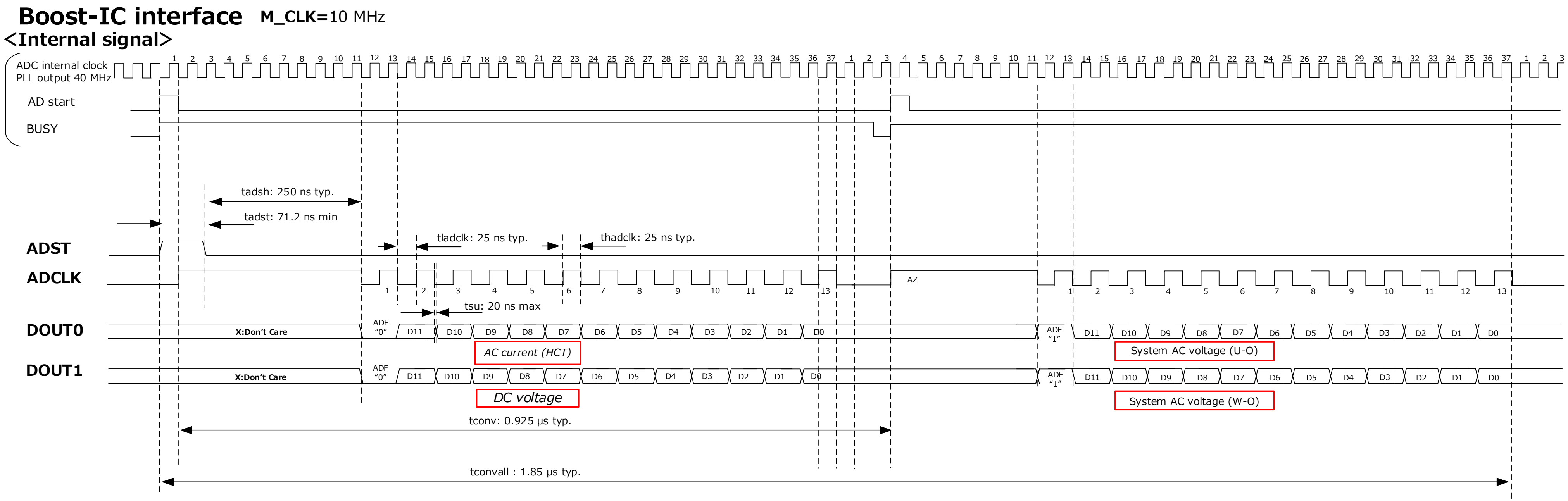


Figure-20

S/P interface Timing condition (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Table-29

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
SCLK frequency	fsclk	—	—	—	10	MHz

<Operation description> Frame format of S/P interface (slave)

S/P interface uses three pins of CSN, SCLK, and DIN. If is slave-only interface to set each configuration of the TC7717FTG and the register for a test.

Input format supports only general transfer format of 16-bit serial data.

1-bit of MSB: Wire only (=1) -> 7 bits (A[6:0]): Register address setting -> 8 bits (D[7:0]): Each data setting

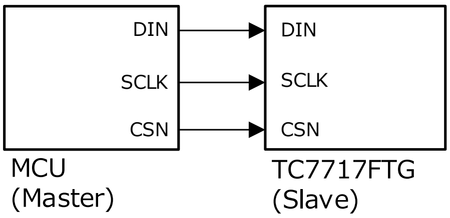
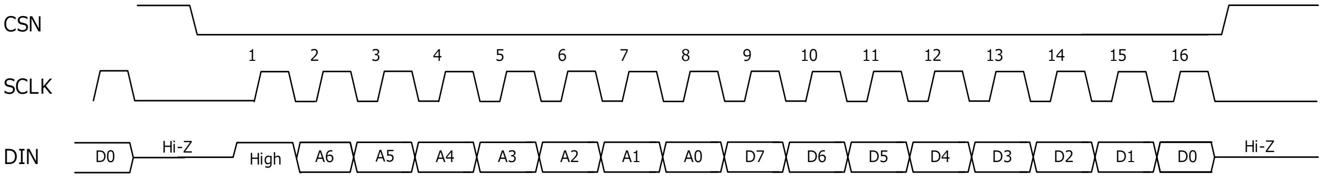


Figure-21

CSN pin: Low active

DIN pin: Always input. When the transmitting side turns off output during non-transmission, fix the output level with Pull-up/Pull-down resistance.



Timing chart>

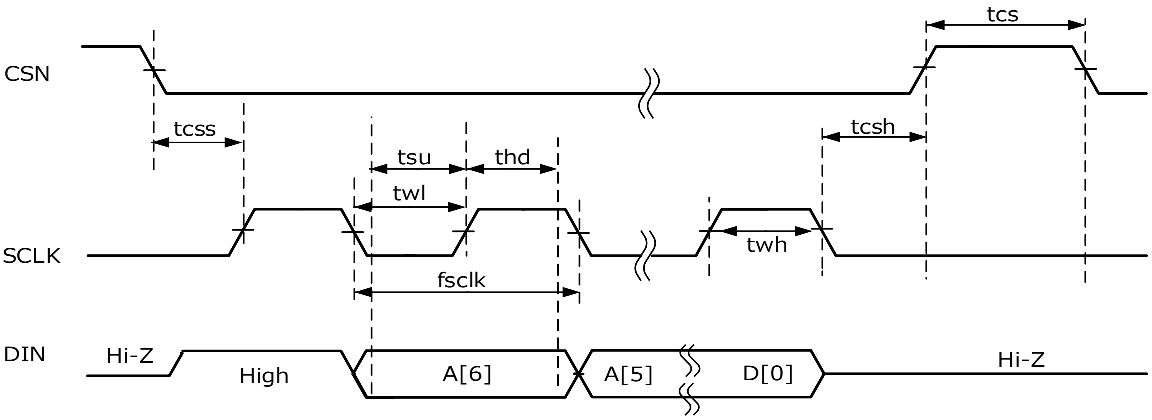


Figure-22

Input timing condition>

Recommended timing corresponding to SCLK frequency (fsclk=10 MHz) is as follows;

Input S/P interface waveform which matches this timing.

Table-30

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Waiting time from CSN↓ to SCLK↑	tcss	For S/P interface 10 MHz	100	—	—	ns
Setup time of DIN and SCLK↑	tsu		50	—	—	ns
Hold time of SCLK↑ and DIN	thd		50	—	—	ns
Waiting time from SCLK↓ to CSN↑	tcsh		100	—	—	ns
Input Low time of SLCK	twl		0.025	—	500	µs
Input High time of SLCK	twh		0.025	—	500	µs
Input High time of CSN	tcs		100	—	—	ns

Data table of S/P interface (slave) (1)

Mode setting register

Table-31

Register name	Address									Data and each register name							
	R/W	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0
Mode setting register (1)	1	0	0	0	0	0	0	1	01	Used by vender	—	—	ACPATHS	DACSEL1	DACSEL0	ADC_en	SOFTRST
Register value in initial mode and external RSTN=Low (reset)										0	0	0	0	0	0	0	0
Description and remark of each register										It is an unused register in the normal operation. D7 is used in the vendor side. And so all inputs are set low in the normal operation.			It commands pass of the internal amplifier in AC voltage detection. 0: Normal operation 1:Amplifier through	It selects the judging level setting DAC of each detection 00: DC_OC_REF 01: DC_OV_REF 10: AC_OC_REF 11: AC_CL_REF		It controls AD conversion of internal ADC. 0: Stop conversion 1: Capable of conversion	For software reset 0: Normal operation 1: Reset (register set is cleared)

Setting register of judging level DAC for each detection comparator

Register name	Address									Data							
	R/W	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0
DAC setting register	1	0	0	0	0	0	1	0	02	—	—	—	DAC4	DAC3	DAC2	DAC1	DAC0
Register value in initial mode and external RSTN=Low (reset)										0	0	0	1	0	0	0	0
Description and remark of each register										It sets voltage of DAC. D[7:5]: All=0, D[4:0]: Each DAC voltage is set							

Setting register of analog monitor

Register name	Address									Data							
	R/W	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0
Analog monitor setting register	1	0	0	0	0	0	1	1	03	—	—	—	Used by vender	INVSEL3	INVSEL2	INVSEL1	INVSEL0
Register in initial mode and in external RSTN=Low (reset)										0	0	0	0	0	0	0	1
Description and remark of each register										It is an unused register in the normal operation. D4 is used in the vendor side. And so all inputs are set 0 in the normal operation.				It monitors the operation by I_INV pin and selects the reference voltage of each detection comparator. 0000: I_INV, 0001:PLL_LOCK flag 0010: DC_OC_REF, 0011:DC_OV_REF, 0100: AC_OC_REF_H, 0101:AC_OC_REF_L, 0110: AC_CL_REF_H, 0111:AC_CL_REF_L, 1000 to 1111 are used in the vendor side. Input is forbidden in the normal operation.			

PLL setting register

Register name	Address									Data							
	R/W	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0
PLL setting register	1	0	0	0	0	1	0	1	05	—	—	—	—	PLL_FIL1	PLL_FIL0	PLL_WIDR1	PLL_WIDR0
Register in initial mode and in external RSTN=Low (reset)										0	0	0	0	1	0	0	1
Description and remark of each register										It is an unused register in the normal operation. All inputs are set 0.				It sets time constant of PLL lock. 00: 51.2 µs, 01: 102 µs 10: 205 µs, 11: 410 µs		It sets window of PLL_LOCK flag. 00: ±1.56 %, 01: ±3.13 %, 10: ±6.25 %, 11: ±12.5 %	

Data table of S/P interface (slave) (2)

Trimming register of reference voltage (ADVREFO pin voltage)

Table-32

Register name	Address									Data and each register name							
	R/W	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0
Trimming register of reference voltage	1	0	0	0	0	1	1	0	06	ADREFTMP2	ADREFTMP1	ADREFTMP0	ADREFT4	ADREFT3	ADREFT2	ADREFT1	ADREFT0
Register in initial mode and in external RSTN=Low(reset)										1	0	0	1	0	0	0	0
Recommended register value										0	1	1	1	0	0	1	0
Description and remark of each register When using this reference voltage (ADVREFO pin), set the registers according to the values in the right columns, and connect to the reference voltage ADVREF pin of the ADC. It supplies about 2.997 V with this recommendation setting.										It adjusts the temperature characteristics of internal reference voltage (ADREFTO (3.0 V)). Set as follows; ADREFTMP[2:0]=011			It adjusts the absolute voltage of internal reference voltage (ADREFTO (3.0 V)). Set as follows; ADREFT[4:0]=10010				

Register not used during normal operation

Register name	Address									Data and each register name							
	R/W	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0
N/A	0	X	X	X	X	X	X	X	XX	—	—	—	—	—	—	—	—
Use vendor	0	0	0	0	0	1	0	0	04	—	—	—	—	—	—	—	—
Register in initial mode and in external RSTN=Low(reset)										0	0	0	0	0	0	0	0
Description and remark of each register										It is an unused register. It is forbidden to input in the normal operation							

As for address setting except above table (Read mode), input is forbidden because it is not used in the normal operation.

Operation of PLL lock flag>

Main control starts after PLL lock of the TC7717FTG is confirmed by MCU. The PLL lock flag is output recognized as the default output of I_INV pin.

Table-33

Characteristics	Condition	Operation
PLL lock flag	Initial state	PLL lock flag is output from I_INV pin.
	PLL lock: incomplete	I_INV="Low"
	PLL lock: complete	I_INV="High"

*: As for time constant of PLL lock and flag window, refer to PLL setting register (05h) of S/P interface.

Each function of reset signal (RSTN pin) and UVLO (AVDD pin) (Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.3 V, ADVREF=3.0 V, AGND=DGND=DC_LG=SH_LG=0 V)

Each function of Reset signal and UVLO operating>

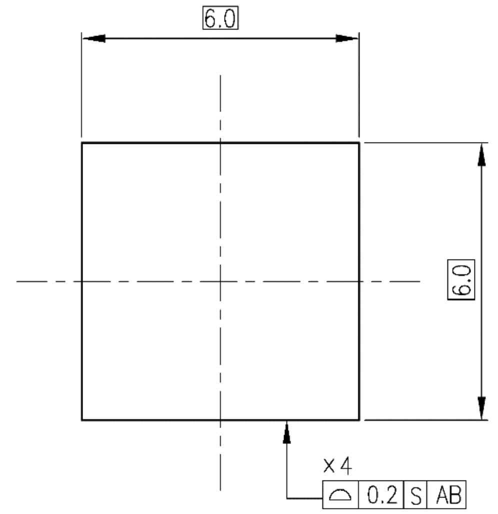
Table-34

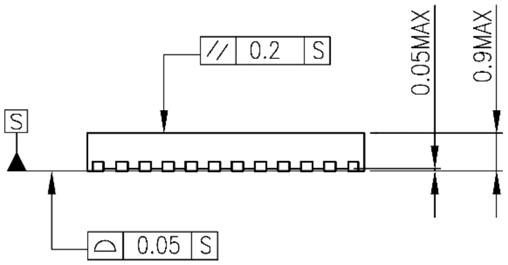
In case of RSTN=Low	Operation of each function
Release reset	Main power supply is connected. Internal circuit starts operation when RSTN outputs from low to high level.
Operation level of reset	It operates as same in the UVLO detection of AVDD (Refer to Page 14).
Register of sampling relation of ADC	All operations: Low, DOUT0 and DOUT1=ADCLK=Low or X (indefinite)
Setting contents from S/P interface	All operations are initialized to default. Data setting is not configured even if a signal is input with S/P interface.
I_INV	It returns to output of PLL flag monitor and outputs low.
Oscillation circuit of PLL circuit and others	Operation of PLL circuit is not in the standby mode if AVDD is applied.
Comparator output	All operations: High
AC_REF(1.5 V) and VDIG	It outputs the voltage of 1.5 V. (VDIG is the same.)
Standby function	Operation of analog circuit is not in the standby mode (voltage cut) if AVDD is applied.

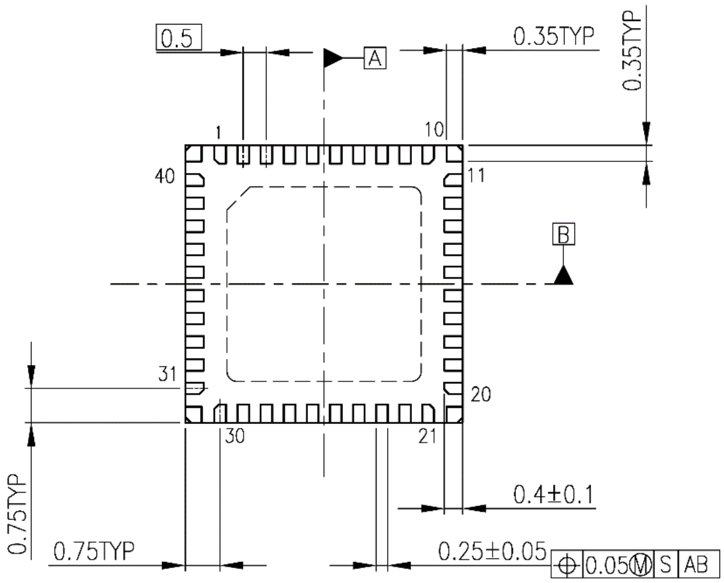
Package dimensions

P-VQFN40-0606-0.50-001

Unit: mm







Weight: 97.6 mg (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
Providing these application circuit examples does not grant a license for industrial property rights.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

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