High-Power Device
PMI: Plastic Module IEGT
PPI: Press Pack IEGT
Application Note
# Table of Contents

1. Structure and Features ................................................................. 4
   1.1. IEGT ......................................................................................... 5
   1.2. IEGT Features ......................................................................... 5
   1.3. IGBT Cross Section Structure and Voltage Resistance Enhancement Issues ........................................... 5
   1.4. IEGT Gate Structure Features and IE Effect Application ............................................................................ 5
   1.5. Press Pack Type IEGT Device PPI (Press Pack IEGT) .................................................................................. 6
   1.6. PPI Features ............................................................................ 6
   1.7. Plastic Case Module Type IEGT Device PMI (Plastic Case Module IEGT) ...................................................... 8
   1.8. PMI Features ......................................................................... 8

2. Terms and Characteristics ............................................................ 9
   2.1. How to Read Data ..................................................................... 10
   2.2. Maximum Ratings .................................................................... 14
   2.3. Electrical Characteristics ........................................................ 16

3. Handling Precautions (When Using Semiconductor Products) .......... 18
   3.1. IEGT Device Selection .............................................................. 18
   3.2. Electrostatic Discharge and Gate Protection .................................................................................................. 19
   3.3. Protection Circuit Design .......................................................... 20
   3.4. Thermal Design ....................................................................... 20
   3.5. Drive Circuit Design ................................................................. 20
   3.6. Parallel Connection ................................................................... 20
   3.7. Mounting Precautions ............................................................... 21
   3.8. Storage and Transportation Precautions ..................................... 21
   3.9. Reliability Precautions (Lifetime Design) .................................... 22
   3.10. Other Notes on Handling Precautions ........................................ 22

4. Protection Circuit Design Methods ............................................... 24
   4.1. Surge Voltage Protection ........................................................ 24
   4.2. Short Circuit Protection ........................................................... 25

5. Thermal Design and Mounting on Thermal Fins .......................... 27
   5.1. Principles of Heat Dissipation ................................................... 27
       5.1.1. Radiation Equivalent Circuit .............................................. 27
       5.1.2. Loss Calculation ................................................................. 27
       5.1.3. Junction Temperature Pulse Response .................................. 28
   5.2. Press Pack Type IEGT ............................................................... 29
       5.2.1. Heat Sink Design .............................................................. 29
       5.2.2. Confirmation of Press Pack Conditions ................................ 31
       5.2.3. Maximum Allowable Power of Press Pack Type IEGT .......... 32
       5.2.4. Maximum Allowable Power of Press Pack Type IEGT and TFT Tolerance ........................................... 32
   5.3. Module Type IEGT ................................................................. 33
1. Structure and Features

IEGT is a voltage-driven power device for switching high current. To enhance IGBT voltage resistance, the on-state voltage will sharply increase. In IEGT, devising the device structure on the emitter side has solved the problem, thereby achieving low on-state voltage characteristics. The basic structure and equivalent circuit of a base N-channel IGBT are shown in Figure 1.1. The structure is similar to MOSFET. The basic difference is that it adopts a P⁺-N⁺-N⁻ substrate whereas MOSFET uses an N⁺-N⁻ substrate. Therefore, its manufacturing processes after the substrate process are basically the same as for MOSFET.

On the equivalent circuit, a thyristor is formed by PNP-NPN transistor coupling. However, as shown in the structure diagram, the base and emitter of the NPN transistor are short-circuited with Al wiring and are designed to operate as little as possible. The thyristor does not normally affect IGBT’s basic operation. Hence, the equivalent circuit and operating mechanism of the N-channel IGBT can be considered as the same as the MOS input inverted Darlington with the N-channel enhancement-type MOSFET at the input stage and the PNP transistor at the output stage.

However, the IGBT features are not just limited to the behaviors described for the equivalent circuit. Another important feature is the conductivity modulation of the N' edge region due to the monolithic configuration of the MOSFET and the PNP transistor. Conductivity modulation (decrease in MOSFET drain resistance) is induced in the N' layer by holes (minority carriers) injected from the P⁺-N⁺ layer into the N⁻ layer. With this conductivity modulation mechanism, the IGBT can obtain low saturation voltage characteristics, which were difficult to obtain from the highly voltage resistant MOSFET.

IGBT's saturation voltage \( V_{ce(sat)} \) from the equivalent circuit can be expressed as follows:

\[
V_{ce(sat)} = V_{BE} + I_{MOS} \left[ R_{N-(MOD)} + R_{ch} \right]
\]

In addition, the relationship of the current between the MOSFET and the PNP transistor can be expressed as:

\[
I_{MOS} = I_{IGBT} / (h_{FE} + 1)
\]

The PNP transistor's \( h_{FE} \) strongly affects the trade-off relationship between the saturation voltage and the switching characteristics of the IGBT.

Figure 1.1 Basic Structure and Equivalent Circuit
1.1. IEGT

IEGT is a voltage-driven power device for switching high current. To enhance IGBT voltage resistance, the on-state voltage will sharply increase. In IEGT, devising the device structure on the emitter side has solved the problem, thereby achieving low on-state voltage characteristics. Furthermore, due to its good shut-off capability and high breakdown tolerance, it contributes to energy saving, miniaturization, and efficiency improvement of equipment. It demonstrates its performance in industrial fields that support social infrastructure such as drive equipment and power converters. Press-pack type and module type packages are available and either can be selected according to the power capacity and load characteristics of the application.

IEGT: Injection Enhanced Gate Transistor

1.2. IEGT Features

- High breakdown voltage, low on-resistance
- Wide safety operating area (high di/dt, dv/dt tolerance) as with an IGBT
- Simplification and miniaturization of drive circuit by voltage driving
- High speed switching operation

1.3. IGBT Cross Section Structure and Voltage Resistance Enhancement Issues

Figure A shows the cross-section structure of a conventional IGBT and its carrier distribution in the N-base. The carrier distribution decreases monotonically from the collector electrode side to the emitter electrode side. To enhance voltage resistance, it is necessary to widen the N-base region between the collector and the emitter, so the region of minority carriers becomes thick and increases resistance, thus increasing the voltage drop. There was a problem that the on-state voltage was higher.

1.4. IEGT Gate Structure Features and IE Effect Application

Figure B shows the cross-section structure and carrier distribution of an IEGT. Compared to IGBTs, the IEGT has deep and wide trench gate electrodes, which increase the carrier density inside the device and prevent carriers from passing to the emitter electrode. Consequently, carrier accumulation occurs and N-base carrier distribution increases on the emitter electrode side. Since this has the same effect as carrier injection and accumulation, it is called the Injection Enhancement (IE) effect. With this gate structure adopted, it is now possible to suppress an increase in voltage drop even while enhancing voltage resistance.

* Another structure which can produce a similar effect is currently being developed and adopted.
1.5. Press Pack Type IEGT Device PPI (Press Pack IEGT)

All electrical connections use press pack. Since wire bonding connections are not used, high reliability against thermal fatigue can be expected. Using several serial connections of PPIs ensures uninterrupted operation of the equipment even when the product fails due to electrical damage. This is because the collector and the emitter electrodes will be short-circuited. Using a double-sided heat dissipation structure can cool down both the collector and the emitter sides. The device has high moisture resistance due to its hermetic sealing structure in a ceramic and metal enclosure, so it can be directly immersed in cooling liquid for efficient cooling.

1.6. PPI Features

- **Electrical connections using press pack**
  IEGT chips are arranged on the same plane and are then uniformly pressed from both sides using a molybdenum plate. The collector and emitter electrodes of the chip come into contact with the respective copper electrodes via the molybdenum plate when mechanical pressure is applied. This makes electrical connections and allows heat dissipation.

- **High reliability due to a hermetic sealing structure**
  Inert gas is hermetically sealed inside the device to prevent degradation of the electrode surface due to oxidation, ensuring high thermal reliability for PPIs.

- **Outstanding parallel operation technology**
  The wiring inside the gate terminal plate is designed to operate a number of parallel-connected IEGT chips consistently so that they do not interfere with each other and oscillate during switching.

- **Rupture-resistant package structure**
  The resin-frame structure that guides the IEGT chip makes the package less prone to rupture even if a chip is melted and destroyed during a switching operation.
PPI structure

PPI cross-sectional schematic diagram
1.7. Plastic Case Module Type IEGT Device PMI (Plastic Case Module IEGT)

PMI can be attached to the cooling fin with screws, simplifying equipment assembly. It incorporates a base plate (Al-SiC) with a low thermal expansion coefficient and has an optimal internal structure and parts. Therefore, it is less susceptible to thermal fatigue and provides an improved power cycling capability for prolonged service life. The package uses a high CTI* material that is less sensitive to tracking breakdown to improve isolation voltage on the package surface.

*CTI: Comparative Tracking Index

1.8. PMI Features

- Easy-to-assemble modular plastic casing
  Multiple IEGT chips are soldered on a ceramic insulating board and wire-bonded to their respective terminals. The plastic module is easy to use because it dissipates heat from one side and is internally insulated.

- Base plate made from composite Al-SiC material
  To ensure thermal reliability, the package uses a composite Al-SiC (Aluminum Silicon-Carbide) material with low thermal expansion coefficient aluminum and silicon carbide on the metal plate of its underside.
2. Terms and Characteristics

Taking MG1500FXF1US62 as an example of the characteristics of an IEGT module, the data described in the technical documents such as a datasheet is explained below.

**Format**

The IEGT PMI and PPI product names are configured as follows:

**PMI**

<table>
<thead>
<tr>
<th>MG 1500 FXF 1US 62</th>
</tr>
</thead>
<tbody>
<tr>
<td>Characteristic serial number</td>
</tr>
<tr>
<td>Chip type</td>
</tr>
<tr>
<td>Device configuration</td>
</tr>
<tr>
<td>Number of devices (or number of terminals)</td>
</tr>
<tr>
<td>Maximum voltage ratings</td>
</tr>
<tr>
<td>Current rating</td>
</tr>
<tr>
<td>Module topology</td>
</tr>
</tbody>
</table>

**PPI**

<table>
<thead>
<tr>
<th>ST 2100 GXH 24 A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device configuration</td>
</tr>
<tr>
<td>Characteristic serial number</td>
</tr>
<tr>
<td>Maximum voltage ratings</td>
</tr>
<tr>
<td>Current rating</td>
</tr>
<tr>
<td>Press pack topology</td>
</tr>
</tbody>
</table>

The meaning of the third item is as follows:

<table>
<thead>
<tr>
<th>Letters of the third part</th>
<th>Maximum voltage range (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>1400 to less than 1500</td>
</tr>
<tr>
<td>T</td>
<td>1500 to less than 1600</td>
</tr>
<tr>
<td>U</td>
<td>1600 to less than 1700</td>
</tr>
<tr>
<td>V</td>
<td>1700 to less than 1800</td>
</tr>
<tr>
<td>W</td>
<td>1800 to less than 1900</td>
</tr>
<tr>
<td>X</td>
<td>1900 to less than 2000</td>
</tr>
<tr>
<td>Y</td>
<td>2000 to less than 2100</td>
</tr>
<tr>
<td>FXF</td>
<td>3300</td>
</tr>
<tr>
<td>GXH</td>
<td>4500</td>
</tr>
<tr>
<td>JX</td>
<td>6000</td>
</tr>
</tbody>
</table>
Meaning of Characteristic Data

Each IEGT module usually contains IEGTs and freewheeling diodes (FWD). Static loss and dynamic loss occur for each device during switching operations. Static loss is the loss when each of IEGTs and FWDs is in the on-state. Dynamic loss is the loss that occurs at the moment each switches from the on-state to the off-state, or vice versa.

The data related to static loss are $I_{C}-V_{CE}$, output characteristics, and $I_{F}-V_{F}$.

The data related to dynamic loss are $E_{on}-I_{C}$, $E_{off}-I_{C}$, $E_{dsw}-I_{F}$, $E_{on}-R_{G(on)}$, $E_{off}-R_{G(off)}$, and $E_{dsw}-R_{G(on)}$.

The data necessary for the IEGT drive circuit’s capacitance design are $C_{ss}$, $C_{oss}$, $C_{res}-V_{CE}$, and $V_{GE}-Qg$. The data related to the timing of an ON signal input to the drive circuit are $t_{o(on)}$, $t$, $t_{o(off)}$, $t_{r}-I_{C}$, $t_{rr}$, and $I_{r}-I_{F}$.

The data related to thermal design is $R_{th(j-c)}$.

The data related to the breakdown mode by a loss due to surge voltage generated at the moment when an IEGT turns OFF is RBSOA. The data related to the breakdown strength during an FWD reverse recovery operation is called RRSOA.

2.1. How to Read Data

(1) $I_{C}-V_{CE}$

This data shows the relationship between the C-E current ($I_{C}$) and the drop voltage between the collector and emitter ($V_{CE}$) when +15 V is applied between the gate and emitter and the device is turned ON. The on-state power loss ($P_{sat}$) when the device is ON can be calculated by multiplying the supplied current $I_{C}$ and the drop voltage ($V_{CE}$) for operating time. Since the device temperature rises during operation, use the curve for $T_{j} = 125^\circ C$ or $150^\circ C$ to calculate the power.

(2) Output characteristics

As $I_{C}-V_{CE}$ characteristics, collector-emitter voltage is measured by holding $T_{j}=150^\circ C$ or $T_{j}=125^\circ C$ and varying $I_{C}$ by sweeping the gate-emitter voltage ($V_{GE}$). This data is used to determine the $V_{GE}$ voltage necessary to lower the device loss under an $I_{C}$ condition.

(3) $I_{F}-V_{F}$

This data shows the drop voltage between the anode and cathode when a forward current ($I_{F}$) passes through FWD. The FWD on-state power loss ($P_{F}$) can be calculated as with the $I_{C}-V_{CE}$ characteristics.

(4) $E_{on}-I_{C}$

Figure 2.1 shows a simplified circuit when using an IEGT while it is switching. Figure 2.2 shows a simplified waveform for each part.
This is the data of the power loss $E_{on}$ generated at the time the device in Figure 2.1 is turned ON, measured by varying $I_c$. Turn-on power loss ($P_{on}$) can be calculated by obtaining the $E_{on}$ for an $I_c$ and then multiplying this value by the operating frequency.

(5) $E_{off-Ic}$
As with $E_{on-Ic}$, the data is used for calculating $E_{off}$ at the time the device is turned OFF.

(6) $E_{dsw-IF}$
Figure 2.3 shows a simplified waveform for each part when using an FWD while it is switching. $E_{dsw}$ is the energy integrating the product of the current waveform ($I_{rr}$) and the voltage waveform ($V_{r}$) during the period specified as $E_{dsw}$ in Figure 2.3. $E_{dsw}$ data is provided for various $I_F$ in the figure. The FWD switching loss ($P_{dsw}$) can be calculated by obtaining $E_{dsw}$ under the $I_F$ condition and then...
multiplying this value by the operating frequency.

(7) $E_{on}$, $R_{G(on)}$, $E_{off}$, $R_{G(off)}$, $E_{dsw}$, $R_{G(on)}$

In the measurement condition for $E_{on}$, $E_{off}$, and $E_{dsw}$ described above, $R_{G(on)}$ and $R_{G(off)}$ in Figure 2.1 are varied to measure the values. In IEGT, varying the drive circuit $R_G$ changes switching time, switching loss, and surge voltage generated at switching time. However, the switching time and the switching loss are in conflict with the surge voltage. Therefore, consider this point to determine the optimum $R_G$ value.

(8) $V_{GE-Qg}$

Figure 2.4 shows the amount of input charge required to design an IEGT gate drive circuit. The characteristics show the change of gate-emitter voltage ($V_{GE}$) relative to the gate input charge value ($Q_g$). This indicates the charge amount of gate capacitance needed to turn on the IEGT. To calculate the current supply capability required for the drive circuit, obtain from this figure the charge amount $Q_g$ until $V_{GE}$ obtained in (2), and then multiply it by the switching frequency.

![Figure 2.4 V_{GE-Qg} Characteristics](image)

(9) $t_{d(on)}$, $t_r$, $t_{d(off)}$, and $t_{r-lc}$, $t_r$, $t_{r-lf}$

This data shows the current dependence of the items defined in Figures 2.2 and 2.3. IEGTs connected in series are turned ON and OFF. If they are turned ON at the same time, an excessive through-current flows from the main power supply to the device. This may result in heat generation due to an increase in dissipation or the possibility of a breakdown in the worst case. Therefore, it is necessary to set a pause period in which neither device is turned ON. This data is used for designing the input signal timing for each device.

(10) $R_{th(j-c)} - t$

This data is used for thermal design. In general, chip temperature rise, when power ($P_c$) is applied during application time ($t$), is indicated by $R_{th(j-c)}(t) \times P_c$. However, since the waveform of the actual power applied is complicated, a detailed explanation will be discussed later. There are occasions when press pack type PPI is measured using $j-f$ (junction-fin) instead of $j-c$. 
(11) RBSOA

A surge voltage is generated in the device due to stray inductance of the circuit at the moment the IEGT changes from an ON to an OFF state. Here, the cutoff current in OFF state and the surge voltage generated at that time are expressed as Lucas. This data shows the area where the device does not break. It is necessary to design so that Lucas of the turn-off waveform can fall within the acceptable area (by lowering circuit stray inductance, adding a surge absorption circuit, or relaxing turn-off speed).

(12) RRBSOA

This data shows the Lucas safe operating area for the reverse recovery current at FWD reverse recovery operation (see Figure 2.3) and the device’s collector-emitter voltage generated at that time. It is necessary to design so that the FWD’s waveform in use during the reverse recovery operation can fall within this area (by reducing circuit stray inductance, relaxing di/dt by relaxation of turn-on time, and so on).
2.2. Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Definitions and content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-emitter voltage</td>
<td>$V_{CES}$</td>
<td>This is the maximum voltage that can be applied between the collector and the emitter in a zero bias state between the gate and emitter (when the gate and emitter are short-circuited). It is necessary to decide the allowable value of the surge voltage so that the breakdown voltage due to the surge generated during actual use is lower than the $V_{CES}$ value by referring to the RBSOA and RRSOA data of each device.</td>
</tr>
<tr>
<td>Gate-emitter voltage</td>
<td>$V_{GES}$</td>
<td>This is the maximum voltage that can be applied between the gate and the emitter in a zero bias state between the collector and emitter (when the collector and emitter are short-circuited). However, even if a voltage less than $V_{GES}$ is applied, applying voltage for long periods may affect the lifetime of the IEGT gate oxide. Take this point into consideration.</td>
</tr>
<tr>
<td>Collector current</td>
<td>$I_C$</td>
<td>This is the maximum DC current allowed for the collector current. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature $T_j$.</td>
</tr>
<tr>
<td>Collector current pulse</td>
<td>$I_{CP}$</td>
<td>This is the maximum pulse current allowed for the collector current. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature $T_j$.</td>
</tr>
<tr>
<td>Freewheeling diode DC current</td>
<td>$I_F$</td>
<td>This is the maximum allowable DC current for the built-in freewheeling diode. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature $T_j$.</td>
</tr>
<tr>
<td>Freewheeling diode pulse</td>
<td>$I_{FP}$</td>
<td>This is the maximum pulse current allowed for the built-in freewheeling diode. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature $T_j$.</td>
</tr>
<tr>
<td><strong>Item</strong></td>
<td><strong>Symbol</strong></td>
<td><strong>Definitions and content</strong></td>
</tr>
<tr>
<td>--------------------------</td>
<td>------------</td>
<td>-------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Collector power dissipation</td>
<td>P&lt;sub&gt;c&lt;/sub&gt;</td>
<td>This is the maximum power dissipation allowed for a single device. However, the guaranteed value is the ideal theoretical value when the case temperature of the device is fixed at 25°C. Derating is needed under limited heat dissipation conditions for practical use. (For more details, refer to the explanation on thermal design.)</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>T&lt;sub&gt;j&lt;/sub&gt;</td>
<td>This is the maximum value of chip junction temperature during normal operation. Since junction temperature affects reliability, it should be taken into consideration in design. For more details, refer to the Reliability Handbook.</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>T&lt;sub&gt;stg&lt;/sub&gt;</td>
<td>This is the guaranteed temperature range when storing or shipping a device without subjecting it to electrical load.</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>V&lt;sub&gt;isol&lt;/sub&gt;</td>
<td>This is the maximum effective value of sinusoidal voltage that can be applied between the mounting surface for cooling where it is isolated from electrodes and the electrodes are being shorted together.</td>
</tr>
<tr>
<td>Tightening torque Attachment</td>
<td></td>
<td>This is the maximum torque value that can be applied to the screw when attaching the device to the cooling chassis using a specified screw.</td>
</tr>
<tr>
<td>Tightening torque Terminals</td>
<td></td>
<td>This is the maximum torque value when connecting the external wiring to the electrode terminal of the device using a specified screw.</td>
</tr>
</tbody>
</table>

Note: Do not exceed the maximum ratings value in any case. In addition, using the product under marginal conditions may affect reliability (device life) although each value is below the maximum rating. Therefore, read our company’s Reliability Handbook and derate the device accordingly.
# 2.3. Electrical Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Definitions and content</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(Refer to the technical datasheet of each product for measurement conditions and specification values.)</td>
</tr>
<tr>
<td>Static characteristics</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector cut-off current</td>
<td>$IC_{ES}$</td>
<td>This is the collector current value that flows when the gate and emitter electrodes are short-circuited and the specified voltage is applied between the collector and the emitter. Since it increases with temperature, it should be considered as loss if necessary.</td>
</tr>
<tr>
<td>Gate leakage current</td>
<td>$IG_{ES}$</td>
<td>This is the gate current that flows when the collector and the emitter electrodes are short-circuited and a specified voltage is applied between the gate and the emitter. Since this is a leakage current through the gate oxide, the increase due to temperature increase is small.</td>
</tr>
<tr>
<td>Gate-emitter cut-off voltage</td>
<td>$V_{GE(OFF)}$</td>
<td>This is the gate-emitter applied voltage value for a specified collector current to flow when applying a specified collector-emitter voltage. When surge voltage exceeding this value occurs between the gate and emitter, the device may be erroneously turned ON. Therefore, the surge voltage should be checked in design.</td>
</tr>
<tr>
<td>Collector-emitter saturation voltage</td>
<td>$V_{CE(sat)}$</td>
<td>This is the voltage value between the collector and the emitter when a specified voltage is applied between the gate and the emitter while a specified current flows through the collector. Since it is an important characteristic affecting the static loss of the device, the voltage should be applied below $VG_{ES}$ to keep this value sufficiently low and stable.</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>$C_{ies}$</td>
<td>This is the capacitance between the gate and emitter when specified voltages are applied between the collector and the emitter and between the gate and the emitter with the collector-emitter short-circuited in an AC manner.</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>$C_{oes}$</td>
<td>This is the capacitance value between the collector and the emitter when a specified voltage is applied between the gate and the emitter while the emitter is grounded.</td>
</tr>
<tr>
<td>Feedback capacitance</td>
<td>$C_{res}$</td>
<td>This is the capacitance value between the collector and the gate when a specified voltage is applied between the gate and the emitter while the emitter is grounded.</td>
</tr>
<tr>
<td>Diode forward voltage</td>
<td>$V_{F}$</td>
<td>This is the voltage value between the anode and the cathode when a specified forward biased current is applied to the freewheeling diode connected in reverse-parallel between the IEGT collector and the emitter. It is an important characteristic affecting the steady loss of a device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Item</strong></td>
<td><strong>Symbol</strong></td>
<td><strong>Definitions and content</strong></td>
</tr>
<tr>
<td>------------------</td>
<td>------------</td>
<td>---------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>$t_{d(on)}$</td>
<td>When the IEGT is turned on, this is the time interval from the time when the gate voltage is at 10% of its setting to the time when the collector current reaches 10% of its setting.</td>
</tr>
<tr>
<td>Rise time</td>
<td>$t_{r}$</td>
<td>When the IEGT is turned on, this is the time interval during which the collector current changes from 10% to 90% of its setting.</td>
</tr>
<tr>
<td>Turn-on time</td>
<td>$t_{on}$</td>
<td>When the IEGT is turned on, this is the time interval from the time when the gate voltage is at 10% of its setting to the time when the collector current reaches 90% of its setting.</td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>$t_{d(off)}$</td>
<td>When the IEGT is turned off, this is the time interval from the time when the gate voltage is at 90% of the maximum setting to the time when the collector current reaches 90% of the setting.</td>
</tr>
<tr>
<td>Fall time</td>
<td>$t_{f}$</td>
<td>When the IEGT is turned off, this is the time interval during which the collector current changes from 90% to 10% of its setting.</td>
</tr>
<tr>
<td>Turn-off time</td>
<td>$t_{off}$</td>
<td>When the IEGT is turned off, this is the time interval from the time when the gate voltage is 90% of its maximum setting to the time when the collector current reaches 10% of its maximum setting on the tangent of the falling current.</td>
</tr>
<tr>
<td>Reverse recovery current</td>
<td>$I_{rr}$</td>
<td>This is the minimum value of the reverse recovery current of the FWD connected in reverse-parallel between the IEGT collector and the emitter.</td>
</tr>
<tr>
<td>Reverse recovery time</td>
<td>$t_{rr}$</td>
<td>This is the time interval during which the reverse recovery current of the FWD, connected in reverse-parallel between the IEGT collector and emitter, reaches the minimum current value $I_{rr}$ from 0 A, and then the tangent of 90% to 50% of $I_{rr}$, again returning toward 0 A, becomes 0 A.</td>
</tr>
<tr>
<td>Reverse recovery charge</td>
<td>$Q_{rr}$</td>
<td>This is the FWD charge amount (the time-integral value of the reverse recovery current) for the period when the reverse recovery current of the freewheeling diode, which is connected in reverse-parallel between the collector and the emitter of the IEGT, reaches the minimum current value $I_{rr}$ from 0 A, and then the reverse recovery current, again returning toward 0 A, becomes 2%.</td>
</tr>
<tr>
<td>Turn-on switching loss</td>
<td>$E_{on}$</td>
<td>When the IEGT is turned on, this is the integral value of the product of the collector current and the collector voltage for the period from the time when the gate voltage is at 10% of its setting to the time when the collector voltage reaches 2% of its setting value.</td>
</tr>
<tr>
<td>Turn-off switching loss</td>
<td>$E_{off}$</td>
<td>When the IEGT is turned off, this is the integral value of the product of the collector current and the collector voltage for the period from the time when the gate voltage is at 90% of the maximum setting to the time when the collector current reaches 2% of its setting.</td>
</tr>
<tr>
<td>Reverse recovery loss</td>
<td>$E_{rr}$ (E_{rr})</td>
<td>This is the integral value of the product of the reverse recovery current and the voltage applied to FWD for the period when the reverse recovery current of the freewheeling diode, which is connected in reverse-parallel between the collector and the emitter of the IEGT, reaches the minimum current value ($I_{rr}$) from 0 A, and then the reverse recovery current, again returning toward 0 A, becomes 2%.</td>
</tr>
<tr>
<td>Gate charge</td>
<td>$Q_g$</td>
<td>This is the amount of electronic charge that needs to be supplied to the gate in order to turn the IEGT on. (When turning the IEGT off, the same amount of discharge is required.)</td>
</tr>
<tr>
<td>Thermal resistance (junction-to-case)</td>
<td>$R_{(j-c)}$</td>
<td>This is the saturated thermal resistance between the junction and case (the back side of the product) in one device of the IEGT or FWD equivalent circuit.</td>
</tr>
<tr>
<td>Thermistor resistance</td>
<td>$R_{therm}$</td>
<td>This is the resistance value of the thermistor at a specified temperature.</td>
</tr>
<tr>
<td>B constant</td>
<td>$B$</td>
<td>This temperature characteristic of the thermistor resistance value is a constant representing the change in resistance under two arbitrary temperature conditions.</td>
</tr>
</tbody>
</table>
3. Handling Precautions (When Using Semiconductor Products)

Though we work continually to improve the quality and reliability of our products, semiconductor products can malfunction or fail. When using our semiconductor products (hereinafter referred to as "Product"), customers are responsible for providing adequate safety designs of the software and systems to avoid loss of human life, bodily injury, or damage to property due to product malfunction or breakdown. Before designing and using the Product, refer to and comply with the latest Product information (including this document, specifications, datasheets, and application notes) and related documents such as instruction and operation manuals of the equipment with which the Product will be used. When using any information contained in the above documents, including product data, technical contents shown in diagrams or tables, program code, algorithms, and sample application circuits, for customers' products, customers must thoroughly evaluate their own products independently as well as their whole systems and determine the applicability of the information in relation to the customers' responsibilities.

3.1. IEGT Device Selection

(1) Voltage Ratings
For the voltage ratings of an IEGT device, the input power supply of the equipment to be used, its stability, and circuit constants should all be considered. Select the device according to its purpose. For steady-state devices in general,
- Peak voltage: 80% or less of the device ratings (VCES)
- DC voltage: 50% to 60% of the device rating (VCES)

It is recommended that voltage be set at 90% or less of the device rating (VCES) even in an unsteady-state. The relationship between the device voltage ratings and the power supply voltage (input AC line voltage) during inverter application is summarized by the following equation:

Device rated voltage (VCES) = [Input voltage] + [Surge Voltage] + [Voltage variation] + [Margin]
- Input voltage: Multiply by √2 if alternating current
- Surge Voltage: Maximum value of spikes due to factors such as circuit inductance.
- Voltage variation: Voltage rise due to events such as power regeneration.
- Margin: Safety coefficient

(2) Current Rating
As the collector current of the IEGT device increases, VCE(sat) rises and the generated steady loss increases. At the same time, the switching loss increases, and the heat generation of the device increases.

When using the IEGT device, the junction temperature (Tj) of IEGT and FWD should be less than the maximum junction temperature Tj(max). Improper selection may cause device damage or deterioration of the device’s long-term reliability.

The overload value is often set for inverter applications. Therefore, the following settings are considered safe:
- Steady-state: 50% to 60% or less of the device rated current
- Unsteady-state (maximum time): Within the device rated current (the junction temperature should also be less than the maximum junction temperature)

Note that the 1 ms rated current (Icp) in the device specification is the peak value, which includes the recovery current at the time of the reverse recovery of the freewheeling diode, and the value when an accident causes various protection operation. (It cannot be used repeatedly, exceeding the maximum junction temperature as described above.)

Current selection during general inverter application is defined by the following equation:

Peak current (Ip) = [Inverter capacity] x [Overload rate] / [AC voltage] / √3 x √2 x [Current ripple rate]
Device rated current (Ic) = Ip/derating rate
- Inverter capacity: Output load (W) ÷ Efficiency
AC voltage: Effective value

However, selection of the rated current depends on operating and heat dissipation conditions of the equipment. Therefore, select the current rating after confirming the occurrence loss and temperature rise of the equipment.

3.2. Electrostatic Discharge and Gate Protection

The $V_{GE}$ guaranteed value of the IEGT device is generally $\pm 20$ V maximum (refer to the guaranteed value in the technical datasheet). The IEGT gate may malfunction if a voltage exceeding the $V_{GES}$ guaranteed value is applied between G-E of IEGT. Make sure that the voltage does not exceed the guaranteed value between G-E.

Also, since the IEGT gate requires handling even against static electricity and other charges, use the product with caution by complying with the following handling precautions:

1. When handling modules, discharge static electricity from the human body and clothing by using anti-static straps, etc. and work on grounded conductive mats.
2. Handle an IEGT device with its package body. Do not touch the terminal (especially the control terminal) part directly.
3. When connecting and fixing wiring parts and materials (bus bars, wires, etc.) to the IEGT terminal, make sure that the material used is not charged to avoid static electricity being applied to the IEGT as in item (1).
4. The IEGT device is shipped with electrostatic countermeasures between G-E with conductive materials like copper wire, copper tape, IC foam, etc. Remove this conductive material immediately before electrically wiring the product.

In addition, the IEGT may be damaged if voltage is applied between the collector and the emitter while the gate-emitter is in the OPEN state. This is caused by the events that the collector potential changes, the gate potential rises after current (i) flows as shown in Figure 3.1, then the IEGT turns on, and the collector current flows.

Consequently, when a product is incorporated into the equipment, the IEGT may be damaged if voltage is applied to the main circuit with a failed gate circuit or if a gate circuit is not operating normally (gate is in the open state). To prevent this damage, it is recommended to add a protection circuit. For example, when the gate circuit power supply is not turned on, the protection circuit short-circuits between the gate and the emitter. Or it prevents the main circuit from being charged without making sure that the gate circuit power supply is ON (the gate and the emitter are negatively biased).

![Figure 3.1 IEGT Behavior in an Open State between G-E](image-url)
3.3. Protection Circuit Design

IEGT devices may be damaged by abnormal phenomena like overcurrent and overvoltage. To protect the devices from damage, a protection circuit such as a snubber circuit may be added. The design of the protection circuit should match the device characteristics. The characteristics and circuit operation of the device should be carefully considered. If the match is inadequate, the effect of the added protection circuit will be ineffective and the desired result may not be obtained. An example is when applying overcurrent protection: the interruption time may take too long to deviate from the SOA and may cause a breakdown. Another example is that when the capacitor capacitance of the snubber circuit is too small, an excessive spike voltage is generated. For more details on overcurrent and overvoltage protection methods, refer to “Protection Circuit Design” in Chapter 4.

3.4. Thermal Design

The maximum allowable junction temperature $T_j(\text{max})$ of an IEGT device is predefined. Therefore, thermal design should be below this temperature. When determining thermal design, the application operation to which the IEGT device will be applied should be thoroughly considered. Inadequate thermal design may cause problems such as breakdowns when the device's temperature exceeds its allowable limit during hardware operation.

To determine the thermal design, calculate the device power loss and then select thermal fins that keep the device below the allowable temperature based on that loss. For more details regarding this topic, refer to “Thermal Design and Mounting on Thermal Fins” in Chapter 5.

3.5. Drive Circuit Design

Designing the drive circuit is important to fully maximize the device’s performance. It is also closely related to the design of protection circuits.

The drive circuit consists of a forward-biased circuit for turning the device on and a reverse-biased circuit for keeping the device off steady-state and for accurately turning it off. The device characteristics change according to each of these condition settings. In addition, depending on the position of the drive circuit and the wiring method, problems such as device malfunctions may occur.

The design of an optimal drive circuit is very important. Therefore, refer to “Gate Driver Circuit Design” in Chapter 6 for more details.

3.6. Parallel Connection

To control large currents such as for large capacity inverters, the devices are sometimes used with parallel connections.

When devices are connected in parallel, it is important to ensure that the uniform current is flowing through the devices. The current balance at the time of parallel connection changes according to the device characteristics and the wiring method. Therefore, management and design, such as the equalized device $V_{CE(sat)}$ or main circuit wiring are necessary. For more details about this topic, refer to “Parallel Connection” in Chapter 7.
3.7. Mounting Precautions

When mounting IEGT devices, pay particular attention to the following notes:

For module type devices

1. When mounting the module on the heat sink, apply the thermal compound to the back of the module and sufficiently tighten it with the specified tightening torque. Moreover, set the surface flatness to 50 μm or less for 100 mm and the surface roughness to 10 μm or less between the screw mounting positions of the heat sink. When the heat sink has a poorly flat (especially convex) surface or when its compound thickness is uneven, not only does the cooling become unbalanced, but in the worst case, it may cause insulation breakdown that can lead to a serious accident.

2. When wiring, do not apply excessive stress to the module electrode terminal. The worst-case scenario is a malfunction such as wire breakage of soldered electric wiring inside the module. For more details about this topic, refer to Chapter 5.

For press pack type devices

1. The press-contact state (evenly flat contact pressure) is important since the press pack type device applies pressure to all contacts between the main electrodes. A specified contact pressure is also used after applying a conductive thermal compound between the device electrode surface and the heat sink.

2. There is a possibility that the device itself expands and the contact pressure rises due to temperature change from the load applied to the device. Even in such conditions, apply contact pressure evenly by using it together with a Belleville washer or similar hardware. For more details about this topic, refer to Chapter 5.

3.8. Storage and Transportation Precautions

Storage

1. Keep the storage temperature of the semiconductor devices at 5°C to 35°C and the humidity at 45% to 75%.

2. Avoid locations that generate corrosive gases, and dusty locations. The packaging box used for delivering the devices is made of corrugated cardboard and is thus not suitable for long-term storage. (There is a slight possibility that sulfidizing gas may be generated.) Consider other packaging for long-term storage.

3. Rapid temperature changes can cause condensation on the semiconductor device. Avoid such environments and store the devices in locations with minimal temperature fluctuations.

4. Do not allow external force or load to be applied to semiconductor devices while they are in storage. Unexpected load may be applied especially when devices are stacked on top of or under other items.

5. Use containers that are less susceptible to static electricity when temporarily storing semiconductor devices.

Transportation

1. Some devices are heavy due to their ratings and structure. Be cautious of falling devices that may cause physical injury.

2. Do not drop or apply physical shocks to products during transportation.

3. When transporting large quantities of semiconductor devices in a container, insert soft spacers between the devices to avoid damaging the contact electrode surfaces and other components.
3.9. Reliability Precautions (Lifetime Design)

In general, when operating an inverter or other electric power converter, the incorporated IEGT device's temperature repeatedly rises and falls. Due to the temperature changes, the IEGT device undergoes thermal stress. Consequently, its lifetime depends on its operating conditions. Therefore, consider making the design lifetime longer than the required lifetime of the equipment.

To achieve an optimal lifetime design in general, check the temperature change of the IEGT device and then make a lifetime design from the thermal fatigue endurance. If the lifetime design is not sufficiently considered, problems may arise such as shortened lifetime and reduced reliability. Therefore, lifetime design based on reliability is important. For more details regarding this topic, refer to “Reliability Information” in Chapter 8.

3.10. Other Notes on Handling Precautions

(1) Make sure that the driving voltage (VGE) is measured at the module terminal and the specified voltage is applied. (When measured at the end of the drive circuit, this voltage is not affected by the voltage drop of the transistor, etc. Therefore, even if the prescribed VGE is not applied to IEGT, a problem may be undetected which may lead to device damage.)

(2) Measure the product’s main terminal part for surge voltage and other issues at turn-on/turn-off. If measurement terminals are described separately in the specification sheet, measure with those terminals.

(3) Use the product within the range of its maximum ratings (voltage, current, temperature, etc.). The product may be damaged if used beyond its maximum ratings. In particular, when a voltage exceeding VCES is applied, avalanche breakdown may occur and the device may be damaged. Make sure that the VCE is used within the range of the maximum ratings.

(4) In the unlikely event that the device is damaged due to an accident, prevent a secondary breakdown by providing a fuse or a fault detection circuit with appropriate capacity between the main circuit capacitor and the semiconductor device.

(5) Thoroughly understand the product’s use environment. Consider whether it satisfies the product’s lifetime reliability expectation before using it. If the product is used beyond its reliability lifetime, the device may be damaged before the equipment using the device can reach its target lifetime.

(6) Use this product within its thermal fatigue lifetime. Thermal fatigue lifetime has two major types: power cycle tolerance and TFT tolerance, respectively caused by ΔTj and ΔTc. The both should be considered for module type devices, and the latter for press pack type devices. When using this product, both thermal fatigue lifetime types are dependent on the thermal design. Consider not only the rise and fall of the junction temperature, but also the rise and fall of the case temperature.

(7) Avoid locations that generate acid, organic substance, or corrosive gas (such as carbon sulfide or sulfidizing gas). When used in locations that generate acid, organic substance, or corrosive gases, product qualities such as functions and appearance are not guaranteed.

(8) Do not apply excessive stress to the main and control terminals while mounting the product on the equipment. A deformed terminal may cause poor contact and terminal structure breakage.

(9) Select the appropriate screw length for the terminal used for the module product in accordance with the outline drawing. Long screws may damage the case.

(10) When only the FWD is used and the IEGT is not used (e.g., when applying to a chopper circuit), apply a reverse bias of -5 V or more (recommended -15 V, maximum -20 V) between G-E of the unused IEGT. If the reverse bias is insufficient, the IEGT may erroneously turn on due to dv/dt at FWD reverse recovery, and this may eventually lead to damage.

(11) If turn-on dv/dt is high, the IEGT of the opposite arm may erroneously turn on. Follow optimum drive conditions (+VGE, -VGE, RG, CGE) to prevent erroneous turn-on.

(12) Soldering the product at extreme temperatures may cause the package to deteriorate. Pay attention to the soldering process.
(13) The cooling fin should have a surface flatness of 50 μm or less at 100 mm between the screw mounting positions and the surface roughness should be 10 μm or less. An excessively convex surface may cause a product breakdown that can lead to a serious accident. Moreover, excessive concave curvature, distortion, and other irregularities can create a gap between the product and the cooling fin and may result in poor heat dissipation that can lead to thermal breakdown.

(14) Excessive static electricity applied to the control terminal may damage the device. Take necessary precautions against static electricity.

(15) When attaching the device to the cooling fin, use a compound that ensures heat conduction. Also, if the coating amount is insufficient or the coating method is inappropriate, heat conductivity will decrease and thus reliability will deteriorate. When applying the compound, confirm that it spreads to the whole radiating surface of the product. (Check the spreading condition of the compound when removing the device after mounting.)

(16) The external resistor $R_G$ stated in the specification document indicates the recommended resistance to minimize switching loss. However, the optimum $R_G$ varies depending on circuit configuration and the operating environment. Therefore, when determining the external resistor $R_G$, carefully consider characteristics such as switching loss, EMC/EMI, spike voltage, surge current, and unexpected vibration in the circuit configuration and operating environment where the IEGT device is used. Note that a proper external resistor $R_G$ must be selected to comply with the specification.

(17) This section only explains the main practical precautions. For more details, check the notes and warnings stated in the specifications of each product.
4. Protection Circuit Design Methods

4.1. Surge Voltage Protection

The IEGT switching time is as short as a few μs, which works well with high-speed switching. However, such high-speed switching characteristics could cause a surge voltage to the IEGT. This is due to stray inductance Ls in the absence of circuit technology. The $V_{surge}$ size is:

$$V_{surge} = -Ls \times \frac{di}{dt} + Vcc$$

Design the main circuit so that this value is sufficiently smaller than the maximum rated voltage between the main terminals described in the datasheet. $V_{surge}$ can be reduced by lowering the $\frac{di}{dt}$, stray inductance, etc. However, reducing the $\frac{di}{dt}$ sacrifices the high-speed switching characteristics of the IEGT. Therefore, stray inductance should be reduced. For example, using a copper plate instead of a wire can greatly reduce inductance. An effective way to reduce generated surge voltage is to add a snubber circuit.

**Snubber circuit example**

Figure 4.1 shows examples of snubber circuits. Although a snubber circuit can absorb the surge voltage, the change in surge voltage would still depend on the IEGT switching characteristics and the main circuit wiring configuration. Therefore, understand the characteristics of the snubber circuit before deploying it. Next, carefully select the circuit configuration and determine the constant by experimentation.

(a) Snubber between PN  
(b) RDC snubber between PN  
(c) Individual clamp snubber

![Figure 4.1 Example of Snubber Circuit](image)

Next, the individual clamp snubber in diagram (c) will be briefly explained. Figure 4.2 shows an example of an individual clamp snubber and the turn-off waveform at that time. $\Delta V1$ is a voltage (surge voltage) that cannot be absorbed due to inductance $L2$ of the snubber circuit. In other words, this is the turn-off voltage generated at $\frac{di}{dt} \times L2$ at turn-off.

Set $Cs$ from the following equation:

$$\frac{1}{2} \times L1 \times (Ic)^2 = \frac{1}{2} \times Cs \times (\Delta V2)^2$$

Here, $L1$ is the main wiring inductance, $L2$ is the snubber circuit inductance, $Rs$ is the snubber resistance, and $Ds$ is the snubber diode.
When connecting modules in parallel, it is recommended to attach a snubber circuit to each module. In large capacity increases with parallel connection, connection by splitting the snubber circuit for each device is considered more efficient in reducing snubber wiring inductance $L_2$ than a single one. Therefore, it is effective for surge voltage suppression. A capacitor is needed between the P and N if excessive surge voltage is generated between them. Especially for large capacity devices, capacitors and individual snubber circuits (c) may be used in combination with a capacitor between the P and N (a) in Figure 4.1.

### 4.2. Short Circuit Protection

About short circuit capacity

When an IEGT is in a short-circuit state, its collector current increases. When the current exceeds the predetermined value, the collector-emitter voltage rapidly increases. Because of such characteristics, the collector current at short circuit is suppressed to a certain value or less.

However, this high voltage or large current state in the IEGT should be eliminated as quickly as possible. Note that the IEGT has a time limit when shutting off the current after a short circuit condition occurs. This is called short-circuit capacity and it is specified from the start time of the short-circuit current flow to the breakdown, as shown in Figure 4.3. Therefore, when a short circuit occurs, shut off it within the specified short circuit capacity. Short-circuit capacity depends on various conditions such as collector-emitter voltage $V_{CE}$, gate-emitter voltage $V_{GE}$, and junction temperature $T_j$.

In general, the short circuit capacity amount is smaller when power supply voltage $V_{cc}$ or junction temperature is higher. For more details on the short-circuit capacity of each device, refer to the technical datasheet.

Overcurrent detection for protection against short-circuit is performed by a CT (Current Transformer), a CE voltage, or the like. Turn the device off immediately when an overcurrent is detected. Short-circuit protection is possible only with current detection. However, depending on use conditions, there is a possibility that (1) surge current at short circuit turn-on will be large, and (2) surge voltage at short circuit turn-off may be high. It is therefore advisable to take the necessary precautions.
(1) Example of how to suppress surge current at short circuit turn-on (Figure 4.4)
When the gate-emitter voltage rises, the surge current at short circuit turn-on increases. This may cause a breakdown. To suppress the surge current, the gate voltage should be suppressed. In general, this is done by inserting a Zener diode (16 to 17 V) between the gate and the emitter. Inserting a Zener diode suppresses the gate-emitter voltage rise and the surge current. However, when the Zener diode voltage is too low, the gate voltage at the time of normal turn-on/turn-off becomes insufficient, which may increase turn-on and turn-off loss. Similarly, when Zener diode voltage is too high, the effectiveness of gate voltage suppression decreases. Therefore, select the appropriate voltage for the Zener diode while checking the waveform.

Red: example with Zener diode
Black: example without Zener diode

![Figure 4.4 Example of a Circuit Diagram with its Waveform when a Zener Diode is Inserted](image)

(a) Example diagram of a circuit in which a Zener diode is inserted
(b) Example of a short-circuit waveform when a Zener diode is inserted and when it is not inserted

(2) Surge voltage at short-circuit turn-off
When the main circuit wiring is long, surge voltage at the time of short-circuit turn-off becomes high. This may lead to damage. As a common method of suppressing surge voltage, detect $V_{CE(sat)}$ abnormalities using an overcurrent detector or driver circuit and apply the soft turn-off method, which is done by increasing the gate resistance or suppressing the gate output voltage. (Figure 4.5; A separate circuit is required.) However, avoid erroneous detection by turn-on operations in every operation mode. Select the appropriate short-circuit protection circuit while checking the waveform.

Black: without soft turn-off
Red: with soft turn-off by increased gate resistance using overcurrent detection

![Figure 4.5 Example of a Short-Circuit Waveform with Soft Turn-Off by Gate Resistance](image)
5. Thermal Design and Mounting on Thermal Fins

5.1. Principles of Heat Dissipation

5.1.1. Radiation Equivalent Circuit

If the transfer of heat is replaced by an electric current, the path through which the heat is conducted to the outside can be shown by an electric circuit. Heat conduction from the junction part of the IEGT to the outside air is determined by the thermal resistance and heat capacity of this equivalent circuit. Figure 5.1 shows a heat radiation equivalent circuit in a thermally steady state.

![Figure 5.1 Heat Radiation Equivalent Circuit](image)

Equation (2) from the equivalent circuit in Figure 5.1 gives the whole thermal resistance $R_{th(j-a)}$ from the junction part to the outside air.

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-f)} + R_{th(f-a)}$$ ............................................................... (2)

Let $P_D$ be the power loss at the device, and the junction temperature $T_j$ is given by equation (3).

$$T_j = \Delta T_j + T_a = P_D \times R_{th(j-a)} + T_a$$ ........................................................................... (3)

Design the heat dissipation of the fins so that $T_j$ expressed by equation (3) never exceeds the absolute maximum rating, $T_{j_{max}}$, of the data sheet.

5.1.2. Loss Calculation

The power loss in the device can be expressed by equation (4).

$$P_D = PST(IEGT) + POFF + PON + PST(FWD) + PDSW$$ ........................................................................... (4)

- **PST(IEGT)** : Conduction loss of the IEGT part
- **POFF** : IEGT turn-off power loss
- **PON** : IEGT turn-on power loss
- **PST(FWD)** : Conduction loss of the diode part
- **PDSW** : Diode reverse recovery loss

$PST(IEGT)$ can be calculated from the $I_c-V_{CE}$ curve, and $PST(FWD)$ can be calculated from the $I_F-V_F$ curve. For POFF, PON, and PDSW, measure the $E_{on-I_c}$, $E_{off-I_c}$, and $E_{ds-w-I_F}$ curves, respectively, using circuits and drive conditions that match the application, and use the results for your calculations. The data sheet contains switching loss curves for typical drive conditions. In your thermal design, provide leeway for power loss so that $T_j$ never exceeds $T_{j_{max}}$. 
5.1.3. Junction Temperature Pulse Response

In general, the thermal impedance of a power semiconductor is given by a distributed constant circuit as shown in Figure 5.2.

![Figure 5.2 Thermal Impedance in Power Semiconductor](image)

For ordinary power semiconductors, the actual value can be approximated by considering that m equals 4, but it is difficult to calculate the value of Tj when the values of C and R are not clear. Therefore, in general, estimate Tjmax using the transient thermal resistance curve.

First, consider a single pulse. When a single square wave pulse (width T1, peak value P0) is applied, the transient thermal resistance Rth(T1) with respect to the pulse width T1 is obtained, and Tjmax is given by equation (5).

\[ Tj_{\text{max}} = R_{\text{th}}(T1) \times P0 + T_a \] ......................................................(5)

In the inverter operation, power loss occurs in pulses every time switching is repeated, so the junction temperature changes as shown in Figure 5.3. In this case, the peak value (Tjmax) of the temperature can be estimated by approximating the power loss with a square-wave pulse of a fixed period and using the transient thermal resistance curve.

When a continuous pulse of period T as shown in Figure 5.3 is applied, Tjmax is given by equation (5) in a thermally stable state. In thermal design of power semiconductors, care must be taken that Tjmax in equation (5) does not exceed the maximum ratings of the power semiconductors.

![Figure 5.3 Temperature Change When Pulse Loss is Applied](image)
5.2. Press Pack Type IEGT

Pay attention to the following points when attaching the press pack type IEGT to the thermal fin so the device can provide a sufficient heat radiation effect without applying thermal or mechanical stress to the device.

- Application of Conductive Grease
  Apply conductive grease between the device and the fins to improve the thermal resistance between them. In this case, apply a thin and uniform layer of conductive grease. Non-volatile conductive grease is suitable. (When volatile conductive grease is used, cracks may form in the grease in the long term and the heat radiation effect may decrease.)

- Mounting on the Fins
  To obtain a sufficient heat radiation effect, mount the device’s electrodes directly on the fins. In this case, the fins are also used as electrodes to establish an electrical connection.

- Selecting a Cooling System
  Select a suitable cooling fin for the amount of heat the device generates. Air cooling type fins include inexpensive aluminum fins, copper laminated fins, and the like. Cover the clamp jig with an insulator tube so that it does not touch the fins. Apply contact pressure through the insulator so that the jig does not electrically connect to the frame or the ground. Use a Belleville washer as the spring. Since the Belleville washer is saturated at the specified pressure, constant pressure can be maintained even if temperature and pressure change.

A water cooling system with a significant cooling effect is suitable when handling a larger amount of power. Place the heat sink cooled by the liquid on both the sides of the press pack type device and press the device with press equipment or a bolt until the specified contact pressure force is obtained. As shown in Figure 5.4, in addition to a water-cooling heat sink that becomes an electrode, a clamp jig, a spring (which will be a source of mechanical pressure), and a ball (to uniformly transmit pressure to the device) are required. When using a water cooling system, use high-quality water (pure water) with high electrical resistance to prevent corrosion inside the electrodes and maintain the insulation between the heat sinks. Also, contact the manufacturer of each heat sink to obtain its thermal resistance.

![Image](image_url)

Figure 5.4 Example of Mounting a Press Pack Type Device on a Water-Cooling Fin

Provided by Toshiba Mitsubishi-Electric Industrial Systems Corporation
5.2.1. Heat Sink Design

The most important point for press pack type IEGTs is to apply pressure uniformly. Note the following when designing the heat sink.

- The heat sink should meet the specifications shown in Figure 5.5.
- Even when the operating environment (temperature, atmospheric pressure, etc.) changes, the total pressure should be within the specified value range.
- The partial pressure density difference of the device should be 20% or less of the average pressure density (total pressure/press-contact area).

(Figure 5.6)

<table>
<thead>
<tr>
<th>Item</th>
<th>Values on Fin's Press-Contact Surface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Surface flatness</td>
<td>10 μm or less</td>
</tr>
<tr>
<td>Flatness</td>
<td>3 μm or less</td>
</tr>
<tr>
<td>Parallelism</td>
<td>100 μm or less</td>
</tr>
<tr>
<td>Hardness (Vickers Hardness)</td>
<td>100 to 120</td>
</tr>
</tbody>
</table>

(Figure 5.5 Recommended Specifications for Cu Heat Sink for Press Pack Type Devices)

(Figure 5.6 Pressure Distribution Example by a Pressure Measurement System)
5.2.2. Confirmation of Press Pack Conditions

Make sure that the individual devices being stacked are pressed uniformly. One way to check the pressure distribution on the main electrode surface of the device is to apply a load after stacking with a pressure sensor sheet or the like inserted between the press-pack device and the heat sink. Select a pressure sensor sheet with appropriate specifications according to the pressure applied to the main electrode surface of the press pack type device (Figure 5.7).

![Figure 5.7 Using the Pressure Sensor Sheet](image)

Figures 5.8 and 5.9 are examples verified using Fujifilm’s prescale (LW). Figure 5.8 shows an example of uniform press-contact, and Figure 5.9 shows an example of uneven press-contact with pressure loss at the arrow.

![Figure 5.8 Example of a Device Pressed Uniformly](image)  ![Figure 5.9 Example of Uneven Press-Contact with Pressure Loss (Arrow)](image)
5.2.3. Maximum Allowable Power of Press Pack Type IEGT

The TFT tolerance (see note) determines the maximum allowable power of the press pack type IEGT. The TFT tolerance also varies depending on the applied power. The maximum allowable power can be calculated as follows, with 25°C as the maximum value of Tj. However, since the TFT tolerance, which determines lifetime by actual use, depends on the applied power, it is recommended to apply the maximum power as shown in Figure 5.10, especially for PPI.

(Note) Refer to 8.4.2 for an explanation of TFT tolerance and TFT lifetime.

Simple application allowable power calculation (Tc = 25°C):

\[(\text{Maximum } T_j - 25^\circ \text{C}) / \text{Thermal resistance } [^\circ \text{C/W}]\]

Maximum applied power (recommended value from TFT tolerance)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>IEGT Side (W)</th>
<th>Diode Side (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST2100GXH24A</td>
<td>7000</td>
<td>-</td>
</tr>
<tr>
<td>ST1500GXH24</td>
<td>5000</td>
<td>1500</td>
</tr>
<tr>
<td>ST1200GXH24A</td>
<td>5000</td>
<td>-</td>
</tr>
<tr>
<td>ST750GXH24</td>
<td>2000</td>
<td>750</td>
</tr>
</tbody>
</table>

Figure 5.10 Recommended Value of Maximum Applied Power

5.2.4. Maximum Allowable Power of Press Pack Type IEGT and TFT Tolerance

This is an example of ST1500GXH24 with an electrode diameter of 125 mmφ. As shown in Figure 5.11, the lifetime can be lengthened by derating the applied power.

Figure 5.11 Applied Power and TFT Lifetime
5.3. Module Type IEGT

5.3.1. Mounting Module Type IEGT

Set the heat sink flatness of the contact part with the device to 50 μm or less for 100 mm and the surface roughness to 10 μm or less. Apply thermal grease between the device and the fin to improve thermal resistance between the case and the fin. Select a type of grease for heat conductivity that is non-volatile, provides high insulation, and has a long lifetime to ensure the necessary heat conductivity ratio. Apply a thin and uniform coat (about 100 μm) so that air does not get between the base surface of the module and the heat sink.

After applying the grease, tighten the module to the heat sink with the specified torque shown in the data sheet in the order shown in Figure 5.12 or Figure 5.13. Tightening with more than the specified torque may cause damage.

In addition, as the condition of thermal grease varies with long-term use, attention to this is necessary.

![Figure 5.12 Tightening Order of Module Type IEGTs (190 mm x 140 mm type)](image1)

![Figure 5.13 Tightening Order of Module Type IEGTs (130 mm x 140 mm type)](image2)
6. Gate Driver Circuit Design

Design the gate driver for each purpose of the application by using driver IC, photocoupler, hybrid IC, etc. Design points are shown below.

**Gate Voltage**
When designing a gate driver, the recommended value for gate forward bias is +15V and the recommended value for gate reverse bias is -15V. The fluctuation of forward and reverse bias power supply voltage should be ±10% or less.

**Gate Resistance**
To adjust the di/dt at turn-on and to reduce the surge voltage at turn-off, verify real machine operation to optimize the gate resistance value. As gate resistance decreases, switching loss decreases, and increasing the resistance increases the switching loss, so select an appropriate gate resistance value.

**Dead Time**
When configuring an inverter circuit with an IEGT, set dead time to prevent the upper and lower arms from short-circuiting. Dead time is the period during which the gate driver outputs off signals to both the upper and lower arms. Set an appropriate value by verifying the dead time with an actual circuit so as not to cause erroneous turn-on.

**Gate Wiring**
Wiring from the gate driver to the device should be as short as possible to prevent malfunctions caused by effects like electromagnetic noise. Measures such as using a coaxial cable or twisted wires for gate wiring can reduce the influence of external noise. When the gate voltage applied to the IEGT exceeds the gate absolute maximum rating (20 V) described in the datasheet, protect it properly with Zener diodes, etc.

Manufacturers such as Power Integration, InPower, and Amantys sell gate drivers for our IEGTs. Table 6.1 shows examples of combinations of IEGTs and driver circuits.

<table>
<thead>
<tr>
<th>Driver Manufacturer</th>
<th>Power Integration</th>
<th>InPower</th>
<th>Amantys</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST1500GXH24</td>
<td>ISO51251-45</td>
<td>1IPSE1A45-105H</td>
<td>-</td>
</tr>
<tr>
<td>MG1500FXF1US62</td>
<td>1SP0635</td>
<td>1IPSE1A33-60-100</td>
<td>AN33AA1</td>
</tr>
<tr>
<td>MG900GXH1US53</td>
<td>1SD312F2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG1200FXF1US53</td>
<td>1SD536F2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG800FXF1US53</td>
<td>2SC0535T-33</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.1 Correspondence Table for IEGTs and Each Company's Drivers
7. Parallel Connection

Since IEGT is a voltage-driven device, applying an IEGT drive voltage to each parallel-connected IEGT is sufficient. Parallel connection is relatively easy. However, to control high power at high speed, consideration must be given to device selection and characteristics variation.

When IEGT modules are used in parallel, current must not concentrate even during transition and must flow in a uniform and balanced manner to each device under all load conditions.

In the case of a parallel connection, the cause of variation in operation during on-state and the cause of variation during switching are different. The following explains the causes of dispersion for on-state and switching.

During On-State

During on-state, the difference in on-state voltage between modules connected in parallel may cause imbalance. In a steady state, each device shares current so that the on-state voltage between modules is equalized, so a large amount of current flows in devices with low $V_{ce(sat)}$. Also, if the wiring is not uniform, a small current flows in devices with a large wiring resistance component, and a large current flows in devices with a small resistance component. To prevent these problems, design so that the variation of device $V_{ce(sat)}$ is as small as possible and the wiring between devices is as uniform as possible.

During Switching

In general, the imbalance of the current appears most significantly during the transition time of switching on and off. This causes the difference in switching time between devices. This variation in switching time largely depends on the threshold voltage $V_{GE(off)}$ between the gate and emitter. In other words, the smaller the $V_{GE(off)}$ is, the sooner it turns on, and the larger it is, the slower it turns on. Conversely, when turning off, the larger the $V_{GE(off)}$ is, the sooner it turns off, and the smaller it is, the slower it turns off. As a result, current is concentrated on devices with a small $V_{GE(off)}$ for both switching on and off, causing current imbalance. The imbalance of this current may cause excessive loss to the device and an eventual breakdown.

Variations in $V_{ce(sat)}$ may also cause variations in switching time. A device with a low $V_{ce(sat)}$ takes more time for turning off since more current flows during on-state. As a result, concentration of current tends to occur in the device. Therefore, considering the variation of switching time at a transient time, it is preferable that the $V_{ce(sat)}$ and $V_{GE(off)}$ of the IEGTs are as uniform as possible for parallel connection.

Apart from the characteristics of the device, variations of the wiring of the main circuit and gate and the positional relationship can also cause imbalance during switching. When the gate current varies between devices during switching, oscillation occurs not only between the gate and the emitter but also between the emitter and the collector, and this may damage the device. When mounting the gate driver away from the device, twisting the emitter wiring and gate wiring can reduce the influence of rush-in noises.

The parasitic inductance of the main circuit is proportional to the surge voltage in turn-off state. If the parasitic inductance is large, a voltage higher than the breakdown voltage is applied to the device in turn-off state, causing breakdown. On the other hand, if the main circuit inductance of each device is different, current and voltage concentrate on one device, causing breakdown. Therefore, wire so that the main circuit inductance is small and equal among the devices.
8. Reliability Information

8.1. Overview

From the beginning of industrial production, makers have enhanced durability, long lifespan, safety, and serviceability as product quality features that increase the reliability of their products. However, reliability has been more systematically adopted since the 1950s. Along with the increased sophistication and complexity of devices and the progress of systemization for complex systems such as chemical plants and electric power grids, the increased social effect and damage caused by breakdowns have made reliability an important quality characteristic. For this reason, movement from the abstract concept of reliability to developing more quantitative ways, to plan, improve, and manage the reliability of actual systems and products, has become active. JIS quantitatively defines "reliability" as "the probability that an item will perform its intended function for a specified interval under stated conditions." The following focuses on the reliability of power devices. For more information on the concept of reliability, refer to reliability information of semiconductor products on the website of Toshiba Semiconductor & Storage Products.

<http://toshiba.semicon-storage.com/jp/design-support/reliability/device.html>

8.2. Reliability of Power Devices

In general, the failure rate of a power device has a curve shape like a bathtub shown in Figure 8.1. An initial failure period at the beginning of device use is followed by a random failure period and then a wear-out failure period. When choosing a power device, consider the application and the characteristics of the failure rate curve. Details of each failure period are described below.

![Bathtub Curve](image)

Figure 8.1 Time Course of Failure Rate of Semiconductor Products (Bathtub Curve)

Initial failure period

Initial failures are caused by errors such as minute defects in chips like IEGT and FWD, insulating board defects, or wiring defects such as a short defect. We compile past cases of quality issues and carry out continuous quality improvement activities by feeding these cases back to the design of power chips, the module structure, the assembly process, etc. In this way, we are working to reduce the number of products with initial defects. However, it is extremely difficult to completely eliminate initial defects at the design stage, so we are carrying out a shipping test to compensate for this. In the shipping test, we reduce the initial failure rate by conducting screening and aging tests.

Random Failure Period

In the random failure period on the failure rate curve, the failure rate of devices is almost constant because the initial failure products have been removed. In other words, the failure rate varies depending on the operating conditions of a power device application in this period. Specifically, it depends on conditions of use and the environment of the entire system composed of power devices and other parts, so it corresponds to the reliability of each system. To reduce the failure rate in this period, it is necessary to prevent various characteristics (voltage, current, temperature, etc.) from exceeding the absolute maximum ratings of the device under the worst operating conditions of the system. It is recommended to use the device with derating (in general, the voltage is 50 to 60% of the maximum rating, and the junction temperature is 70 to 80% of the maximum rating) with respect to the absolute maximum ratings described
in the specifications, and to comply with conditions of the device application circuits, mounting environmental conditions, and other features specific to the system.

### Wear-Out Failure Period
The wear-out failure period on the failure rate curve is a period that failures occur due to the lifespan of the product. It is necessary to design a system that will result in the projected product lifespan being reached before the product reaches this period. Toshiba verifies the long-term reliability test shown below at the design stage and checks the quality. For the thermal fatigue breakdown model of power devices in particular, as shown in Section 8.4, we verify the lifetime for two breakdown modes: the power cycle and the TFT (Thermal Fatigue Test). Design the product lifetime within the thermal fatigue breakdown tolerance suitable for the operation mode of the applicable system after applying the thermal fatigue breakdown model.

#### 8.3. Typical Reliability Tests
Figure 8.2 shows typical reliability test.

<table>
<thead>
<tr>
<th>Classification</th>
<th>PMI</th>
<th>PPI</th>
<th>Test Item</th>
<th>Content and Test Conditions</th>
<th>Compliant Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Breakdown Test</td>
<td></td>
<td></td>
<td>Temperature Cycle Test</td>
<td>Evaluates the tolerance when the device is left at a high temperature and high humidity for a long time. Normal test conditions: Ta = 60°C, RH = 90%</td>
<td>EIA/JED-4701 105, MIL-STD-883 1010.7, IEC 60749 106, JESD 22 A104-B</td>
</tr>
<tr>
<td>Mechanical Test</td>
<td></td>
<td></td>
<td>Physical Shock Test</td>
<td>Evaluates the tolerance to physical shock received during transport or use. Normal test conditions: Test conditions vary depending on the structure, but the resin mold type has an impact acceleration of 15,000 m/s² in four directions, three times each.</td>
<td>EIA/JED-4701 404, MIL-STD-883 2002.3, IEC 60749 2004.5, JESD 22 A104-C</td>
</tr>
<tr>
<td>Mechanical Test</td>
<td></td>
<td></td>
<td>Vibration Test</td>
<td>Evaluates tolerance to vibration experienced during transportation or use. The test has variable frequency vibration, which is normally performed, and constant frequency vibration. Normal test conditions: Constant frequency vibration: 60 ± 20 Hz, 200 m/s², 96 ± 8 hours in each of three directions. Variable frequency vibration: 100 to 2000 Hz, 200 m/s², three directions, four 4-minutes up-and-down cycles each.</td>
<td>EIA/JED-4701 403, MIL-STD-883 2007.2, IEC 60749 2004.5, JESD 22 A105-C</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>Terminal Strength Tensile Test</td>
<td>Evaluates whether the strength of the terminal part is adequate for the force applied during wiring for its mount or use. Normal test conditions: A specified load is hung on the tip of the lead pin. It is bent and unbent by 90°. Apply a tensile load in a direction parallel to the lead pin. The specified load differs depending on the structure.</td>
<td>EIA/JED-4701 401, MIL-STD-883 2004.5, IEC 60749 2005.8, JESD 22 A103-C</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>High Temperature Preservation Test</td>
<td>Evaluates the tolerance when the device is left at a high temperature for a long time. Normal test conditions: Ta = Tstg. Max</td>
<td>EIA/JED-4701 201, MIL-STD-883 1008.2, IEC 60749 1005.8, JESD 22 A103-B</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>High Temperature Operation Test</td>
<td>Applies electrical stress (voltage, current) and thermal stress to the device for a long time and evaluate its tolerance. Normal test conditions: Ta = 125°C, Power supply voltage: Operation Max</td>
<td>EIA/JED-4701 101, MIL-STD-883 1005.8, IEC 60749 1005.8, JESD 22 A108-B</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>Low Temperature Preservation Test</td>
<td>Evaluates the tolerance when the device is left at a low temperature for a long time. Normal test conditions: Ta = Tstg. Min</td>
<td>EIA/JED-4701 202, MIL-STD-883 1008.2, IEC 60749 1005.8, JESD 22 A108-B</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>High Temperature Bias Test (Gate)</td>
<td>Applies electrical stress and thermal stress to the device for a long time and evaluate its tolerance. Normal test conditions: Ta = 25°C, Power supply voltage: Operation Max</td>
<td>EIA/JED-4701 102, MIL-STD-883 1008.2, IEC 60749 1005.8, JESD 22 A101-B</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>High Temperature Bias Test (Collector)</td>
<td>Stresses the device with electricity for a long time and evaluate its tolerance. Normal test conditions: Ta = 85°C, Power supply voltage: Operation Max</td>
<td>EIA/JED-4701 102, MIL-STD-883 1008.2, IEC 60749 1005.8, JESD 22 A101-B</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>Room Temperature Bias Test</td>
<td>Evaluates the tolerance when the device is left at a high temperature and high humidity for a long time. Normal test conditions: Ta = 25°C, RH = 90%</td>
<td>EIA/JED-4701 102, MIL-STD-883 1008.2, IEC 60749 1005.8, JESD 22 A101-B</td>
</tr>
<tr>
<td>Lifetime Test</td>
<td></td>
<td></td>
<td>High Temperature High Humidity Preservation Test</td>
<td>Evaluates the tolerance when the device is left at a high temperature and high humidity for a long time. Normal test conditions: Ta = 60°C, RH = 90%</td>
<td>EIA/JED-4701 103, MIL-STD-883 1008.2, IEC 60749 1005.8, JESD 22 A101-B</td>
</tr>
</tbody>
</table>

Figure 8.2 Typical Reliability Test
8.4. Thermal Fatigue Lifetime Test

In a power device, the temperature rises or falls according to the operating conditions where it is used. This temperature change (ΔT) degrades the internal structure of the power device as thermal fatigue. The progress (lifetime) of this thermal fatigue depends on ΔT. That is, its lifetime changes greatly depend on operating and environmental conditions on the system side.

This thermal fatigue lifetime is generally called power cycle lifetime (power cycle tolerance). Power cycle lifetime can be derived from the power cycle tolerance curve showing the relationship of the number of repetition cycles to ΔT, but there are two types of curves (power cycle tolerance curve and TFT tolerance curve) since two different modes exist due to the time dependence of ΔT.

8.4.1. Power Cycle Tolerance Curve (Module Type Device)

Power cycle tolerance is a lifetime curve caused by sharp rising and falling of chip temperature. Figure 8.3 shows the current-application pattern of the power cycle tolerance test. The feature of this failure mode is that when the chip junction temperature (Tj) due to the switching operation changes in the general power module structure shown in Figure 8.4, the stress generated by the difference in the thermal expansion coefficient between the aluminum wire and the power chip causes and grows cracks on this connecting part. This causes the wire to enter peeling mode, which leads to failure (peeling between chip and wire). The amount of tolerance must be taken into consideration when a chip temperature change occurs relatively frequently due to an inverter operation and the like. Figure 8.5 shows the power cycle tolerance curve of the representative product MG1200FXF1US53.

**Figure 8.3 Current-Application Pattern of a Power Cycle Tolerance Test**

**Figure 8.4 Vertical Structure of a Power Device**

**Figure 8.5 Power Cycle Tolerance Curve**
(Representative Product MG1200FXF1US53)
8.4.2. TFT Tolerance Curve (Module Type Device)

This mode is a lifetime curve caused by changes in the case temperature (mainly the base temperature) Tc that follows the rising and falling of the chip temperature. Specifically, tolerance needs to be considered for operations such as system activation/stopping or continuous operation/stopping for a relatively long time, when a temperature change occurs in the power module's Tc.

In this breakdown mode, large stress-strain occurs between the base and the insulating board as shown in Figure 8.4. As this stress is repeatedly generated, cracks form in the solder between the insulating board and the copper base, which leads to breakdown as the thermal resistance increases. This tolerance indicates the lifetime of the solder joint under the insulating board.

Figure 8.6 shows the current-application pattern of the TFT tolerance curve test. In addition, Figure 8.7 shows the TFT tolerance curve of the representative product MG1200FXF1US53.
8.5. Reliability Requirement of Press Pack Type Devices

In the reliability of the press pack type device, it is necessary to consider the mounting method of the device, stress during operation, and stress of the use environment. These are related each other. The following explain major concepts of each for using the devices with high reliability.

- Mounting Press Pack Type Devices
  The press pack type device obtains electrical and thermal contact by applying a load between the main electrodes. Note the following requirements for stack mounting.
  
  (1) The main electrode surface of the device uniformly applies pressure to the specified load value. To apply pressure without variations, attention must be paid to the material and surface flatness of the components (heat sink, etc.) in the stack load portion. When current is applied, the device expands due to the applied load and the pressure rises. Therefore, use items such as Belleville washers with the stack so that contact pressure can be kept uniform.
  
  (2) Ensure good heat conduction and perform appropriate thermal design. In order to obtain a sufficient radiation effect, bring the main electrode of the device directly to the heat sink and apply a conductive thermal compound between them. In addition, cool both the sides of the main electrode of the device.

- Operating Conditions of Press Pack Type Devices
  Voltage and current added to press pack type devices and environmental conditions of use for equipment are major factors affecting reliability. Set the operating point by proper device selection and circuit design according to the target circuit.
  
  The failure rate of press pack type devices is significantly affected by the temperature during operation and the difference between maximum and minimum temperatures. The failure rate increases as the temperature becomes high or the difference between the maximum and the minimum temperature increases. Press pack type devices are used for applications that handle relatively large current and voltage and consume large power. Power consumption generates heat to the press pack type device, which is undesirable in terms of characteristics and reliability, so efficient heat radiation is necessary. In circuit design, make allowance for the superposition of an extraneous surge voltage and noise as well as the deviation of the device characteristics by considering sufficient margins for circuit and protection circuits to significantly prolong the lifetime of the devices and consequently the whole system.
  
  To use the press pack type devices with high reliability, it is recommended to perform derating for the specified voltage, current, power, and temperature with the maximum ratings. However, it is necessary to determine the derating to use while considering reliability and economy.

- Characteristics Variation of Press Pack Type Devices
  Automation of the manufacturing process and progress of manufacturing technology have been remarkable. With these developments and active introduction of new technologies, quality and reliability steadily improve from year to year. Any semiconductor products including press pack type devices are diverse in shape, structure, and dimensions and built by well-controlled and managed precision technologies, based on physicochemical techniques. Therefore, even a slight deviation has a large influence on characteristics, and keeping various characteristics uniform is difficult even with the latest technology. Depending on operating conditions and circuit configuration, it may be necessary to consider the circuit layout according to the characteristics of each device. Additionally, in a press pack type device, multiple semiconductor chips are arranged in parallel inside the package. We uniformize the characteristics of those semiconductor chips in the same package to improve its reliability as a single device.

- Environment Resistance of Press Pack Type Devices
  The press pack type device realizes high reliability by a hermetically-sealed structure. However, direct exposure to harmful gas, saltiness, radiation, and other extrinsic devices may induce characteristics variation and degradation, as well as rusting of the seal and lead parts, so care must be taken. Also, when using the device under high voltage, care must be taken against dew condensation and surface dirt accumulation on the package. If dew condensation or the amount of dirt is severe, there may be a creeping discharge, which may destroy the equipment. For insulation, devices are sometimes immersed in a cooling medium such as oil. In this case, the cooling medium may influence the marking on actual product, and the gate and emitter lead pins, so consult with our company contact in advance of using this technique.
8.6. Thermal Fatigue Mode of Press Pack Type Devices

The thermal fatigue lifetime of a press pack type device strongly depends on the temperature change (ΔT) and the operating conditions in which it will be used.

In a press pack type device, the electrical connection and heat radiation are made possible by the press pack structure, so high thermal fatigue reliability can be expected. Due to this structural feature, unlike a wire bonding type power semiconductor device, there is no constraint on the thermal fatigue lifetime due to power cycle tolerance, but there is TFT tolerance that strongly depends on ΔT.

The degradation mode from TFT tolerance leads to damage to the semiconductor chip due to repeated occurrence of stress caused by the thermal expansion difference between the copper electrode, molybdenum plate, and semiconductor chip that make up the press pack type device.

8.7. Failure Mode of Press Pack Type Devices

The types of failures are broadly classified as short-circuit, open, and degradation.

The major causes of short-circuit failures are 1) overstress such as overvoltage and overcurrent, 2) short-circuit due to high deterioration, and 3) electrochemical reactions. There are other, less-likely causes.

Unlike with semiconductor products with general bonding wires, open failures are less likely to happen due to the structural features of press pack type devices.

In terms of electric characteristics, various cases of deterioration occur, such as reduction of breakdown voltage below standard value, abnormal increase of current, or drifting of characteristic values. Because the devices are made based on physical and chemical techniques, it is conceivable that variations occur due to thermochemical changes in the surface and inside the device depending on the voltage, current, and temperature, and these may increase sequentially and exceed the specified values. The main causes are 1) manufacturing defects, 2) design problems, and 3) handling problems.

In addition, when excessive current flows in a press pack type device, the package is not easily broken by the hermetic sealing structure, but the package can rupture and damage the peripheral equipment depending on the magnitude of the overcurrent.
9. Countermeasures When Problems Occur

When IEGT devices are applied to various circuits, the devices may malfunction or be damaged due to defects such as wiring mistakes, mounting errors, or control signal mismatches. If abnormal device operation or breakdown occurs, clarify the cause and take appropriate countermeasures to avoid a repetition.

In investigating factors when the device breaks down, it is generally easier to get to an understanding by proceeding with FTA (Fault Tree Analysis) as shown in Figure 9.1.

The breakdown mode can be determined by disassembling the broken device and observing the state of the chip. For breakdown mode details, refer to Figure 9.2.

![Figure 9.1 Example of FTA](image)

To check whether the product has broken down, measure and confirm the following (1), (2) for the IEGT device and (3) for the FRD device by characteristics measuring equipment such as a transistor curve tracer.

1. Leakage Current Between G and E
2. Leakage Current Between C and E
3. Leakage Current Between A and K (K: Cathode)

In addition, simple failure determination is possible even if using an instrument that can measure voltage and resistance, such as a tester or battery checker, instead of a curve tracer.
<table>
<thead>
<tr>
<th>Time of Breakdown (Possibility = ◎: Large, ○: Possible, -: Not applicable)</th>
<th>Pellet Breakdown Pattern Diagram</th>
<th>Supplementary Information (TR = IEGT, D = Diode)</th>
<th>Possible Electrical Factors, Others</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-Off Breakdown</td>
<td></td>
<td>One TR CE short, GE short Breakdown in the pattern's cell The size of the trace of breakdown differs depending on the power at the time of breakdown. (Includes chip sorting time) There may be degradation of other chips.</td>
<td>Vcc, Vcp, and Icp were applied, exceeding device tolerance. Ls is excessive. Overcurrent due to SW after FRD breakdown, etc.</td>
</tr>
<tr>
<td>GE Breakdown Voltage Failure 1</td>
<td></td>
<td>At least one TR GE or CE short circuit There may be trace amounts of melted marks.</td>
<td>Applying voltage that exceeds the rating between GE (Includes VGE variation due to dv/dt) Applying voltage between CE with GE open</td>
</tr>
<tr>
<td>GE Breakdown Voltage Failure 2 (Mainly press pack type devices)</td>
<td></td>
<td>One or more TR(s) Gate wiring collapse AI electrode protrudes and short circuits with other wiring Random in the surface</td>
<td>- Wiring collapsed due to excessive repeated press-contact - Foreign particle caught between devices - Wiring collapse and deformation due to excessive or uneven contact pressure</td>
</tr>
<tr>
<td>Overvoltage to CE/AK</td>
<td></td>
<td>One TR or more, or one D or more, breakdown near the end of the chip (Many at chip corners)</td>
<td>- At the time of IEGT shutoff, the surge voltage for FRD reverse recovery exceeding the device tolerance was applied</td>
</tr>
<tr>
<td>Reverse Recovery Breakdown (FRD)</td>
<td></td>
<td>Melting in one or multiple D AK short circuit</td>
<td>- Applying back power by excessive VR, IF, etc.</td>
</tr>
<tr>
<td>After short-time current application Reverse recovery breakdown (FRD)</td>
<td></td>
<td>Melting in the bulk of one D AK short circuit</td>
<td>- Application of excessive back power for a short time (When operating as the FWD of the other arm due to IEGT turn-off breakdown, etc.)</td>
</tr>
<tr>
<td>Cosmic Ray Breakdown (LTDS)</td>
<td></td>
<td>At least one TR or D Part near the chip end or bulk melts in spots.</td>
<td>- Excessive Vcc/VR - High altitude and other environmental impacts</td>
</tr>
<tr>
<td>Surge Current Breakdown (FRD)</td>
<td></td>
<td>At least one TR or D Significantly melting in bulk. In the case of FRD where reverse recovery is involved, multiple melt marks may be generated in peripheral parts.</td>
<td>- Applying current beyond the allowable surge current - In the case of IEGTs, current application exceeding latch tolerance</td>
</tr>
</tbody>
</table>

Figure 9.2 Example of an IEGT/FRD Chip Breakdown Pattern and Estimated Breakdown Mode

Note 1: When the melting area of the main breakdown chip is enormous, adjacent chips may also degrade in breakdown voltage and melt.

Note 2: Some example pattern figures double as an IEGT/diode. (For diode, there is no gate electrode at the right upper corner in the squares. In addition, although the position of the gate electrode in press pack type and module type IEGTs is generally different, it is the same here.)
RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”. Hardware, software and systems described in this document are collectively referred to as “Product”.

- Toshiba reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from Toshiba. Even with Toshiba’s written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though Toshiba works continually to improve Product’s quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant Toshiba information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the “Toshiba Semiconductor Reliability Handbook” and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. Toshiba assumes no liability for customers’ product design or applications.

- Product is neither intended nor warranted for use in equipments or systems that require extraordinarily high levels of quality and/or reliability, and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage and/or serious public impact (“unintended use”). Except for specific applications as expressly stated in this document, unintended use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. If you use Product for unintended use, Toshiba assumes no liability for Product. For details, please contact your Toshiba sales representative.

- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by Toshiba for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.

- Absent a written signed agreement, except as provided in the relevant terms and conditions of sale for Product, and to the maximum extent allowable by law, Toshiba (1) assumes no liability whatsoever, including without limitation, indirect, consequential, special, or incidental damages or loss, including without limitation, loss of profits, loss of opportunities, business interruption and loss of data, and (2) disclaims any and all express or implied warranties and conditions related to sale, use of Product, or information, including warranties or conditions of merchantability, fitness for a particular purpose, accuracy of information, or noninfringement.

- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.

- Please contact your Toshiba sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Toshiba assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.