TC78B004FTG

Usage considerations

Summary

The TC78B004FTG is a three-phase full-wave brushless motor controller IC for office equipment, equipped with a motor speed control function. High-efficiency drive and noise reduction are realized by sine-wave PWM drive with 2-phase modulation system.

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1. Power supply voltage

1.1. Power supply voltage usage range

Table 1.1 Power supply voltage usage range

Characteristics	Symbol	Voltage usage range	unit
Power supply voltage	V_{CC}	10 to 28	V

2. Output current

Absolute maximum rating for each pin is as follows;
LU(U), LV(U), LW(U), LU(L), LV(L), and LW(L): 10 mA (source current in FET drive),
100 mA (sink current in FET drive)
Vreg: 25 mA
The absolute maximum rating should never be exceeded, even for a moment.

3. Control input

3.1. F_{ref} signal input

Table 3.1 Frequency range of external clock

Characteristics	Symbol	Frequency range	unit
External clock frequency	F_{ref}	200 to 4000	Hz

External clock signal is input to F_{ref} pin to control the motor speed. F_{ref} input frequency range is determined by the number bits of the external clock counter and the frequency of the internal reference clock.
When F_{ref} is sufficiently lower than the usage range (200 Hz to 4 kHz), counter overflows.
For example, when F_{ref} is lower than around 150 Hz (i.e., CLK frequency × 8 × 16^3 = 6.55 ms) under the condition that f_x is 5 MHz, counter overflows and the driving output turns off. (Overflow detection)
When f_x is 4 MHz, the counter overflows at 122 Hz, and when f_x is 6 MHz, it overflows at 183 Hz.
Off mode is released when START signal is set high or BRAKE signal is set low, and the motor starts operating after resupply. To startup the operation completely, set the proper frequency (F_{ref}) that does not cause counter overflow, then configure START and BRAKE signals.

4. Detection circuit

This IC incorporates below functions. Note that this circuit does not necessarily provide the IC with a perfect protection from any kind of damages. Make sure to use the IC within the absolute maximum ratings.

4.1. Over current detection circuit

The current is limited by turning off the upper output transistor. The resistor (R11) detects the over current. This circuit operates when the output voltage reaches the reference voltage of the current limiter circuit (V_{dc} = 0.25 V (typ.)).

The current threshold value (I_{OUT}) for over current detection is calculated as follows; I_{OUT} = Reference voltage of current limiter circuit (V_{dc})/Detection resistor (R11). Please adjust the filter values for the resistor of R12 and the capacitor of C12 to reduce the PWM switching noise that causes malfunction of the over current detection.

Ex.) When the resistor (R11) is set 0.06 Ω, I_{OUT} (typ.) = 0.25 V (typ.) / 0.06 Ω ≈ 4.17 A.

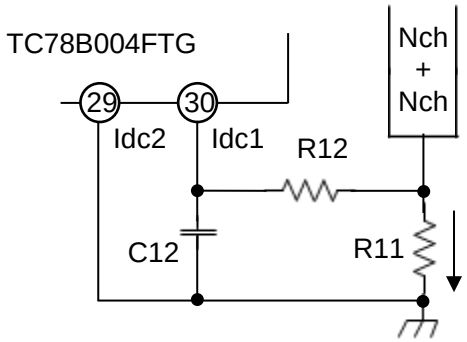


Figure 4.1 Adjustment of the filter value

Test conditions

V_{CC} = 24 V, F_{ref} = 1 kHz (Duty 50 %), No load on motor, R11 = 0.05 Ω, R12 = 1 kΩ, and C12 = 2200 pF

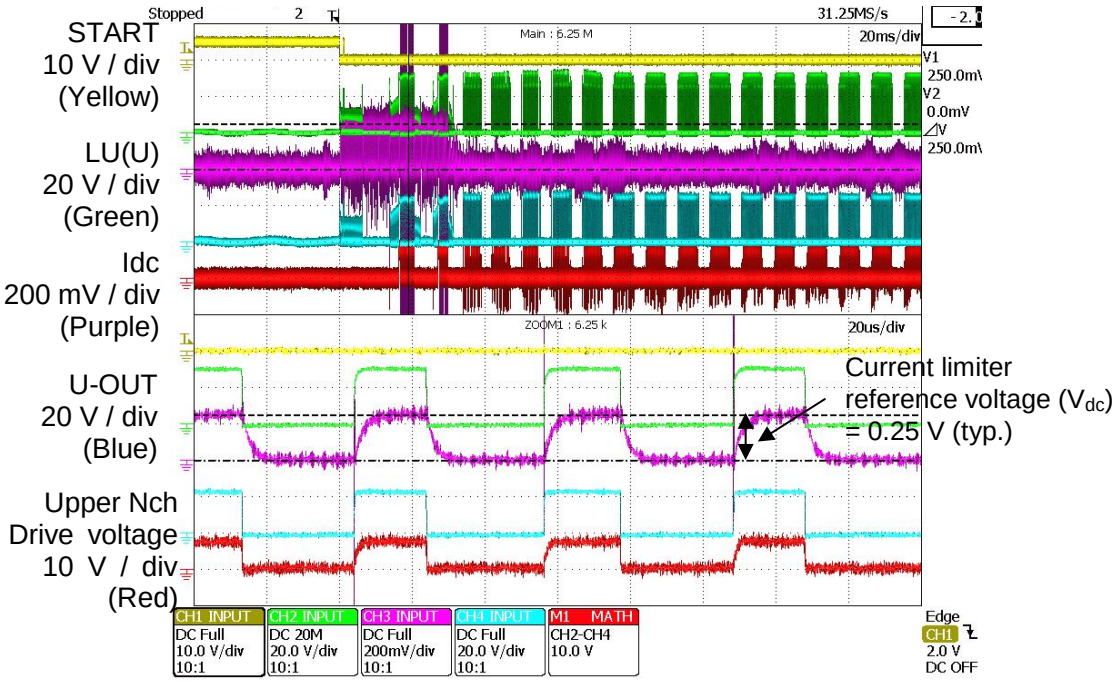


Figure 4.2 Operation waveforms of over current limiter (for reference only)

4.2. Lock protection circuit

Lock protection circuit turns off the output power FET when the motor is locked.
<Setting method>
Below 7 modes are set by the input voltage of CLD pin and the current feedback gain.
<Operation description>
When READY pin outputs high level for the configured lock protection period, all output power FET are turned off.
<Releasing method of turning off the outputs>
Latch mode is released by setting the stop state or the brake state.

Table 4.1 Mode and lock detection time for each external resistor and CLD voltage

External resistance (kΩ)		CLD input voltage (V)		Mode	Lock detection time (s)	Current feedback gain
R1	R2	Min	Max			
100	0	0.00	0.48	Invalid	—	0
82	18	0.68	1.07	Latch	1	0.0625
68	27	1.27	1.65			0.125
56	38	1.85	2.23			0.5
47	51	2.43	2.82		3	0.0625
36	62	3.02	3.40			0.25
0	100	3.60	V_{reg}			0.5

Test conditions
V_{CC} = 24 V, F_{ref} = 1 kHz (Duty 20 %), No load on motor, and CLD pin voltage = 2.23 V

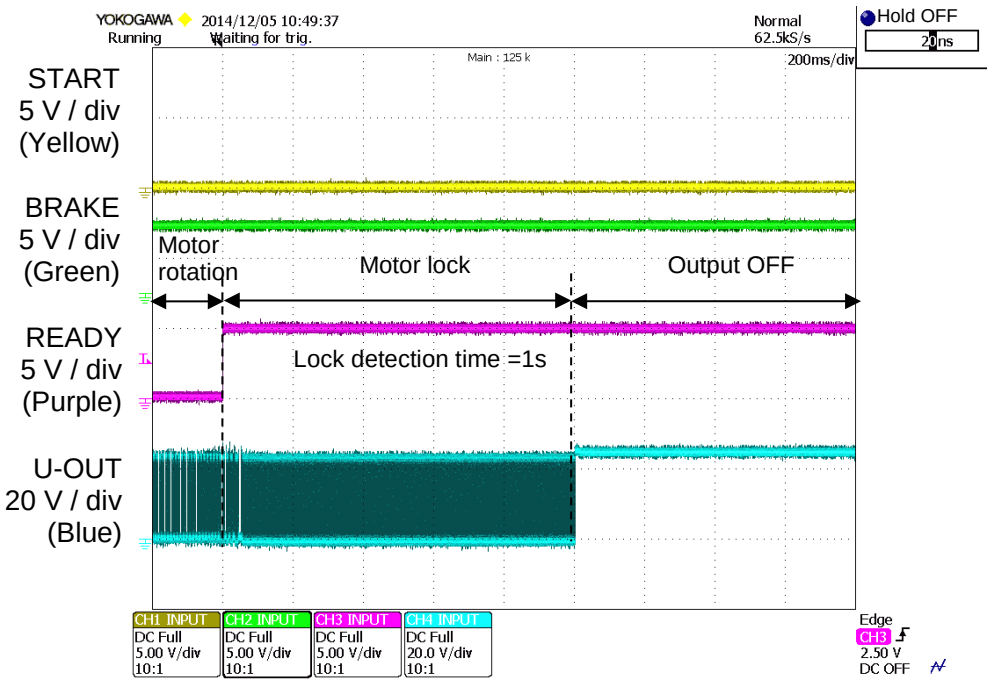


Figure 4.3 Operation waveforms of lock protection (for reference only)

Lock protection voltage is set by the internal AD converter.
The AD converter uses V_{reg} as a power supply and determines the reference voltage with the internal dividing resistor voltage. The lock protection voltage is configured by adopting the external resistors whose errors are ±5 %. Recommended values of external resistors and the CLD input voltage that considers the resistance variation are shown below. CLD pin should not be open. Configure its voltage as below table.
Capacitor should be connected to CLD pin to reduce the noise.

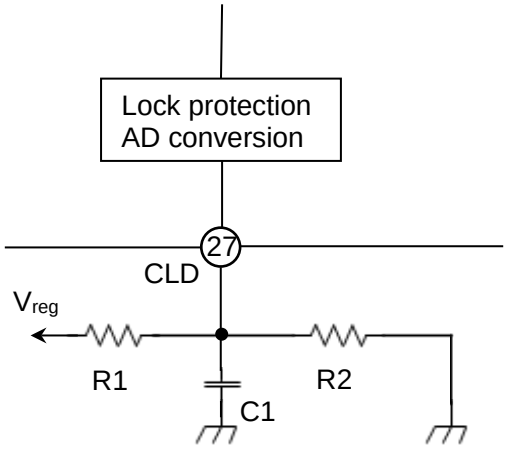


Figure 4.4 Adjustment of CLD input voltage by dividing resistor voltage

Table 4.2 Recommended values of external resistor for CLD pin

Mode	Lock detection time (s)	Current feedback gain	CLD input voltage (V)		External resistance (kΩ)		Dividing resistor voltage in the case the external resistor has variation of ±5% (V)	
			Min	Min	R1	R2	Min	Max
Invalid	—	0	0.00	0.48	100	0	0.00	0.00
Latch	1	0.0625	0.68	1.07	82	18	0.83	0.98
		0.125	1.27	1.65	68	27	1.32	1.53
		0.5	1.85	2.23	56	38	1.90	2.14
	3	0.0625	2.43	2.82	47	51	2.48	2.73
		0.25	3.02	3.40	36	62	3.05	3.28
		0.5	3.60	V_{reg}	0	100	5.00	5.00

4.3. Boost avoiding function

When the motor rotation speed decreases suddenly during sine-wave drive mode, the voltage of the power supply rises because the current flows reversely from the motor to the power supply. This function suppresses the power supply boosting.
When V_{CC} rises, the operation switches from 180°energization (synchronous rectification) to 120°energization (Upper PWM drive).

<Operation conditions>

(1) 180° energization → 120° energization: V_{CC} > 28.8 V(typ.)
(2) 120°energization → 180°energization: Fixed speed rotation (READY signal = Low)

V_{CC} for normal usage should be 27.8 V (minimum of power supply monitor voltage: V_k) or less. This function does not avoid voltage boosting phenomena of all power supplies. When the power supply voltage boosts from the factor of regulator circuits, add other boosting protection circuit. Also, the voltage boosting cannot be suppressed when it is caused by other reasons.

Test conditions
V_{CC} = 24 V, F_{ref} = 600 Hz (Duty 50 %), and motor lock

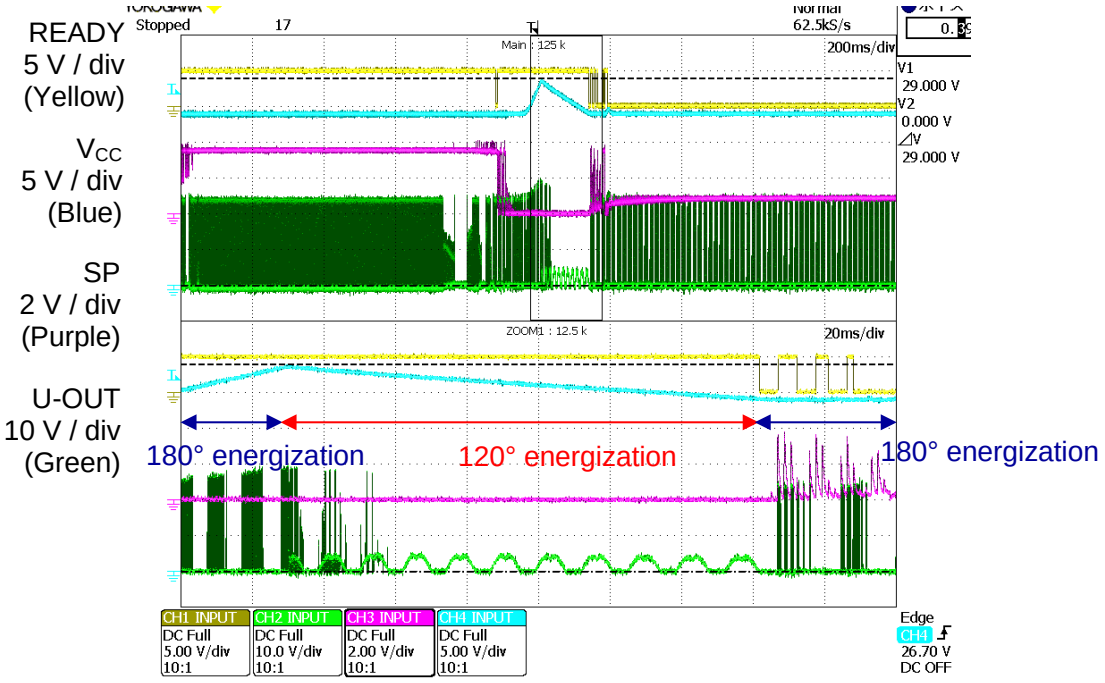


Figure 4.5 Operation waveforms in motor deceleration (for reference only)

4.4. Power supply monitor function

Supply voltage monitor function is incorporated for V_{CC}, V_{reg}, and $V_{reg}1.5$.

V_{CC} supply voltage (24 V, applied externally)

- $V_{CC}(H) \leq$ 9.0 V (typ.), $V_{CC}(L) \leq$ 8.0 V (typ.)

(Power ON)
When V_{CC} is 9.0 V (typ.) or less at the rising edge, external FET (upper and lower) turns off and the internal logic is reset.
(Power OFF)
When V_{CC} is 8.0 V (typ.) or less at the falling edge, external FET (upper and lower) turns off and the internal logic is reset.

V_{reg} supply voltage (5 V, internal reference supply)

- $V_{reg}(H) \leq 4.2$ V(typ.), $V_{reg}(L) \leq 3.5$ V(typ.)

(Power ON)
V_{reg} rises after V_{CC} rises. When V_{reg} is 4.2 V or less, external FET (upper and lower) turns off and the internal logic is reset.
(Power OFF)
V_{reg} falls after V_{CC} falls. When V_{reg} is 3.5 V or less, external FET (upper and lower) turns off and the internal logic is reset.

$V_{reg}1.5$ V supply voltage (internal logic supply)

- $V_{reg}1.5(H) \leq 1.4$ V(typ.), $V_{reg}1.5(L) \leq 1.3$ V(typ.)

(Power ON)
V_{reg} rises after V_{CC} rises. Then, $V_{reg}1.5$ rises after V_{CC} exceeds 9.0 V and V_{reg} exceeds 4.2 V. When $V_{reg}1.5$ is 1.4 V or less, external FET (upper and lower) turns off and the internal logic is reset.
(Power OFF)
V_{reg} falls after V_{CC} falls. Then, $V_{reg}1.5$ falls after V_{CC} falls below 8.0 V or V_{reg} falls below 3.5 V. When $V_{reg}1.5$ is 1.3 V or less, external FET (upper and lower) turns off and the internal logic is reset.

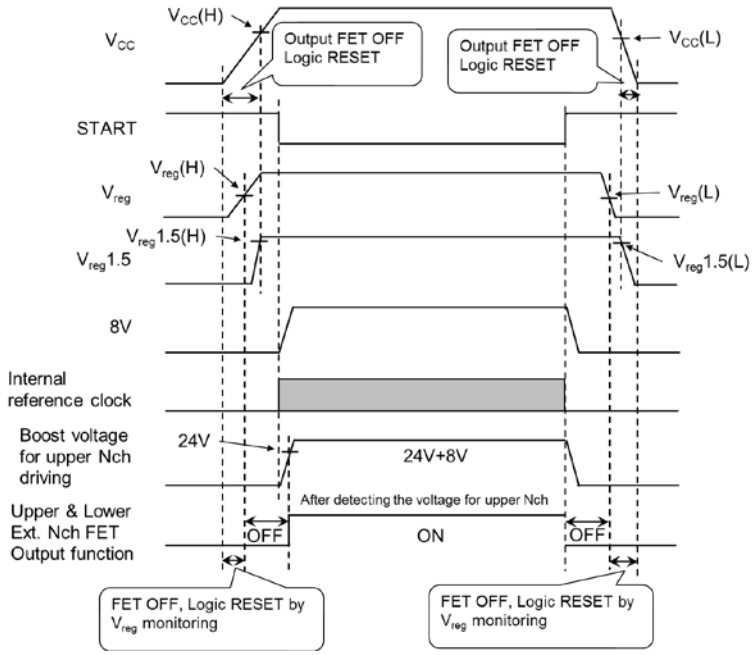


Figure 4.6 Power supply sequence

5. Application circuit example

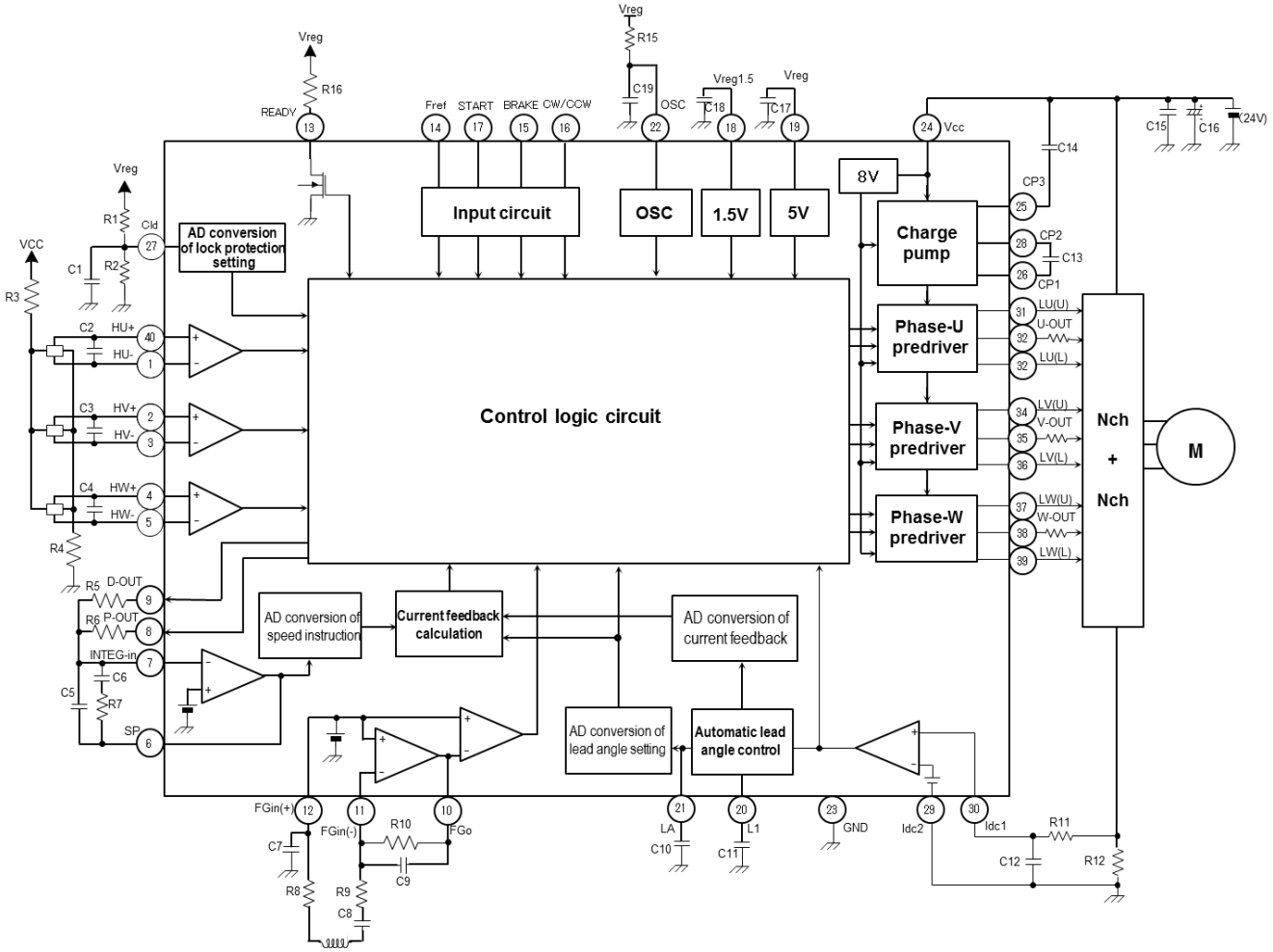


Figure 5.1 Application circuit example

(1) Internal reference clock frequency

The IC generates reference clocks internally with the external capacitor (C) and resistor (R).

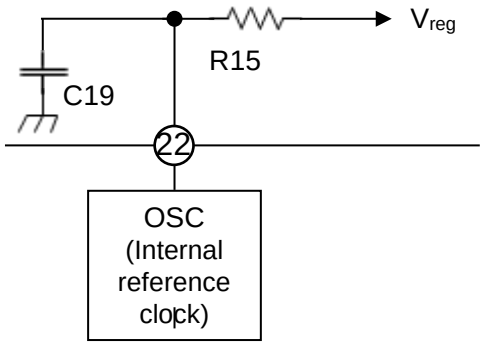


Figure 5.2 Adjustment of internal reference clock frequency

When the external capacitor (C19) is 100 pF, characteristics of the external resistor (R15) and the internal reference clock frequency (f_x) are shown below.

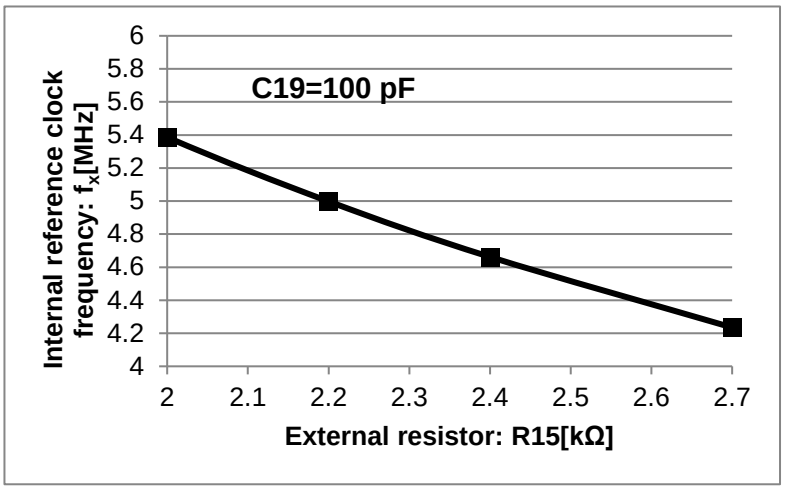


Figure 5.3 Characteristics of external resistor (R15) and internal reference clock frequency (f_x) (for reference only)

When the external resistor (R15) is 2.4 kΩ, characteristics of the external capacitor (C19) and the internal reference clock frequency (f_x) are shown below.

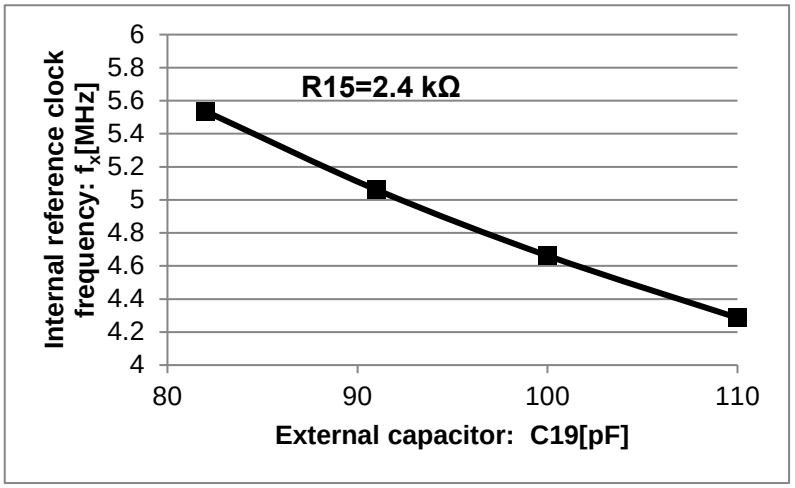


Figure 5.4 Characteristics of external capacitor (C19) and internal reference clock frequency (f_x) (for reference only)

Internal reference clocks are used for below configurations. Consider their variation in setting.

- PWM frequency (fpwm) = f_x (internal reference clock frequency) / 248
- Dead time (t_d) = (1 / f_x) × 6
- Operation frequency of charge pump (voltage boosting circuit): f_x / 16
- Reference clocks for ADC block of lead angle circuit
- Reference clocks for counting time of external clocks
- Reference clocks for FLL and PLL

(2) Capacitor for charge pump

Charge pump circuit boosts voltage with 1/16 of the internal reference clock frequency (fx).
Use below capacitor as a standard.

C13 = 0.022 µF or more
C14 = 0.22 µF or more

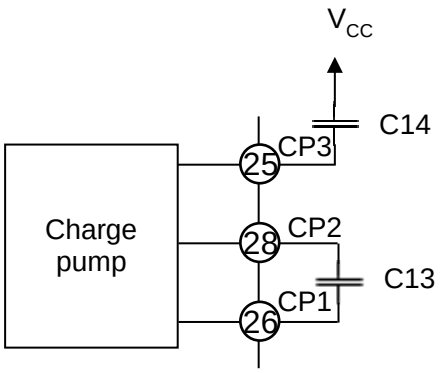


Figure 5.5 Capacitor for charge pump

CP3 voltage is used to drive upper FET. C14 is discharged during FET driving. CP3 voltage may fall depending on the external FET.
Voltage detection for upper Nch transistor is incorporated. It turns on outputs when 'CP3 voltage – V_{CC}' is higher than 6.35 V (typ.) in CP3 voltage rising. And it turns off outputs when 'CP3 voltage – V_{CC}' is lower than 5.8 V (typ.) in CP3 voltage falling. In the normal operation, the voltage should not be in the above range. In the case it is within this range, increase capacities of C13 and C14.

(3) External FET

It is recommended to use TPC8227-H(Note) or TPC8224-H(Note) as an external FET. Connect the resistor of 10 Ω to each OUT pin (U-OUT, V-OUT, and W-OUT) in series.

Note: Our company's products.

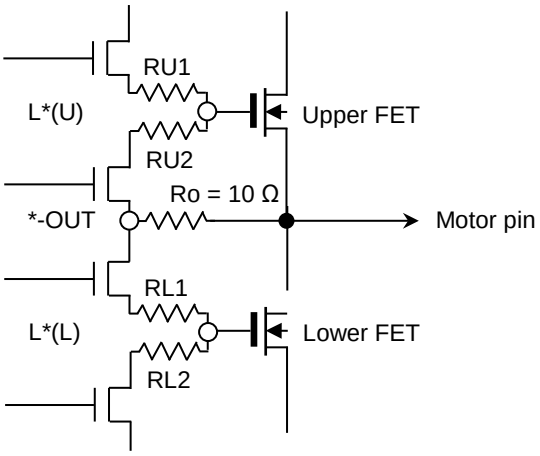


Figure 5.6 External FET

(4) Filter for Idc1 pin

To reduce the noise influence on the power block, which is caused by connecting the over-current detection resistor, connect the filter externally. Connect the ceramic capacitor as close to the IC as possible. GND line of the capacitor should be connected to the GND pin.

(5) Peripheral circuit of FG amplifier

Adjust values of peripheral components according to the used FG frequency.
(Example)

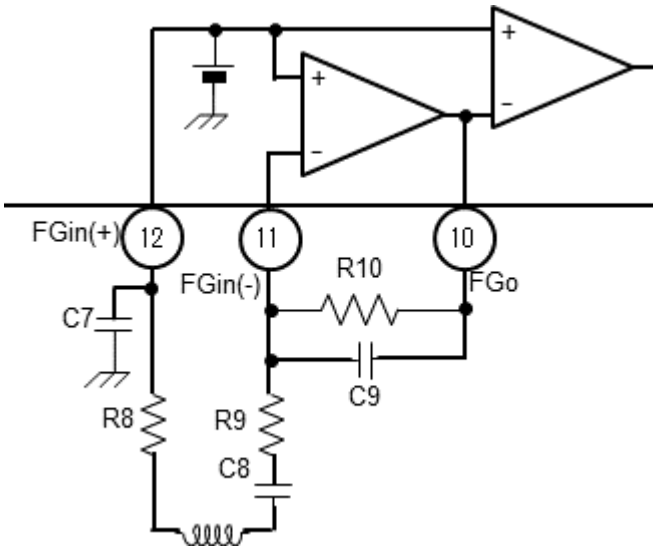


Figure 5.7 Peripheral circuit of FG amplifier

$R9 \leq 1 / (2\pi \times C8 \times F_{ref}(\min))$
$R10 = R9 \times G_{FG}$
$C9 \geq 1 / (2\pi \times R10 \times F_{ref}(\max))$
*G_{FG}: FG gain
When C8 = 0.1 µF, Fref (min) = 500 Hz, F_{ref} (max) = 2 kHz, and G_{FG} = 100 (times),
R9 ≤ 3.18 kΩ, then R9 = 2 to 3 kΩ and R11 = 200 to 300 kΩ.
When R10 = 200 kΩ, C9 ≥398 pF, then C9 = 470 pF to 1000 pF.
C7 = 0.047 µF to 0.1 µF and R8 = 0 Ω.
G_{FG} has an input hysteresis of the FG comparator (0.25 V (typ.) for each side). So, amplitude of FGO waveform should be 0.5 V or more.

(6) Peripheral circuit of integral amplifier

Constant numbers of peripheral circuit should be adjusted according to the used motor.

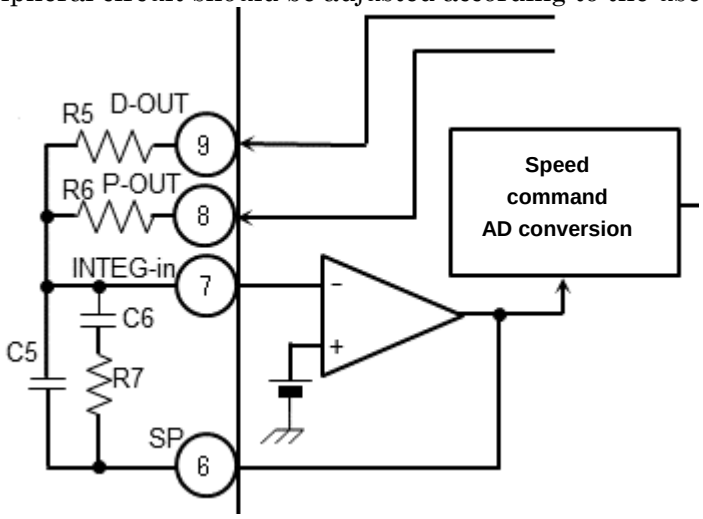


Figure 5.8 Peripheral circuit of integral amplifier

(7) Peripheral circuit of hall bias

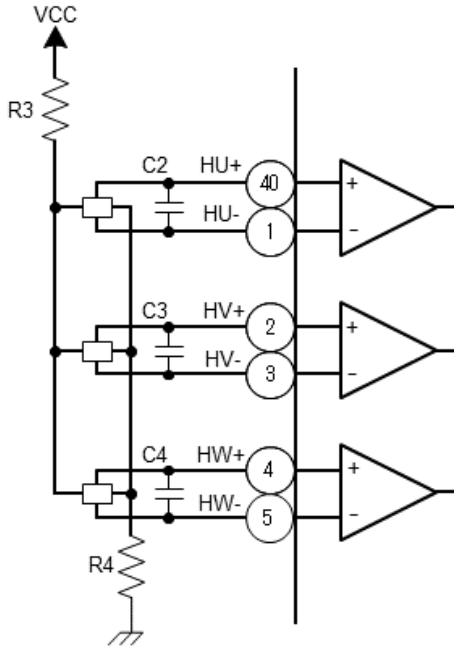


Figure 5.9 Peripheral circuit of hall bias

Adjust resistors of R3 and R4 according to the used hall sensor. (Note)

Note: In using hall IC, configure input voltage of one side Vreg / 2 and the other side in the range of 0 to 5 V.
In case the hall signal has a noise, connect CR filter to the hall signal.

6. Sine-wave drive (60° modulation / 60° reset)

6.1. Sine-wave drive

TC78B004FTG drives by sine-wave PWM control of dual-phase modulation. The position detection signal is modulated, and the modulated signal is compared to a triangular waveform to generate a sine-wave PWM signal. The IC counts the time between adjacent zero-cross points of 3 position detection signals (i.e., 60° electrical angle), and use this time as next 60° phase length.

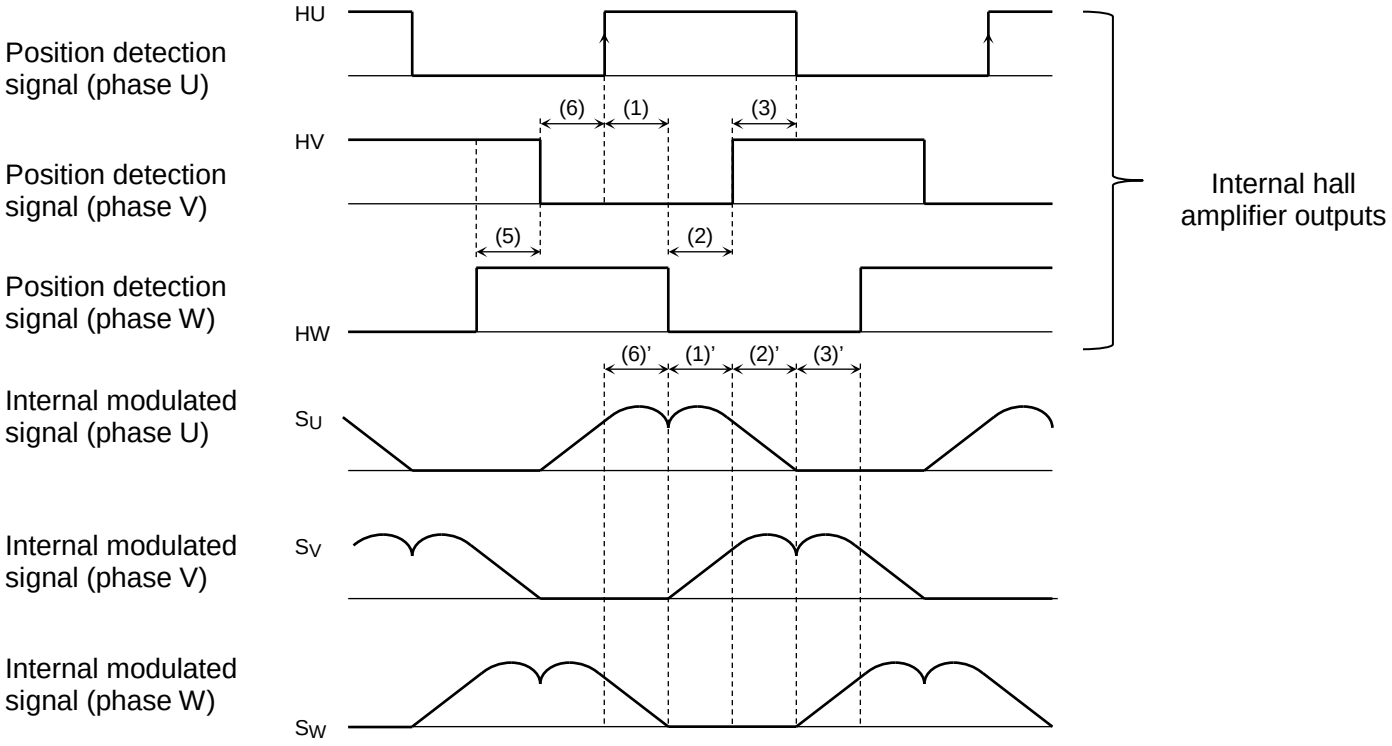


Figure 6.1 Sine-wave drive

6.2. Energization mode switching

TC78B004FTG starts up with 120° energization mode (rectangle-wave drive). And it switches to 180° energization mode (sine-wave drive) in accordance with below sequence.

- First, the frequency of the position detection signal (hall sensor signal) for one phase (f) exceeds the configured frequency (f_H).
- Then, 6 hall switching edges are recognized. ('6' is not for each phase, but total in 3 phases.)

TC78B004FTG switches to 180° energization mode at the falling edge of HA.
(In the case 6th of the switching edge corresponds to the HA falling edge, the mode is switched at the next HA falling edge.)

Position detection signal for one phase → f
Setting frequency → $f_H = 1 / \{ (2^{16} - 1) \times (1 / f_x) \times 6\}$
Internal reference clock frequency → f_x

$f_H > f$: 120° energization mode, $f_H < f$: 180° energization mode.

Switching frequency depends on the internal reference clock frequency (f_x).
Other than startup, TC78B004FTG drives with 120° energization when the motor rotation speed is slow ($f_H > f$).
For noise measurement, it also drives with 120° energization when f is much higher than the usage range as follows;
$f \geq 666.7$ Hz (when $f_x = 4$ MHz), $f \geq 833.3$ Hz (when fx = 5 MHz), $f \geq 1$ kHz (when $f_x = 6$ MHz)
In 120° energization mode, upper transistor is PWM controlled. In 180° energization mode, the operation adopts the PWM control with the synchronous rectification.

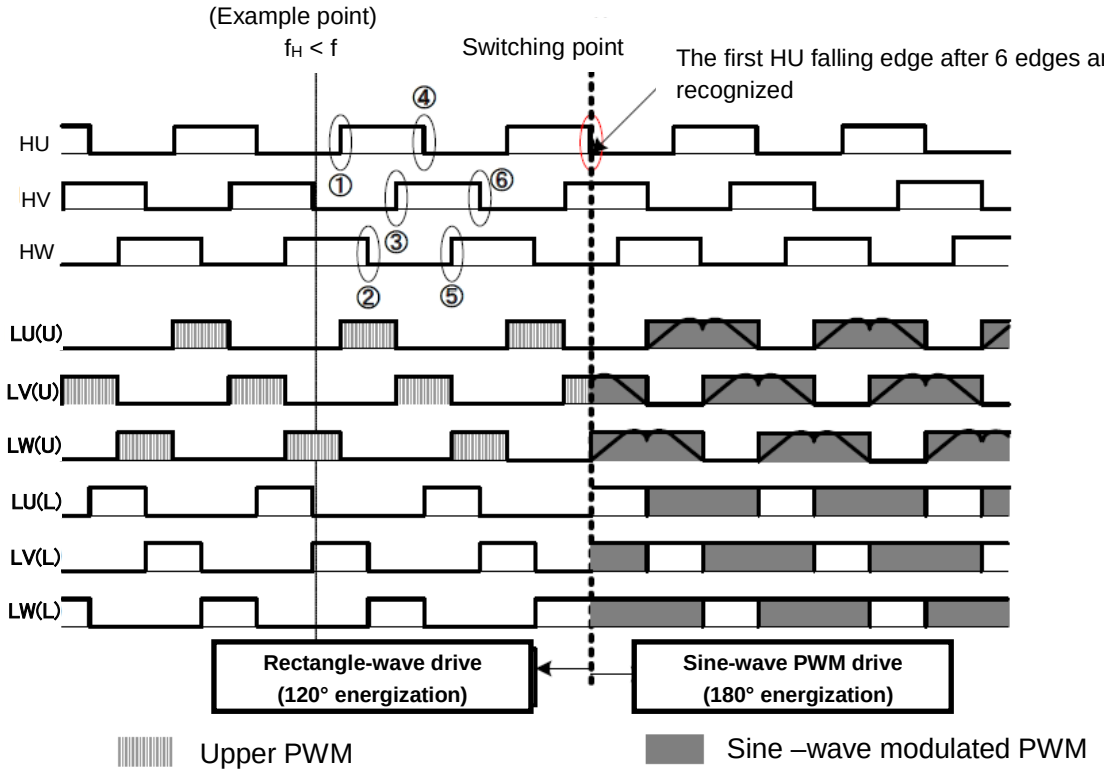


Figure 6.2 Energization mode switching

7. Speed control

Rotation speed is controlled by FLL and PLL.

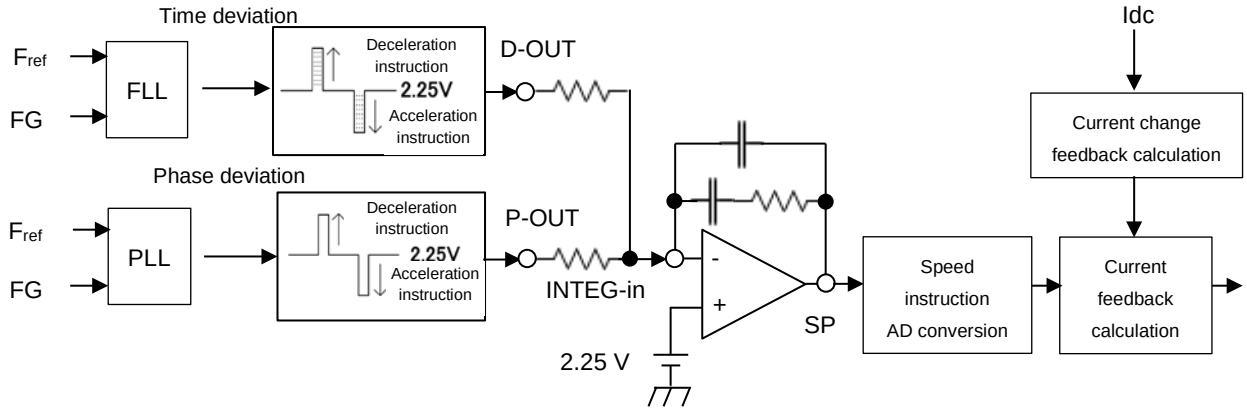


Figure 7.1 Speed control system

D-OUT and P-OUT output pulse voltage (±1.25 V) which corresponds to the time deviation referring to 2.25 V.
(Acceleration instruction is for minus side and deceleration instruction is for plus side, referring to 2.25 V.)
Gain adjustment circuit for D-OUT adjusts the peak voltage with 1/8 resolution.
P-OUT is fixed at ±1.25 V.

P-OUT is output only when READY is low level.
In the case that F_{ref} is not input for a definite period, output FET turns off after recognition period (120 ms when CLD = 0.1 µF) has passed.
When F_{ref} is much lower than the usage range, output FET also turns off.
Even if BRAKE mode is set continually, output FET turns off under below conditions.
$F_{ref} \leq 122$ Hz, 150 Hz, and 183 Hz, when f_x = 4 MHz, 5 MHz, and 6 MHz, respectively.
To release OFF mode, set START pin high or BRAKE pin low, and resume the operation.
Please refer to the data sheet for more details

8. Automatic lead angle control

Internal lead angle function sets the lead angle automatically by feed backing the motor current (i.e., Idc1 voltage).

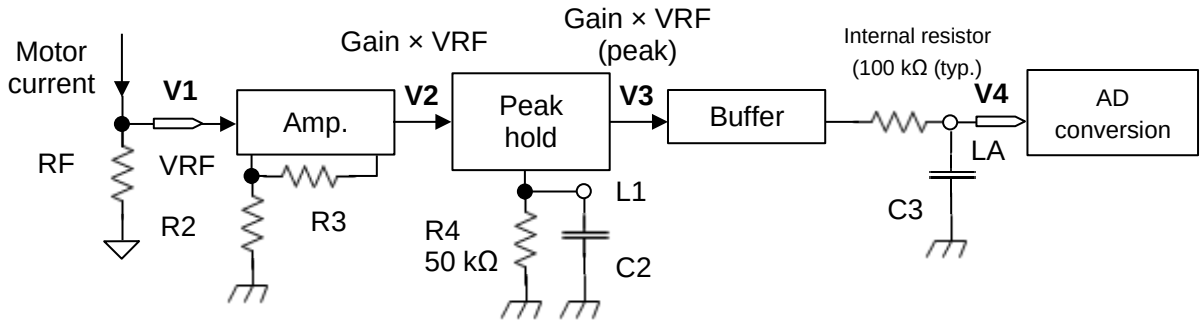
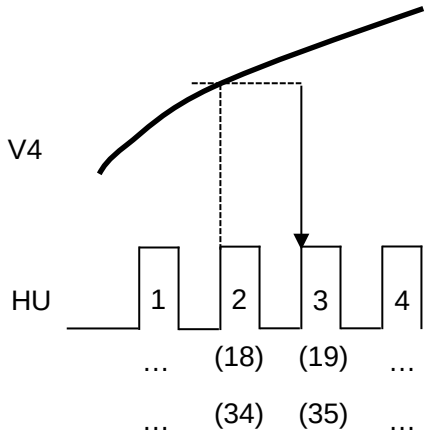


Figure 8.1 Automatic lead angle offset circuit

This function converts the motor current to the voltage with RF resistor and feeds back it. The converted voltage (VRF) is amplified by using 'Amp.'.
Amp. Gain = (R2 + R3) / R2: 17 times (fixed in the IC).
In the peak hold circuit,
(1) When V2 > V3, C2 is charged to equalize V2 and V3.
(2) When V2 < V3, charged C2 is discharged through the resistor (R4), and V3 decreases to V2. Then, V3 continually decreases to V4 through Buffer and the filter circuit (100 kΩ-resistor and C3).
The lead angle is set by AD conversion of V4. The angle is 0° when V4 is 0 V, and 30° when V4 is 2.5 V. Each angle is configured into 16 levels in this range. When V4 exceeds 2.5 V, the lead angle is set 30° (max).

Reflecting timing of V4 at the lead angle setting
V4 is reflected in the lead angle setting every 16 cycles of the Hall signal HU.
After startup, the first reflection is performed at the rising edge of the third cycle. V4 at the rising edge of the second cycle is reflected in the lead angle.
After that, the reflection is performed every 16 cycles.



V4, which is at the rising edge of the second cycle of HU, is reflected in the lead angle, which is at the rising edge of the third cycle. Then, it is performed every 16 cycles.

Figure 8.2 Timing of lead angle setting

9. Current feedback

To avoid irregular rotation, the IC has current feedback functions to suppress the fluctuation of motor current. The feedback of the current fluctuation controls the rotation speed.

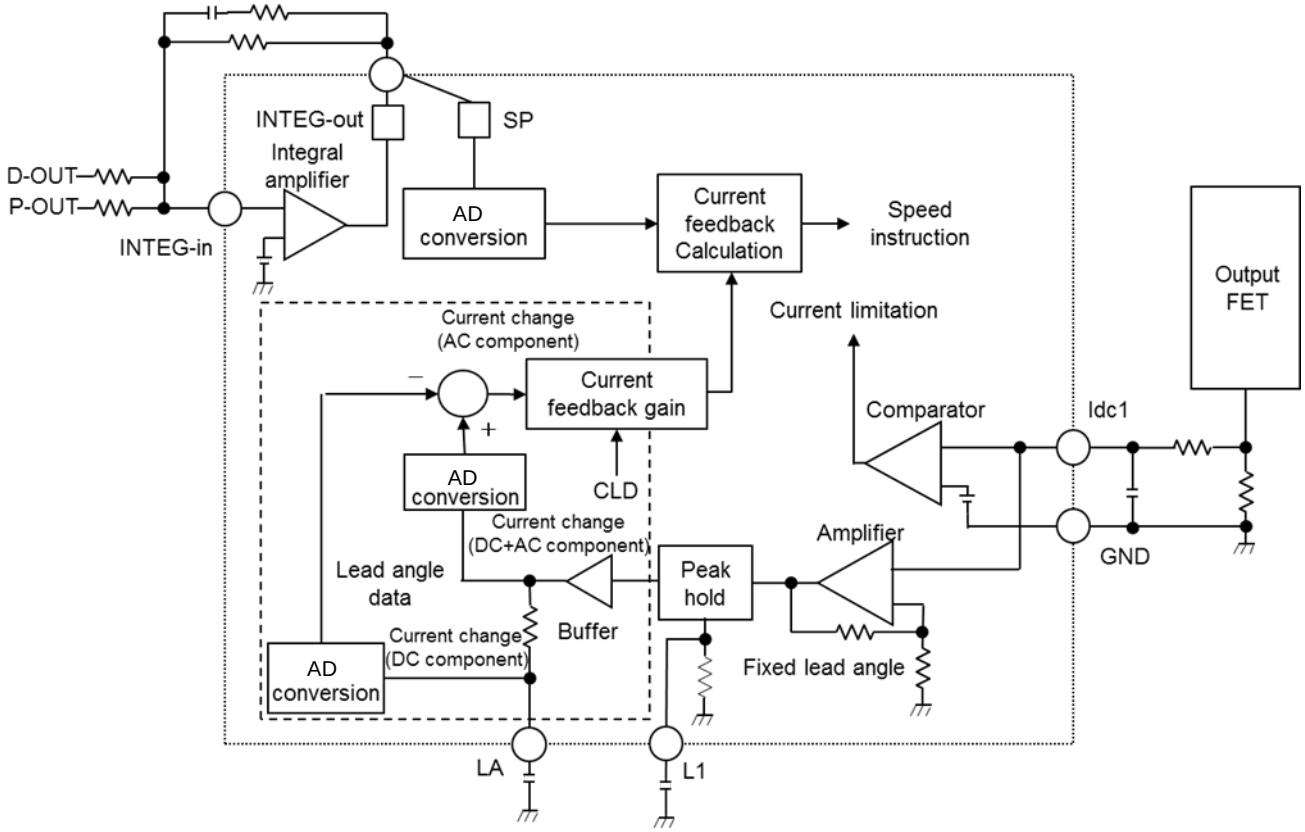


Figure 9.1 Current feedback

Feedback system for speed instruction uses only AC component of the current. Difference of the lead angle data (DC component) and the current feedback data (DC component + AC component) is used as the current feedback value.

P_D

10. Power dissipation

In mounting on board (glass-epoxy board: 76.2 mm × 114.3 mm × 1.6 mm, Cu dimension: 60 %, double-sided)

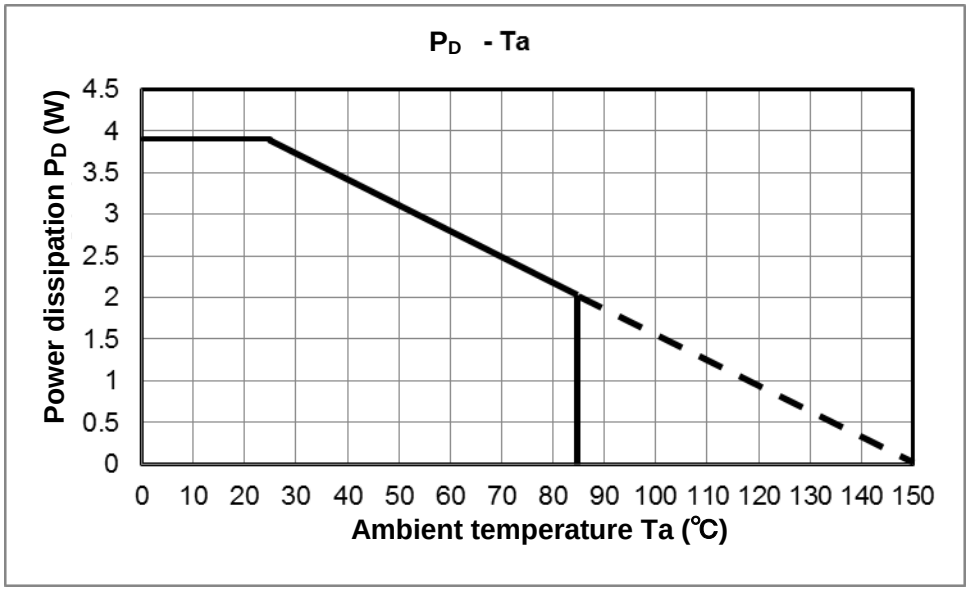


Figure 10.1 P_D – Ta characteristics

11. Notes in designing PCB layout

Please pay attention to the followings in designing layout.

・GND should be solid wired to reduce impedance.

・Output wiring of the external FET, where large current flows, should be as wide as possible.

・The electrolytic capacitor connected to VM pin should be assigned close to the input pin as possible. Otherwise, switching noise may increase.

・The GND of the IC and that of the external FET should be connected to a common grounding point not to have common impedance.

・The dimensions of the land pattern for reference is as follows;

Unit: mm

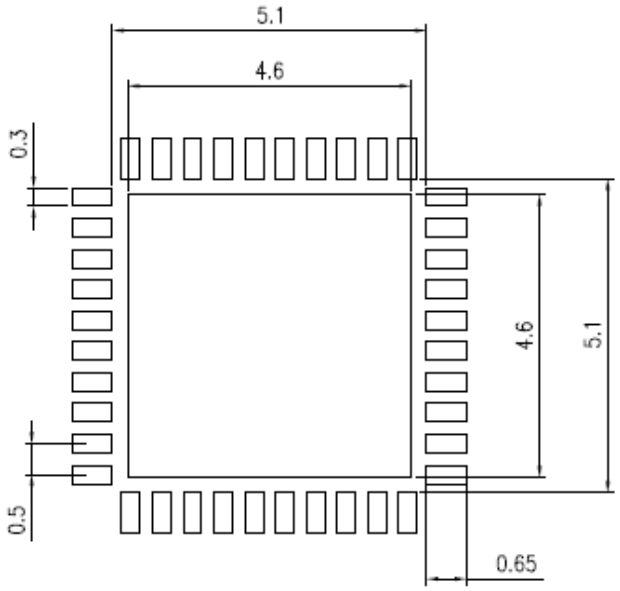


Figure 11.1 Dimensions of the land pattern (for reference only)

Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. We are not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant information of this document and the instructions for the application that Product will be used with or for.

12. Evaluation board

Below evaluation board is available. (Socket type)

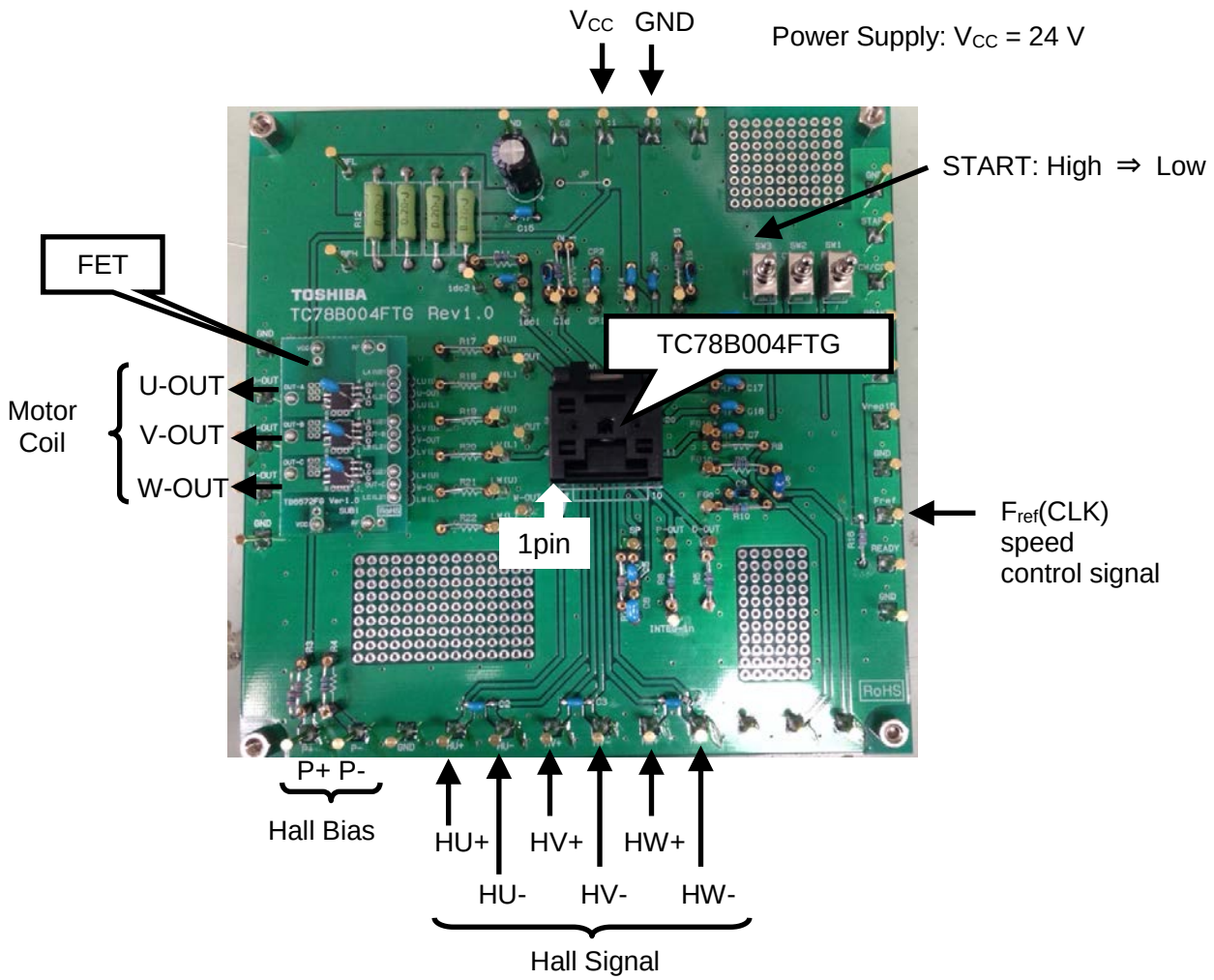


Figure 12.1 Evaluation board for TC78B004FTG

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Any license to any industrial property rights is not granted by provision of these application circuit examples.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(5) Others

Utmost care is necessary in the design of the output, V_{CC}, VM, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

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