Discrete Semiconductor Devices
Hints and Tips for Thermal Design — Part 2

Description

This document provides hints and tips based on simulation results to help you reduce the chip temperature of discrete semiconductor devices.

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1. Introduction

Hints and Tips for Thermal Design for Discrete Semiconductor Devices uses actual measurement data as a basis to provide thermal design tips for reducing chip temperature. As a sequel, Part 2 describes thermal design tips based on simulation data.

Simulation allows great flexibility in analysis once analysis models are created. It is beneficial in that analysis data can be obtained under various test conditions and environments. Unlike real-world devices, devices under simulation do not fail even under extreme conditions. Simulation can therefore replicate conditions that are nearly impossible with actual devices.

We exploited this advantage of simulation to obtain data using models and conditions that are impossible with actual measurement. This application note provides a summary of simulation results. Simulation allows conditions that cannot be replicated physically, making it easy to predict results in extreme device conditions. Therefore, *Hints and Tips for Thermal Design for Discrete Semiconductor Devices — Part 2* provides data that are unavailable in the previous application note based on actual measurement.

2. Summary of simulation results

Simulations are performed under certain fixed conditions. An actual decrease in chip temperature depends on conditions. You can expect, however, that the tendencies in chip temperature that were revealed by simulation also apply to real-world devices. The following table summarizes the simulation results. Use these data as a reference for thermal design. Detailed conditions and data are provided in subsequent sections.

Countermeasure	**Reduction in Chip Temperature**	**Comment**
Multi-layer PCB	Dropped by 7% when the number of PCB layers was increased from 4 to 8	Consideration is required for a PCB because increasing the number of PCB layers, albeit effective, incurs extra cost.
PCB trace thickness	Dropped by 6% when the trace thickness was increased from 70 μm to 105 μm	Increasing the thickness of PCB traces increases their cross section and therefore causes heat to disperse across the PCB more quickly.
Vias just below a drain frame	Compared to a PCB with no via: Dropped by 9% when three vias were added and by 12% when five vias were added	Considerably effective
Peripheral vias	Compared to a PCB with no via: Dropped by 7% when six vias were added and by 10% when ten vias were added	Not as effective as vias placed just below the drain frame However, peripheral vias may prevent heat from conducting to surrounding areas.
Heatsink size	Compared to no heatsink: Dropped by 12% with a heatsink with a height of 1 cm (26 cm^3) Dropped by 19% with a heatsink with a height of 2 cm (52 cm^3)	Adding a heatsink is considerably effective, compared to dissipating heat only from the PCB.

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Heatsink emissivity	Dropped by 12% when the heatsink surface was treated with anodized aluminum (The emissivity increases from 0.04 to 0.8.)	Consideration is required because anodization incurs extra cost.
Thermal interference (Middle device when three devices were arranged in a row)	Increased by 3% when the device spacing was 3 mm Did not increase when the device spacing was 12 mm	In order to prevent thermal interference, it is important not to place heat-generating devices in close proximity. In addition, chip temperature may be reduced by isolating copper traces as appropriate and by adding vias between heat-generating devices to prevent heat dispersion.
Thermal interface material (TIM)	A thinner TIM provides better heat dissipation when the surface area is small.	The TIM thickness should be carefully considered when a TIM is used for a small area.

Note: Thermal interface material (TIM) is a thermally conductive material.

3. Simulation accuracy

Before using simulation data, we compared measured and simulated chip temperatures. Table 1 shows the results. The simulation results were satisfactory; as shown in Figure 1, the accuracy of temperatures was within ±5%

Table 1 - Measured and Simulated Temperatures of MOSFETs

Package	Internal structure	Measured temp. (℃)	Sim temp. (℃)	Temp. difference (℃)	Accuracy
SOP-Adv.	Connector	71.6	69.42	2.18	3.05%
	Ribbon	73.04	72.98	0.06	0.08%
	Wire	77.1	78.05	-0.95	-1.23%
TSON-Adv.	Connector	84.63	83.94	0.69	0.82%
	Ribbon	87.87	86.02	1.85	2.11%
	Wire	91.17	90.14	1.03	1.13%
DSOP-Adv.	Connector	79.86	79.04	0.82	1.03%
PS-8	Wire	94.61	95.87	-1.26	-1.33%
DPAK	Wire	80.93	80.83	0.10	0.12%
D2PAK	Wire	74.35	75.37	-1.02	-1.37%

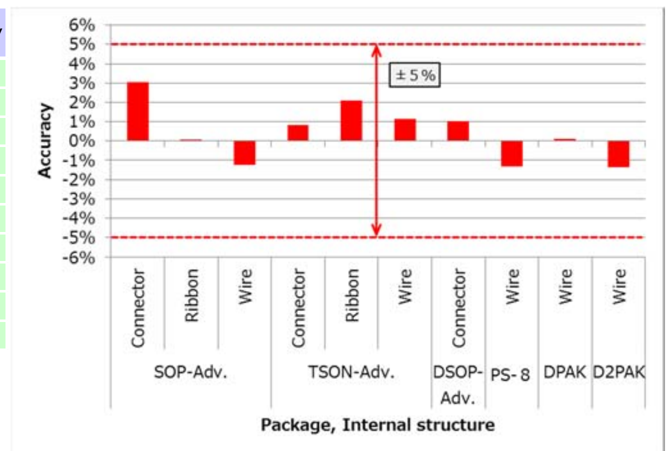

Figure 1 - MOSFET Model Accuracy

Note 1: SOP-Adv., TSON-Adv., and DSOP-Adv. stand for SOP Advance, TSON Advance, and DSOP Advance, respectively.

Note 2: The Simulated column shows the simulated temperatures.

Note 3: Accuracy (%) = ((measured Value – simulated Value) / measured Value) x 100

For simulation, a connector model of the surface-mount SOP Advance package was mainly used.

4. About simulation models

This section describes the basic guidelines adopted for simulation settings and models.

Device:

For simulation, we used a model of a device in a surface-mount SOP Advance package with a connector that provides good heat dissipation paths to a PCB.

PCB:

It is considered that a PCB that is too small for the amount of heat generated adversely affects chip temperature. To avoid an adverse effect, we modeled a PCB two inches square that has four times the area of Toshiba's standard evaluation board (one inch square). Only the solder resist on the backside of the PCB was modeled. The solder resist on the front side was expressed by increasing the emissivity of the board material, i.e., glass epoxy (FR4).

This helps reduce the number of meshes that occur on the surface and provides a model with the same effect as solder resist. The thickness of a PCB was set to roughly 1.6 mm, which is equal to that of commonly used PCBs.

The standard PCB was modeled with four layers. The thickness of all the standard copper traces was set to 70 μm on all the PCB layers. In order to eliminate the impact of the shapes of traces, the inner layers were modeled with solid traces (with 100% fill). In addition, the thicknesses of the prepregs and the core material between traces were made equal on all the layers.

Vias in a model:

All vias were modeled as thermal through-holes (hereinafter simply referred to as "vias"). To make it easy to cut vias in a mesh array, cylindrical vias were represented by cuboids. Vias are 0.25 mm square, which is equal to the cross section of the plated cylindrical vias. Vias were placed on the drain trace that is the primary thermal path in the package. Vias placed on a copper trace just below a device's drain frame (hereinafter "E-pad") were modeled as inner vias while those around the periphery of a device were made outer vias. Outer vias were placed close to a device in order to make it easy to evaluate their effect. We considered that it would be difficult to measure the effect of vias in the second peripheral row. Therefore, we arranged vias in a single row around a device and performed simulations with different via-to-via spacing.

Heatsink:

Since the effect of a heatsink varies with the fin shape, the heatsink was modeled with cuboid blocks. A heatsink with the same shape was used for all simulations, except when it was parametrized.

Thermal interference:

In the thermal interference model, three instances of a device were placed on the common drain trace of the same PCB. For thermal interference modeling, a PCB with the same size as for a single-device simulation was used.

Thermal interface material (TIM)

For all models, the same physical property values were used for the TIM. Instead, its thickness was varied for modeling purposes. We simulated the effect of TIM by placing it between a device and a copper trace and between a copper trace and a heatsink.

- Basic model example

Figure 2 shows a simulation model for a four-layer PCB with a device.

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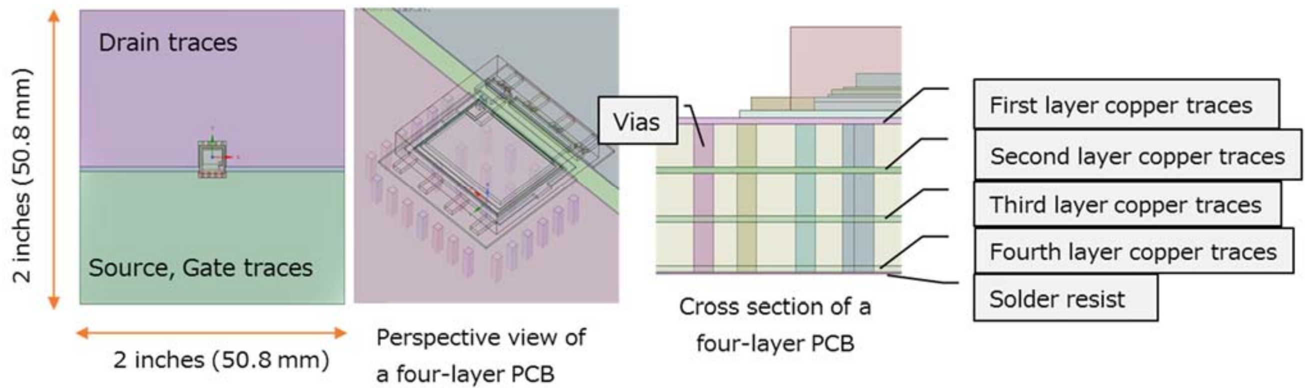

Figure 2 - Simulation Model for a Four-Layer PCB with a Device

5. Thermal interference model

Heat-generating devices are subject to thermal interference according to the distance between them. We created a thermal interference model as shown in Figure 3 in order to examine the impact of thermal interference. To simulate horizontal thermal interference, no vertical via was added to the model since vertical vias block the horizontal heat dispersion. In addition, a two-layer PCB was used so as not to increase the thermal conductivity in the vertical direction. Three devices were placed in proximity at the center of the PCB, and simulations were performed with different device-to-device spacing. Figure 4 shows thermal interference models with different device-to-device spacing.

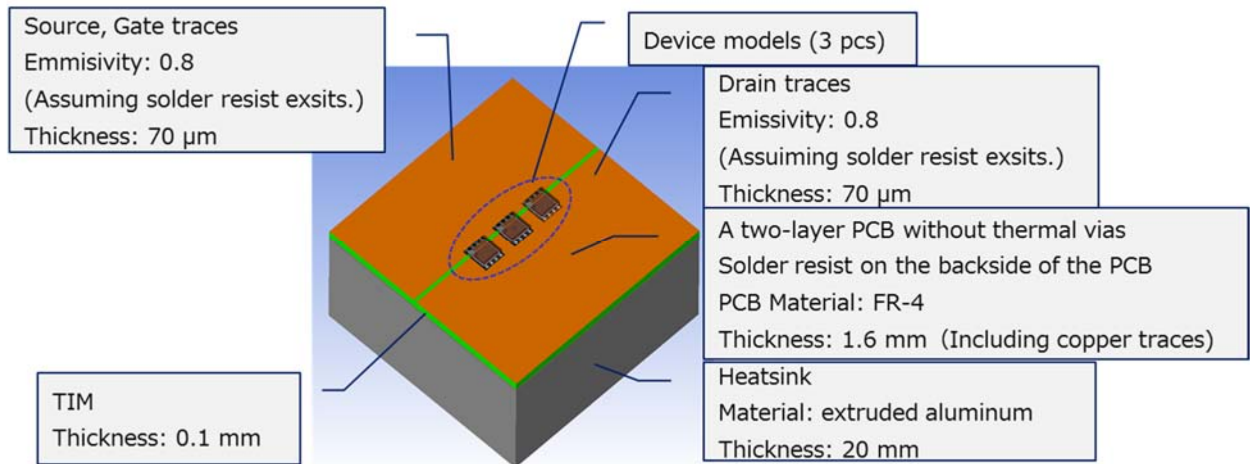

Figure- 3 Thermal Interference Simulation Model

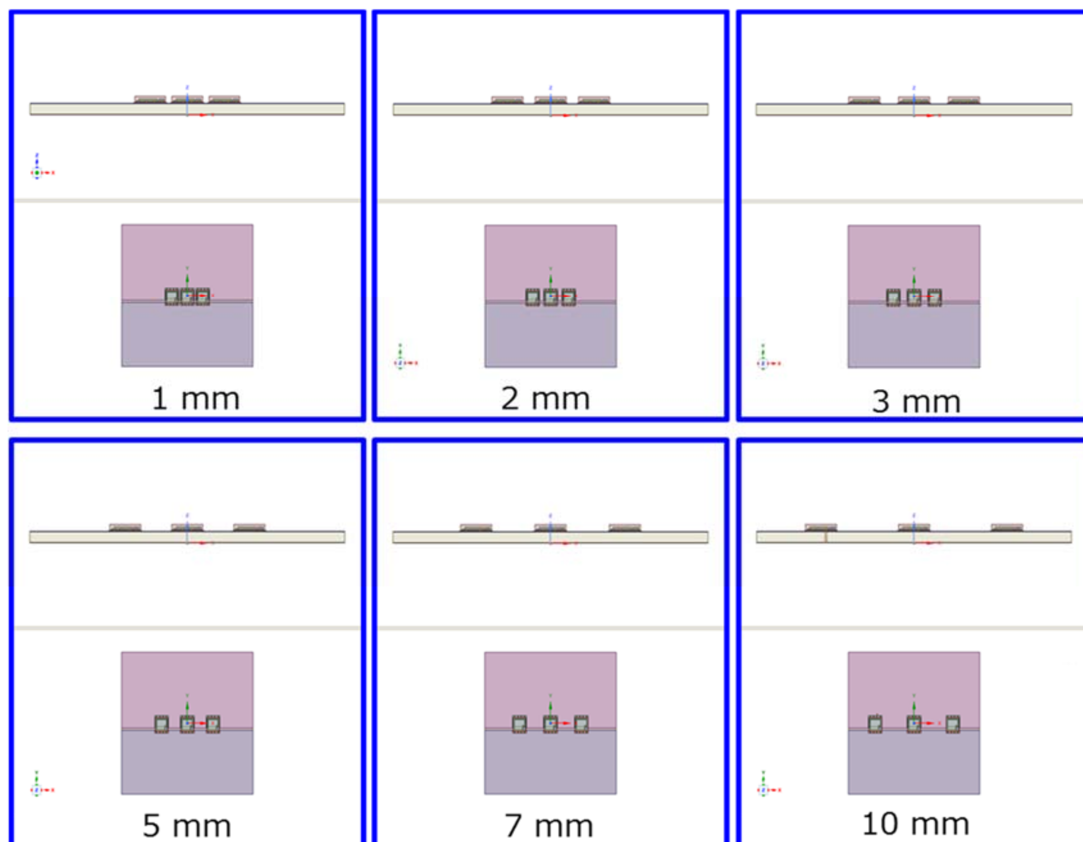

Figure 4 - Simulation Models with Different Device-to-Device Spacing

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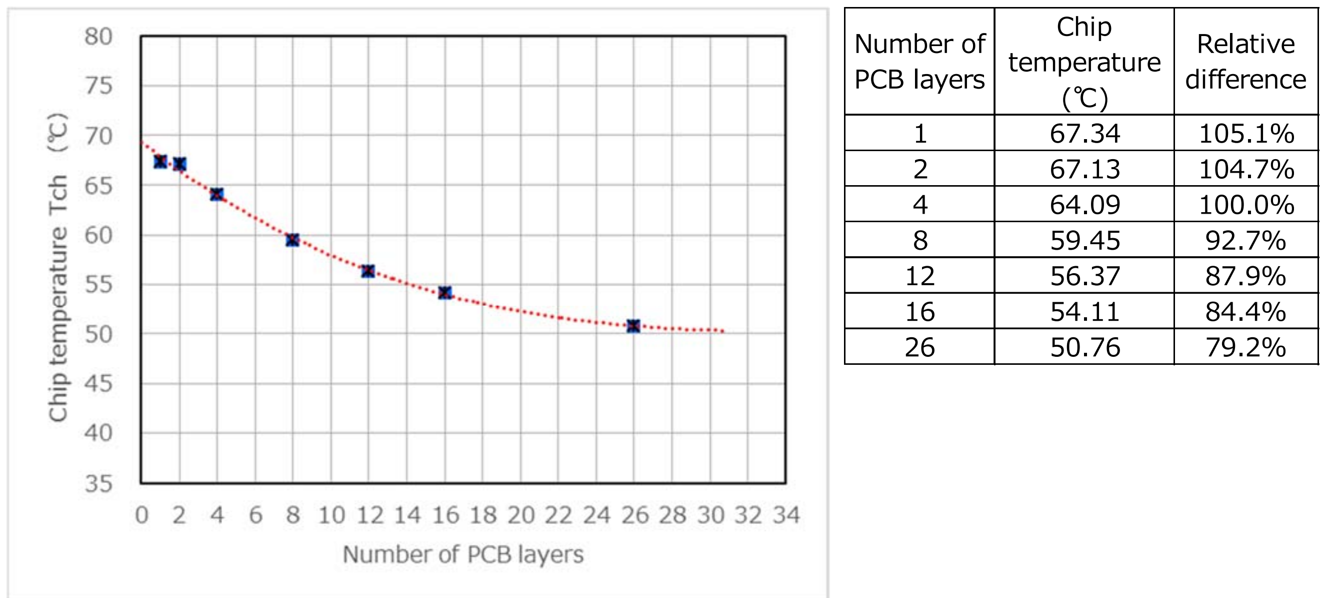
6. Simulation results and tendencies for chip temperature

6.1. Effects of multi-layer PCBs

In line with the shrinking of PCB area, multi-layer PCBs have entered widespread use. Figure 5 shows the effects of using multi-layer PCBs. The PCBs were modeled with no vias and with solid traces (with 100% fill) on inner layers.

A device (in the SOP Advance package) was placed at the center of the PCB. Figure 5 is a plot of chip temperature (Tch) at a power dissipation of 1 W versus the number of PCB layers. A PCB with one surface layer is a single-layer PCB; the chip temperature of a device on a single-layer PCB is also plotted for reference.

The percent values in the table use the chip temperature on a four-layer PCB as a baseline of 100. The chip temperature decreased to roughly 93% on an eight-layer PCB, 88% on a 12-layer PCB, 84% on a 16-layer PCB, and 79% on a 26-layer PCB. Conversely, the chip temperature increased by roughly 5% when the number of inner PCB layers was reduced. The results of this simulation indicate that PCBs with more layers provide better heat dissipation through the PCB. However, it is necessary to consider whether the use of a multi-layer PCB only for heat dissipation purposes can be justified since multi-layer PCBs are more expensive.



Number of PCB layers	Chip temperature (℃)	Relative difference
1	67.34	105.1%
2	67.13	104.7%
4	64.09	100.0%
8	59.45	92.7%
12	56.37	87.9%
16	54.11	84.4%
26	50.76	79.2%

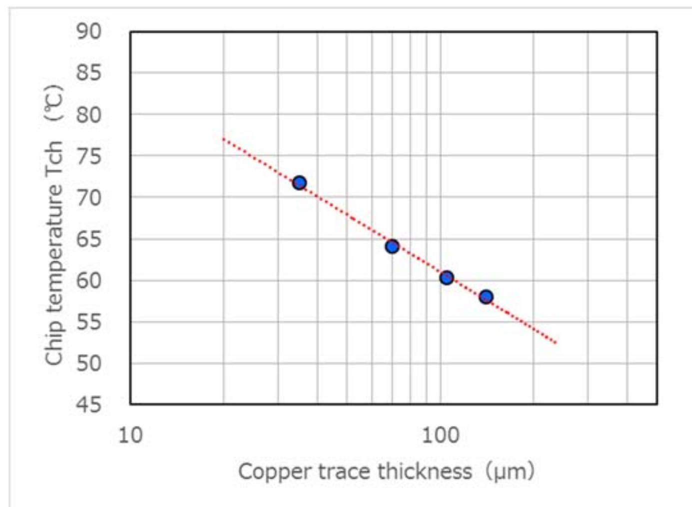
Figure 5 - Number of PCB Layers vs. Chip Temperature

6.2. Effect of the PCB trace thickness

Using a four-layer PCB, we simulated the impact of the thickness of copper traces on Layer 1 (top layer) and Layer 4 (bottom layer). Figure 6 shows the simulation results. The thicker the copper traces, the lower the chip temperature (Tch). Figure 6 indicates there is a strong positive correlation between the reciprocal of copper trace thickness and chip temperature. The area of copper traces is the same in all models. It is therefore considered that thicker copper traces with larger cross sections help conduct more heat. As heat disperses more rapidly across the PCB, thicker copper traces provide higher heat dissipation performance.

Compared to copper traces with a thickness of 70 µm (2 oz), those with a thickness of 35 µm (1 oz) led to a roughly 12% rise in chip temperature. The use of 105-µm (3-oz) copper traces caused the chip temperature to decrease to roughly 94% of the baseline of 70-µm copper traces while the chip temperature decreased to about 91% by using 140-µm (4-oz) copper traces.

Copper traces on 1 & 4 layer		Chip temperature (℃)	Relative difference
(µm)	(oz)		
35	1	71.71	111.9%
70	2	64.09	100.0%
105	3	60.32	94.1%
140	4	58.06	90.6%



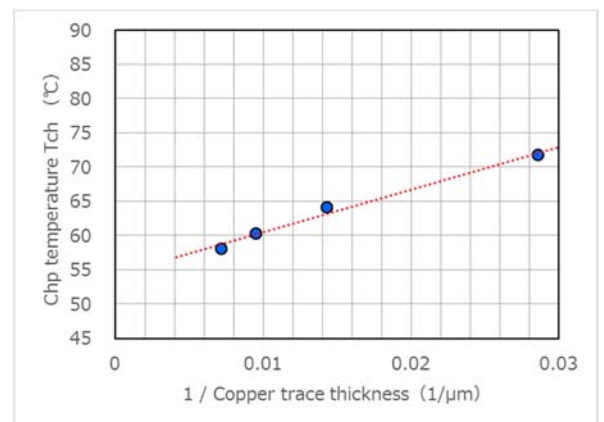


Figure 6 - Copper Trace Thickness vs. Chip Temperature

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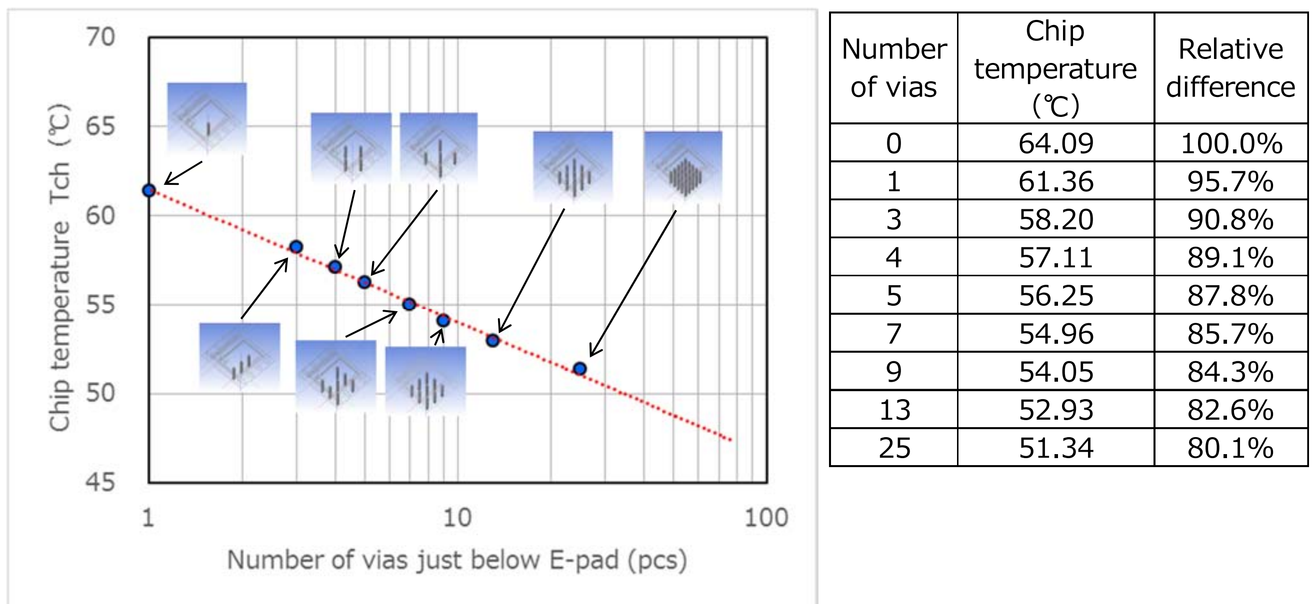
6.3. Effect of vias just below E-pad

For this simulation, we created a model for a four-layer PCB having a device at its center and through-vias that run from Layer 1 to Layer 4 just below E-pad. Figure 7 shows the results of simulation for different numbers of vias.

It plots the chip temperatures for PCBs with 1, 3, 4, 5, 7, 9, 13 and 25 vias. A PCB with nine vias caused the chip temperature to drop to roughly 84%, compared to the chip temperature on a PCB with no via. When a PCB with 25 vias was used, the chip temperature decreased to roughly 80% of the baseline.

A PCB with more vias provides a greater effect. However, E-pad size is finite and imposes a limit on the number of vias that can be added. Solder might flow into vias during board assembly; thermal performance could be adversely affected if solder causes voids to form just below E-pad. It is therefore important to add an appropriate number of vias.



Number of vias	Chip temperature (℃)	Relative difference
0	64.09	100.0%
1	61.36	95.7%
3	58.20	90.8%
4	57.11	89.1%
5	56.25	87.8%
7	54.96	85.7%
9	54.05	84.3%
13	52.93	82.6%
25	51.34	80.1%

Figure 7 - Number of Vias Just Below E-pad versus Chip Temperature

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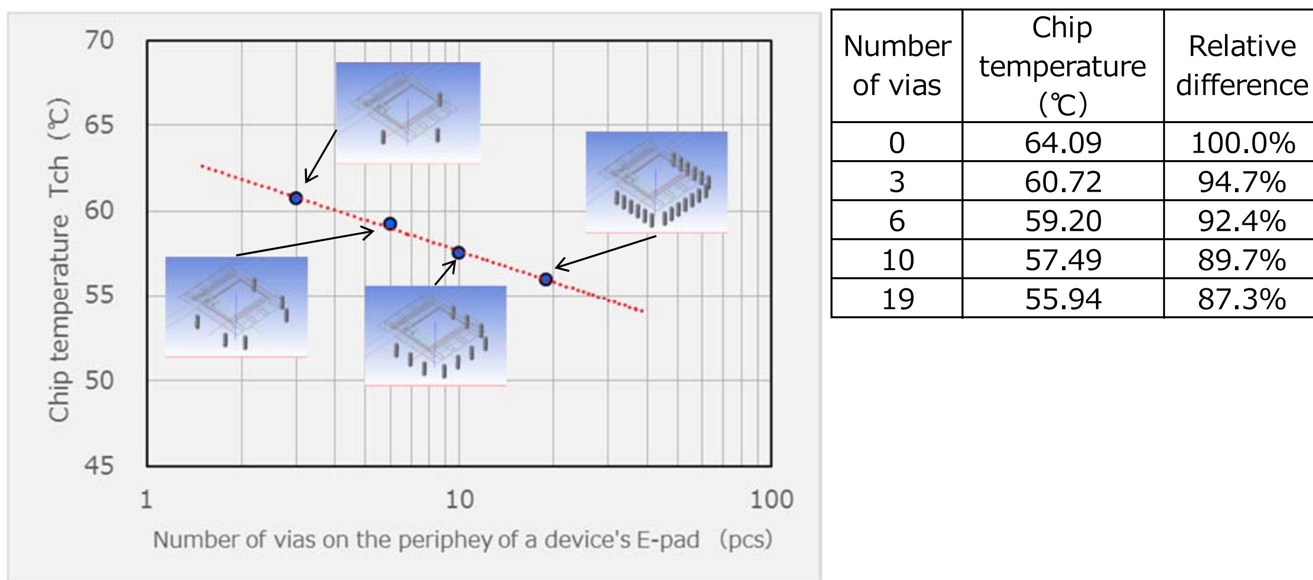
6.4. Effect of peripheral vias

We used the same model as that used in Section 6.3 and added vias on the periphery of E-pad to simulate their effect on chip temperature. Figure 8 shows the simulation results. In order to measure the effect of peripheral vias accurately, vias below E-pad were removed. Peripheral vias were arranged in one row as close as possible to E-pad. The same number of vias was placed on each side of E-pad, and simulations were performed with 3, 6, 10 and 19 vias.

Figure 8 shows that a PCB with more vias led to lower chip temperature. A PCB with 19 vias (the greatest among all models) caused the chip temperature to decrease to roughly 87.3% relative to the chip temperature on a PCB with no via. Peripheral vias are effective in reducing chip temperature although they are slightly less so than those just below E-pad.

Vias just below E-pad are closest to the heat source (i.e., chip) and therefore have a significant effect in reducing chip temperature. In contrast, peripheral vias help disperse the heat that has transferred through copper traces via conduction. Dissipating heat close to the heat source is most effective in reducing chip temperature.



Number of vias	Chip temperature (℃)	Relative difference
0	64.09	100.0%
3	60.72	94.7%
6	59.20	92.4%
10	57.49	89.7%
19	55.94	87.3%

Figure 8 - Number of Vias on the Periphery of a Device's E-pad vs. Chip Temperature

Figure 9 compares data for vias just below E-pad and peripheral vias. It indicates that vias just below E-pad are more effective. Vias just below E-pad should be given precedence over peripheral vias in order to obtain a greater effect with the same number of vias. This is particularly important when heat from surface-mount devices is dissipated to the PCB.

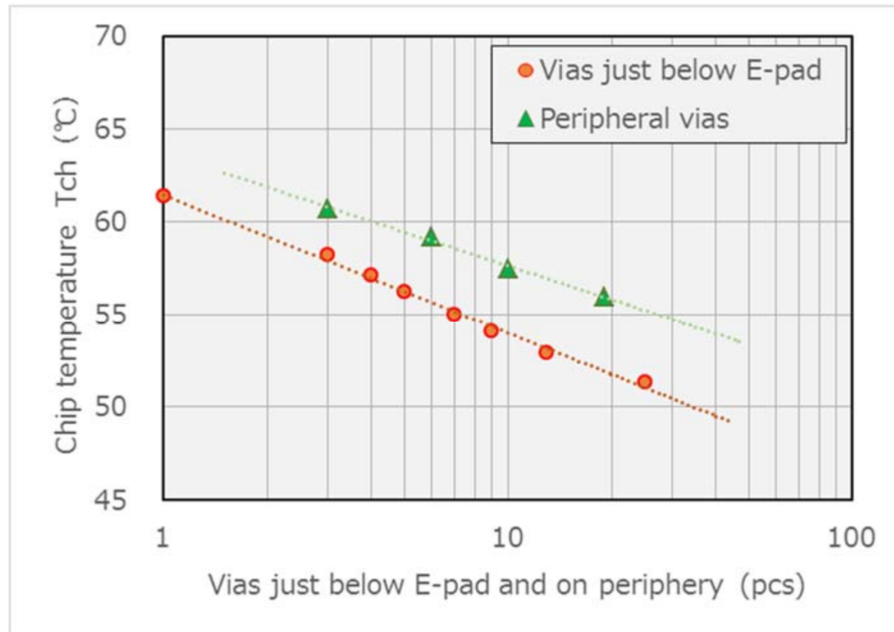
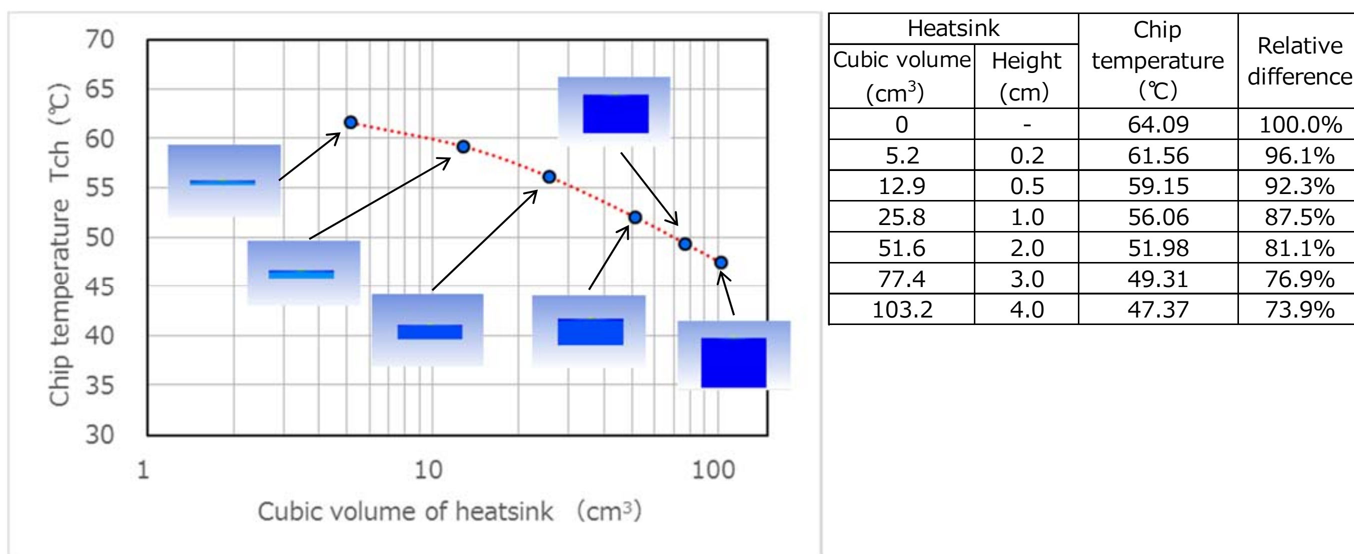


Figure 9 - Vias Just Below E-pad vs. Peripheral Vias

6.5. Effect of the heatsink size

We used a four-layer PCB having nine vias just below E-pad and 19 vias on its periphery. Simulations were performed using heatsinks with different sizes. Figure 10 shows the chip temperatures obtained by simulation. In all the models, the area of contact between a heatsink and a PCB is roughly 25.8 cm^2 (5.08 × 5.08 cm). Simulations were performed, varying the height and thus the cubic volume of the heatsink. Compared to a PCB without a heatsink, a PCB having a heatsink with a height of 1 cm caused the chip temperature to decrease to roughly 87.5% whereas a PCB having a heatsink with a height of 2 cm caused the chip temperature to decrease to roughly 81.1%. Figure 10 indicates that larger heatsinks are more effective in reducing chip temperature. The use of a heatsink is considerably more effective in reducing chip temperature than other measures.



Heatsink		Chip temperature (℃)	Relative difference
Cubic volume (cm^3)	Height (cm)		
0	-	64.09	100.0%
5.2	0.2	61.56	96.1%
12.9	0.5	59.15	92.3%
25.8	1.0	56.06	87.5%
51.6	2.0	51.98	81.1%
77.4	3.0	49.31	76.9%
103.2	4.0	47.37	73.9%

Figure 10 - Cubic Volume of Heatsink vs. Chip Temperature

6.6. Effect of heatsink emissivity

Next, we used the previous model with a 2-cm heatsink to simulate the effect of heatsinks with different emissivity. Figure 11 shows the simulation results. A heatsink made of aluminum has an emissivity of about 0.04 on polished surfaces. Anodization helps increase its emissivity to 0.8.

Figure 11 indicates that heatsinks with higher emissivity led to lower chip temperatures. There is an approximately 7°C difference in temperature between polished and anodized heatsinks. Anodized heatsinks have an advantage over polished heatsinks in dissipating heat. Although anodization is an effective solution for reducing temperature, it is necessary to consider whether to use an anodized heatsink because anodization treatment incurs extra cost.

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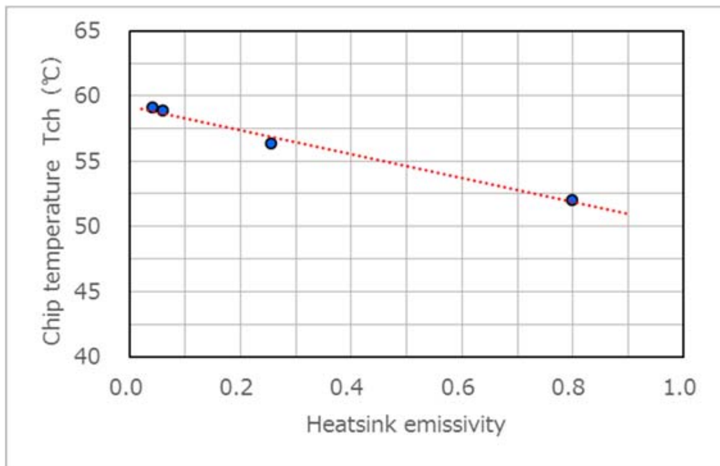


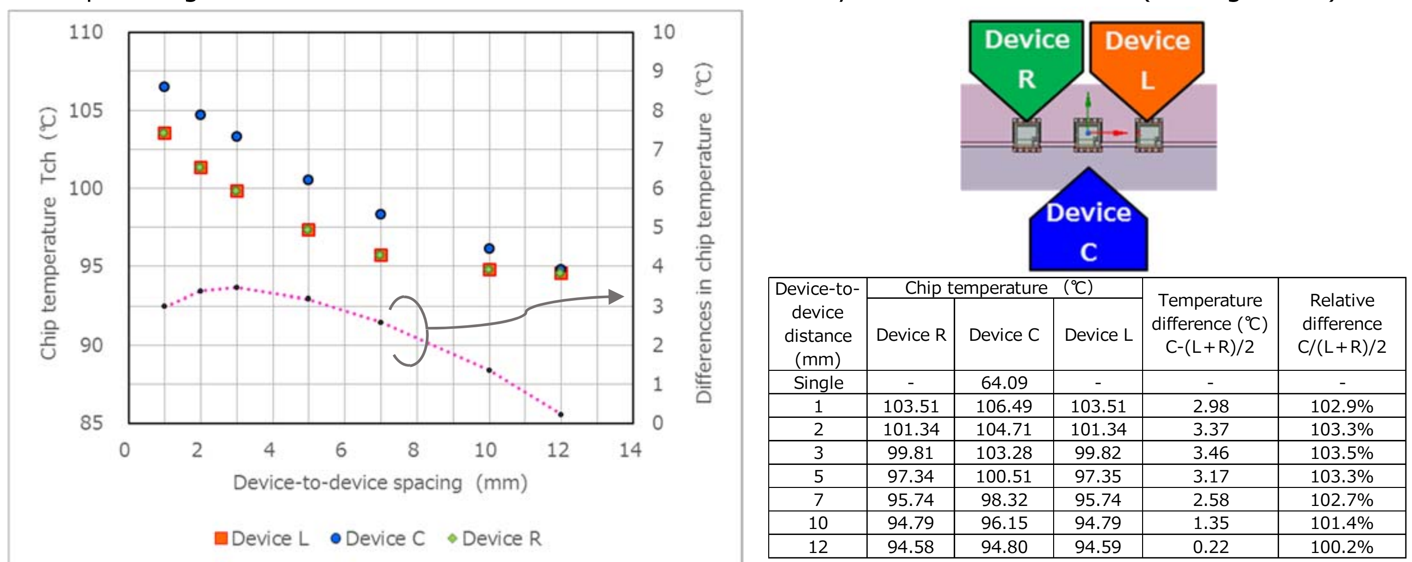
Surface Condition	Heatsink emissivity	Chip temperature (℃)	Relative difference
Polished	0.041	59.05	100.0%
Coarse	0.060	58.81	99.6%
Heavily oxidized	0.255	56.35	95.4%
Anodized	0.800	51.98	88.0%

Figure 11 - Heatsink Emissivity vs. Chip Temperature

6.7. Effect of thermal interference

Figure 12 shows the results of simulating a thermal interference model on which three devices are heated on the same PCB. The device-to-device spacing was used as a parameter for thermal interference. When three devices were tightly arranged, the chip temperature of the middle device, C, became the highest since it was affected by the heat generated by the other two devices. The chip temperature of the middle device became lower as the device-to-device spacing was increased. When the device-to-device spacing was 12 mm, thermal interference became less apparent, causing the chip temperatures of the three devices to become almost equal. Compared with the case of a PCB with only one device, thermal interference among multiple devices caused their chip temperatures to increase much more considerably Differences in chip temperature between the middle device and the other devices (as indicated by the dashed line in Figure 12) became smaller at a device spacing of 3 mm or less. It is considered that when three devices are placed at a spacing of 3 mm or less, the chip temperatures of all three devices increase, reducing their differences. Special care should be exercised when devices are mounted on a PCB at a high density.

Thermal interference can be avoided by modifying device placement and PCB traces. For example, heat-generating devices should not be placed adjacent to each other or in proximity, and copper traces should be isolated. Adding vias between heat sources is also effective. Vias prevent heat from spreading in the horizontal direction and release it vertically across a PCB instead (see Figure 13).



Device-to-device distance (mm)	Chip temperature (℃)			Temperature difference (℃) C-(L+R)/2	Relative difference C/(L+R)/2
	Device R	Device C	Device L		
Single	-	64.09	-	-	-
1	103.51	106.49	103.51	2.98	102.9%
2	101.34	104.71	101.34	3.37	103.3%
3	99.81	103.28	99.82	3.46	103.5%
5	97.34	100.51	97.35	3.17	103.3%
7	95.74	98.32	95.74	2.58	102.7%
10	94.79	96.15	94.79	1.35	101.4%
12	94.58	94.80	94.59	0.22	100.2%

Figure 12 - Thermal Interference Simulation

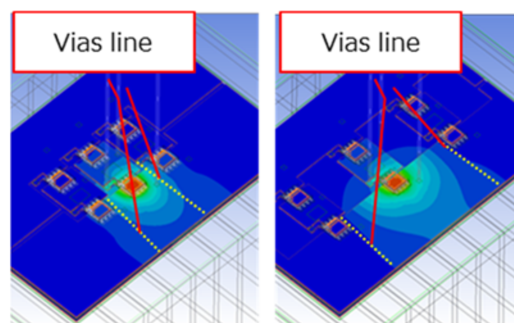


Figure 13 - Peripheral Vias for the Prevention of Thermal Interference in Different Models

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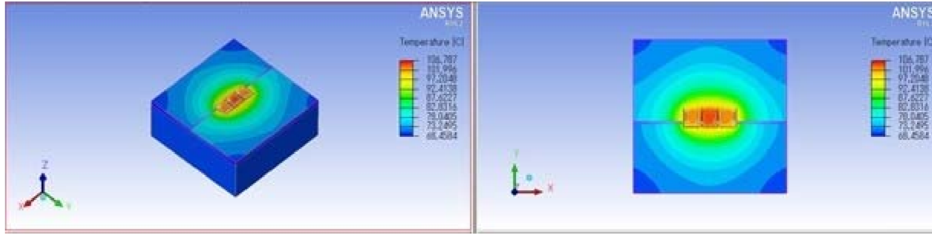
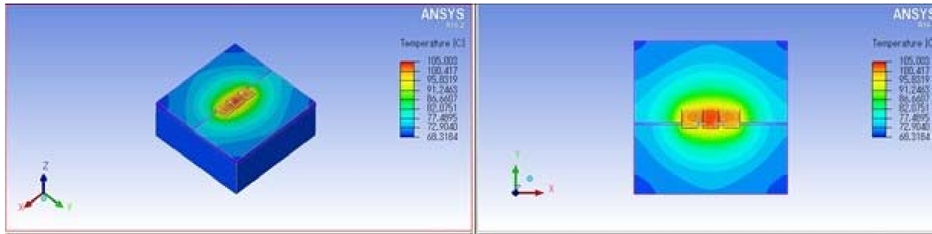
Figure 14 shows temperature distributions across thermal interference models with three devices placed at a spacing of 1 to 12 mm. As shown below, at a spacing of 12 mm, the chip temperatures of the three devices became almost equal.

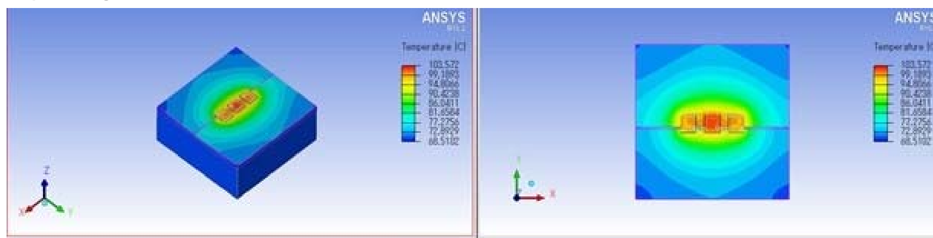
Device spacing: 1 mm



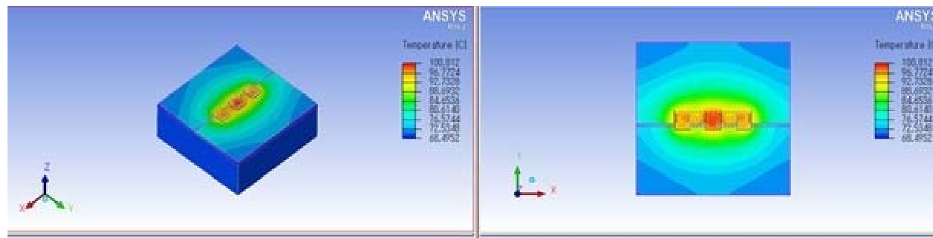
Device spacing: 2 mm



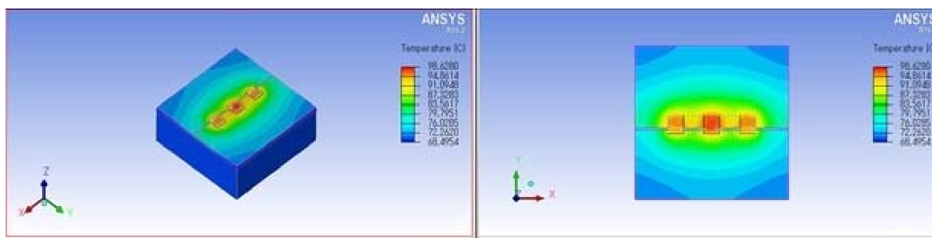
Device spacing: 3 mm



Device spacing: 5 mm



Device spacing: 7 mm



Device spacing: 12 mm

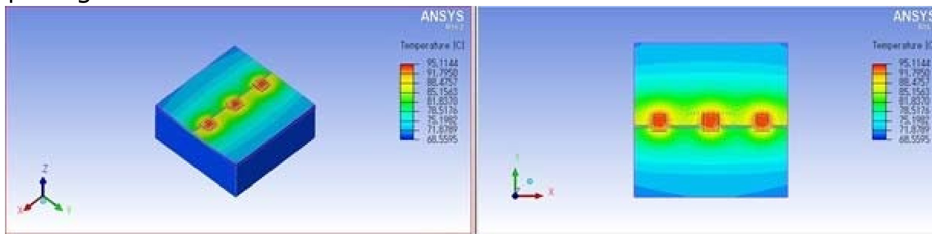


Figure 14 - Temperature Distributions across Thermal Interference Models

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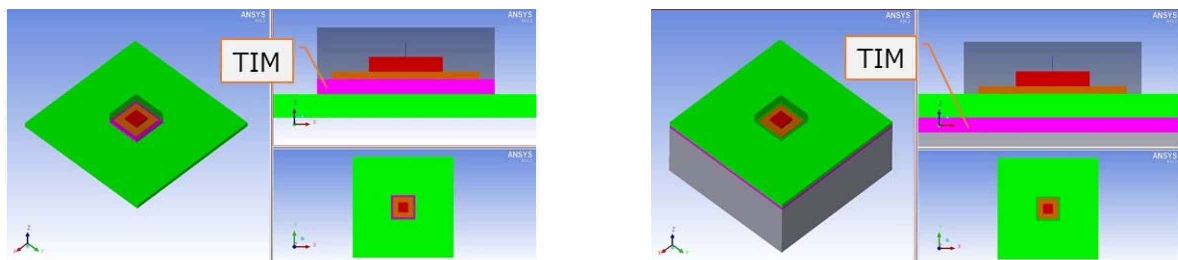
6.8. Effect of a TIM

In order to thermally connect a device or a PCB to a heatsink, thermal grease or thermal sheets are commonly used. These are collectively referred to as thermal interface materials (TIMs). We performed simulation to verify their effectiveness.

In order to simulate the effect of a TIM, we prepared two package models with a simplified structure as shown in Figure 15. A device consists of a chip (5.0×5.0 mm, t = 1 mm), E-pad (10.0×10.0 mm, t = 0.5 mm) and a mold (12.0×12.0 mm, t = 3.5 mm). These models consider heat dissipation only from E-pad. The PCB size is 50×50×1.6 mm, and the device is placed at the center of the PCB. Model A has a TIM between the device and the PCB while Model B has a TIM between the PCB and a heatsink. Model A does not have a heatsink.

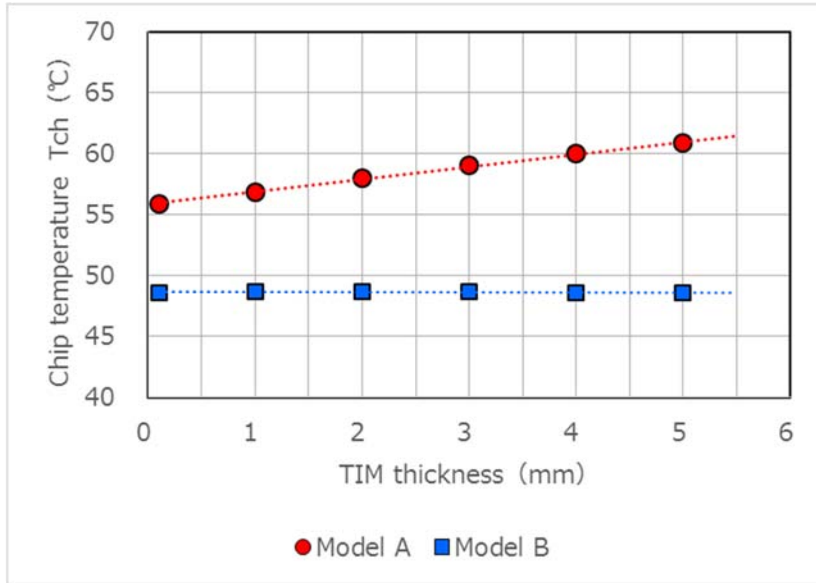
Figure 16 compares the results of simulations of chip temperatures using these models. In Model A, the chip temperature varied with the TIM thickness. The thicker the TIM, the higher the chip temperature became. This indicates that there is a strong positive correlation between the TIM thickness and the chip temperature. In contrast, in Model B, the chip temperature remained almost constant irrespective of the TIM thickness.

These models differ in the area through which heat passes. The TIM area in Model A is equal to the bottom area of the device whereas the TIM area in Model B is equal to the PCB area (see Figure 17). Figure 17 shows how to calculate the thermal resistance of the TIM, considering these areas. Table 2 gives the results of calculation. In Model A, the thicker the TIM, the higher the thermal resistance. However, in Model B, the thermal resistance of the TIM does not increase significantly with the TIM thickness. It is considered that the difference in thermal resistance led to the chip temperature difference between the two TIM models. It is therefore necessary to consider the thickness of a TIM when it is used on a small area.



Model A: TIM Inserted Between Device and PCB   Model B: TIM Inserted Between PCB and Heatsink

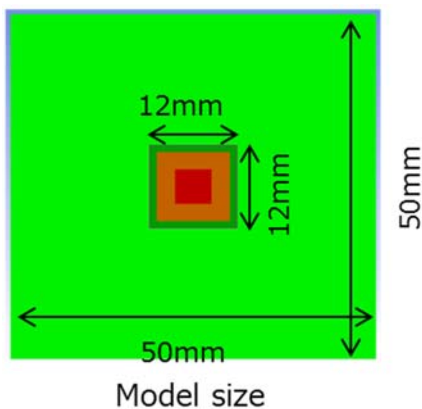
Figure 15 - Device Models for TIM Simulation



TIM thickness (mm)	Chip temperature (℃)	
	Model A	Model B
0.1	55.92	48.58
1.0	56.87	48.69
2.0	58.01	48.67
3.0	59.04	48.65
4.0	60.00	48.63
5.0	60.90	48.61

Figure 16 - TIM Simulation

Table 2 - Thermal Resistance vs. TIM Thickness



Model size

TIM thickness (mm)	Thermal resistance Rth_{TIM} (℃/W)	
	Model A	Model B
0.1	0.21	0.01
1.0	2.10	0.12
2.0	4.21	0.24
3.0	6.31	0.36
4.0	8.42	0.48
5.0	10.52	0.61

Thermal resistance of TIM: $Rth = (1/\lambda) \times (L/A)$

λ: Thermal conductivity of TIM (3.3 W/m·K)

L: TIM thickness, A: TIM area

Figure 17 - TIM Area and Thermal Resistance

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