Toshiba CDMOS Integrated Circuit Silicon Monolithic

T C 7 7 1 6 F T G

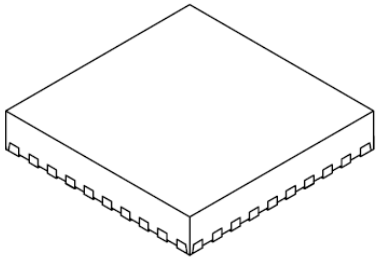
Residential and Commercial Renewable Energy System (up to 1000 V AC or 1500 V DC) Voltage Booster Controller

Outline

TC7716FTG is a DC booster control IC for solar cell power conditioners. The solar panel voltage input pin, 12-bit AD converter, detection circuits, 3 I/O pins for booster and full-bridge control, and UART I/F are built in the IC.

Features

- Process: CD-0.13
- Power supply voltage (VDD): 7.2 V to 14.0 V
- Startup voltage: 7.0 V
- Built in 12bit AD converter (ADC)
- UART I/F
- H-SW soft start
- Voltage booster converter + H-SW controller or full-bridge LLC controller
- Output pulse Duty
  For voltage booster controller: External input
  For H-SW controller: 50%
  For full bridge LLC controller: External input
- Switching Pulse of voltage booster converter: External input
- Switching frequency of H-SW (4-values changeable)
  :50.000 kHz
  :59.524 kHz
  :69.444 kHz
  :80.645 kHz
- Built in protection functions
  Over current protection (OCP)
  Output over voltage protection (OVP, timer latch type)
  Under voltage lock out (UVLO)
  Thermal shutdown (TSD)
- Package QFN 32 (5.0 mm × 5.0 mm, 0.5 mm Pitch)



P-VQFN32-0505-0.50-002

Weight: 70 mg (typ.)

This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

Pin assignment (Top View)

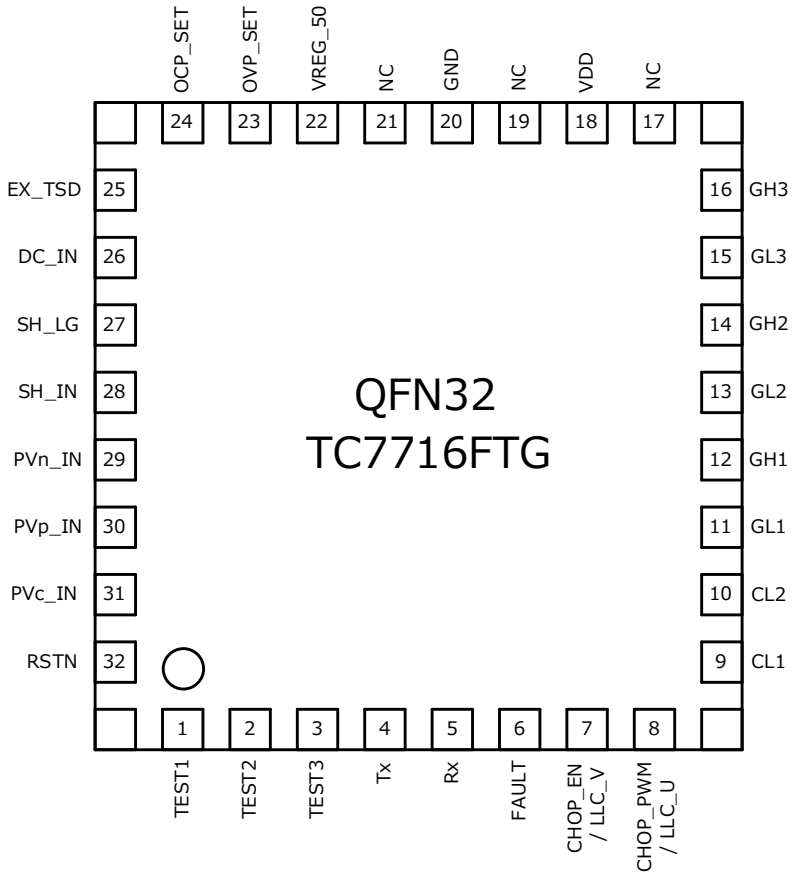


Figure-1

Pin function (1)

Table-1(1)

Pin No.	Pin name	Descriptions
1	TEST1	Test pin for IC shipment. Connect to GND pin (20pin) in normal operation.
2	TEST2	
3	TEST3	
4	Tx	It transmits serial data from UART (Note 1) module in the IC. (Refer to “UART transmitting protocol” in details.)
5	Rx	It receives serial data to UART (Note 1) module in the IC. (Refer to “UART receiving protocol” in details.)
6	FAULT	Monitor pin of protection circuits detection In normal operation, this pin outputs “H” (= 5.0 V). And it outputs “L” (= 0 V) when any circuit of OVP, OCP, or TSD operates.
7	CHOP_EN / LLC_V	It inputs an operation start signal of a half bridge for voltage boosting. It also inputs PFM signal when H-SW operates as a full-bridge LLC converter.
8	CHOP_PWM / LLC_U	It inputs a synchronous rectification PWM signal of a half-bridge for voltage boosting. It also inputs PFM signal when H-SW operates as a full-bridge LLC converter.
9	CL1	It connects to crystal oscillator which generates necessary clocks in the IC. Oscillator of 10 MHz is constructed by connecting the crystal oscillator between CL1 pin and CL2 pin. Oscillator of 10 MHz is used as the sampling clocks of 12-bit ADC. And it is also used as a switching signal generator for PWM controller of H-SW.
10	CL2	
11	GL1 (Note 2)	It outputs PWM signal to FET gate driver IC which configures the right Low side of H-SW.
12	GH1 (Note 2)	It outputs PWM signal to FET gate driver IC which configures the right High side of H-SW.
13	GL2 (Note 2)	It outputs PWM signal to FET gate driver IC which configures the left Low side of H-SW.
14	GH2 (Note 2)	It outputs PWM signal to FET gate driver IC which configures the left High side of H-SW.
15	GL3 (Note 2)	It outputs PWM signal to FET gate driver IC which configures the Low side of the half bridge for voltage boosting.
16	GH3 (Note 2)	It outputs PWM signal to FET gate driver IC which configures the High side of the half bridge for voltage boosting.
17	NC	Non connection pin. It connects to GND in normal use.
18	VDD	Power supply pin for IC. Operating voltage range is 7.2 V (min) to 14.0 V (max). The IC starts at 6.5 V (typ.) and stops operation at 6.0 V (typ.) or less with the UVLO function. VDD voltage (0 V to 8.0 V) should be raised at 200μs or more.
19	NC	Non connection pin. It connects to GND in normal use.
20	GND	Ground (GND) pin for IC.
21	NC	Non connection pin. It connects to GND in normal use.
22	VREG_50	5 V regulator output pin. The 3.0 mA current can be drawn from this pin, with 5.0 V output. The 2.2 μF capacitor is connected between this pin and GND pin (20pin) to stabilize the output voltage. This pin supplies the voltage to OVP_SET pin (23pin), OCP_SET pin (24pin), and the thermistor element for temperature detection.
23	OVP_SET	It configures the threshold value of the OVP (over voltage protection circuit). It is set by dividing the voltage of VREG_50 pin (22pin) (5.0V) with the resistance.
24	OCP_SET	It configures the threshold value of the OCP (over current protection circuit). It is set by dividing the voltage of VREG_50 pin (22pin) (5.0V) with the resistance.

Pin function (2)

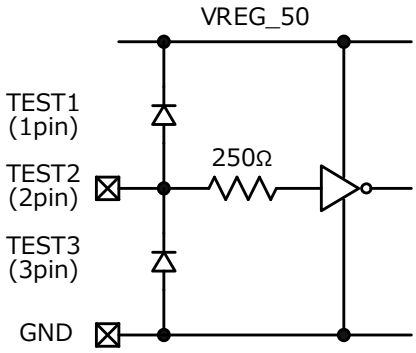
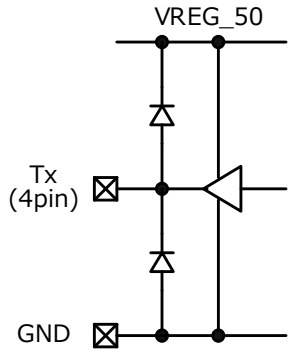
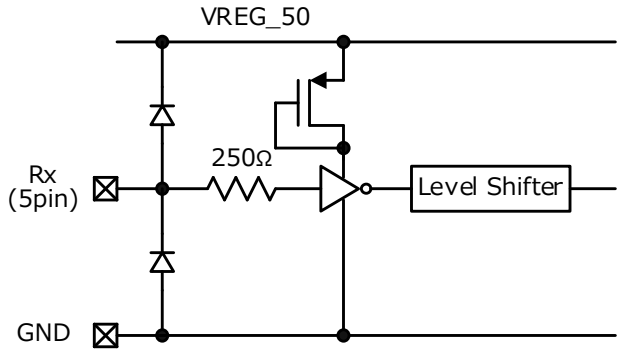
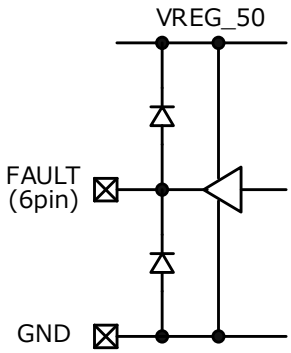
Table-1(2)

Pin No.	Pin name	Description
25	EX_TSD	It connects a thermistor element which monitors temperature around H-SW. The thermistor element is connected between VREG_50 pin (22pin) and this pin. The threshold voltage corresponding to TSD operating temperature is configured by connecting the resistance between this pin and GND pin (20pin).
26	DC_IN	This pin inputs the voltage which is boosted in the half bridge for a booster and is divided with the resistor. When 2.0 μs (typ.) has passed after the voltage of this pin exceeds the threshold value set by OVP_SET pin (23pin), OVP circuit drives and configures the voltage of GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) "L" (= 0 V), and stops switching (Latch). In this time, FAULT pin (6pin) changes outputting "H" to "L" (= 0 V). To release the latch operation, re-starts the IC operation by setting VDD pin (18pin) 5.5 V or less or by setting RSTN pin (32pin) "L" (≤ 1.0 V). After restarting, output of FAULT pin (6pin) returns "L" to "H". (Refer to "Constant number for the threshold setting circuit of over voltage detection and voltage booster input circuit, and conversion equation to ADC input voltage" in details.)
27	SH_LG	It is a reference pin for SH_IN pin (28pin) which detects the current flowing in the voltage booster circuit. This pin should be set the same potential as GND pin (20pin).
28	SH_IN	It detects the current flowing in the voltage booster circuit. This current flowing is input by converting with the resistance. When the voltage between this pin and SH_LG pin (27pin) exceeds the threshold value set by OCP_SET pin (24pin), OCP circuit drives and configures the voltage of GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) "L" (= 0 V), and stops switching. In this time, FAULT pin (6pin) changes outputting "H" (= 5.0 V) to "L". When the current of the voltage booster circuit decreases to the current, which corresponds to the threshold voltage, OCP is released and the IC operation restarts 1.0 ms (typ.) after release. After restarting, FAULT pin (6pin) returns outputting "L" to "H."
29	PVn_IN	These pins detect respectively a short-circuiting to the power supply and GND of the minus and the plus side, from the voltage of the minus side, the plus side, and the middle point of the solar panel. PVn_IN pin inputs the voltage by dividing the voltage between the minus side of the solar panel and GND, with a resistor. PVp_IN pin inputs the voltage by dividing the voltage between the plus side of the solar panel and GND, with a resistor. PVc_IN pin inputs the voltage by dividing the voltage between the middle point of the solar panel and GND, with a resistor. (Refer to 'Constant number for detecting voltage input circuit of PV voltage, PV current, and PV short to the power supply or GND, and conversion equation to ADC input voltage' in details.)
30	PVp_IN	
31	PVc_IN	
32	RSTN	It forcedly resets the internal register externally. When the voltage of this pin is configured 1.0 V or less, the register in the IC is reset forcedly. Then, the reset is released when this pin is configured more than 4.0 V. Do not apply this pin voltage of VREG_50 (5.0 V (typ.)) or more.

Note 1: UART: Universal Asynchronous Receiver Transmitter
Note 2: Pull-down resistance in the IC is not connected to GL1 (11pin), GH1 (12pin), GL2 (13pin), GH2 (14pin), GL3 (15pin), and GH3 (16pin).

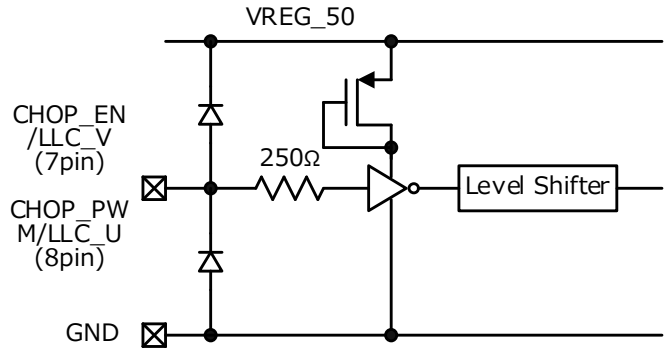
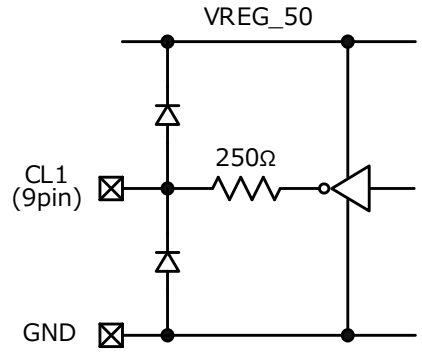
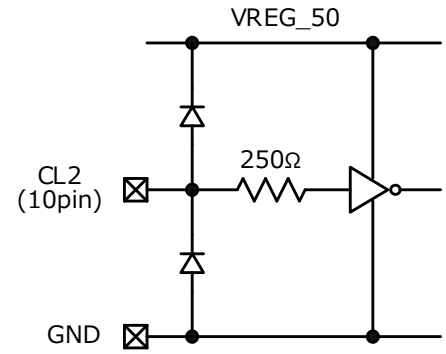
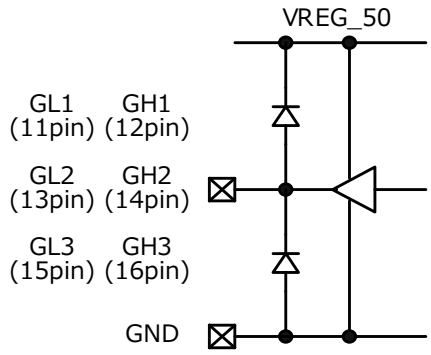
I/O equivalent circuit (1)

Table-2(1)

Pin name	Equivalent circuit
TEST1 TEST2 TEST3	
Tx	
Rx	
FAULT	

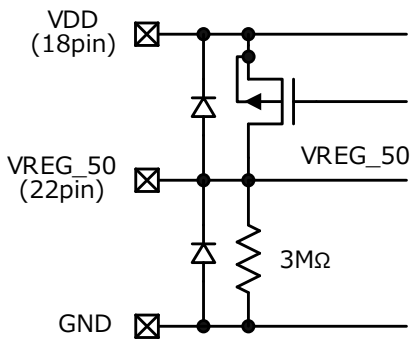
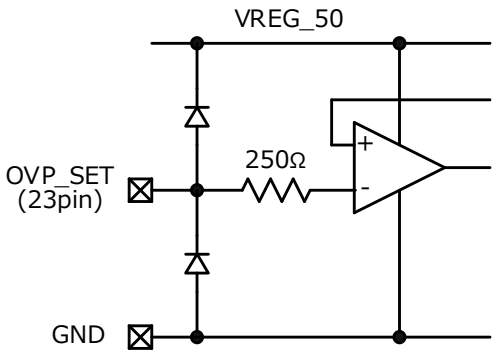
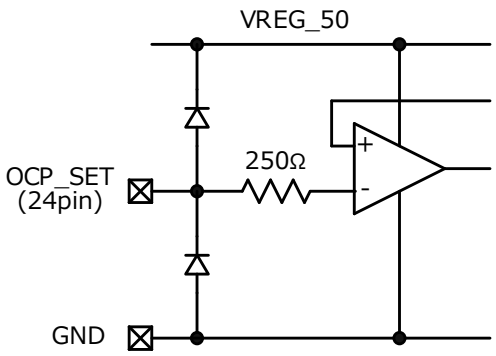
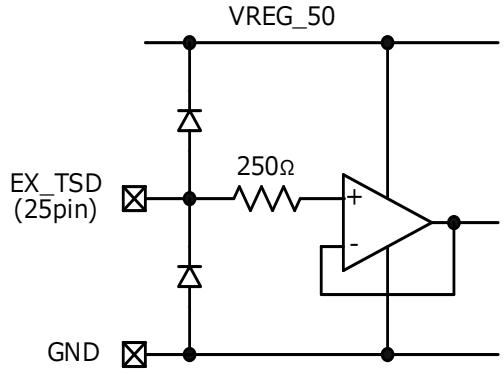
I/O equivalent circuit (2)

Table-2(2)

Pin name	Equivalent circuit
CHOP_EN / LLC_V CHOP_PWM / LLC_U	
CL1	
CL2	
GL1 GH1 GL2 GH2 GL3 GH3	

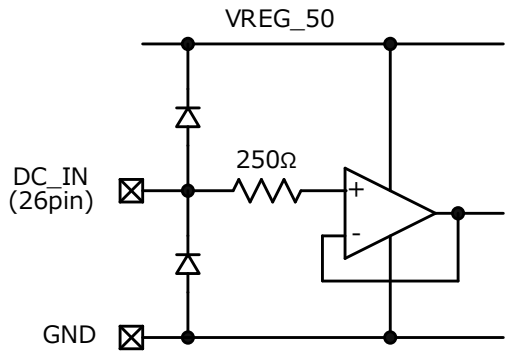
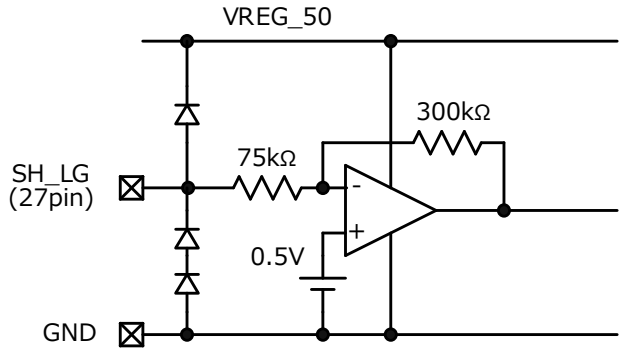
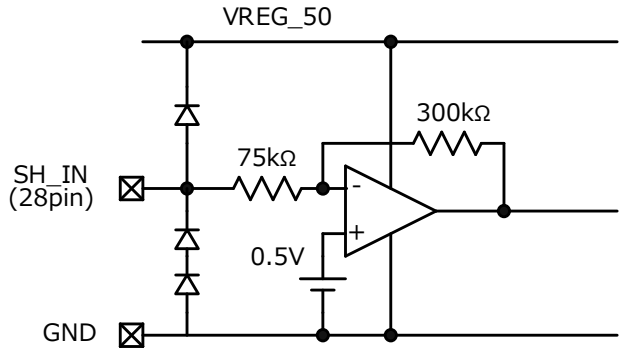
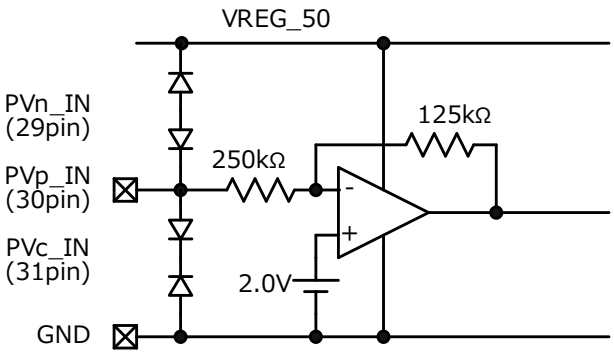
I/O equivalent circuit (3)

Table-2(3)

Pin name	Equivalent circuit
VREG_50	
OVP_SET	
OCP_SET	
EX_TSD	

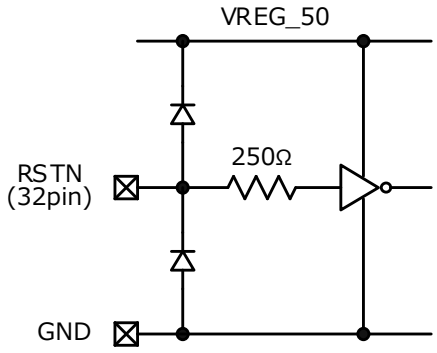
I/O equivalent circuit (4)

Table-2(4)

Pin name	Equivalent circuit
DC_IN	
SH_LG	
SH_IN	
PVn_IN PVp_IN PVc_IN	

I/O equivalent circuit (5)

Table-2(5)

Pin name	Equivalent circuit
RSTN	

Block diagram

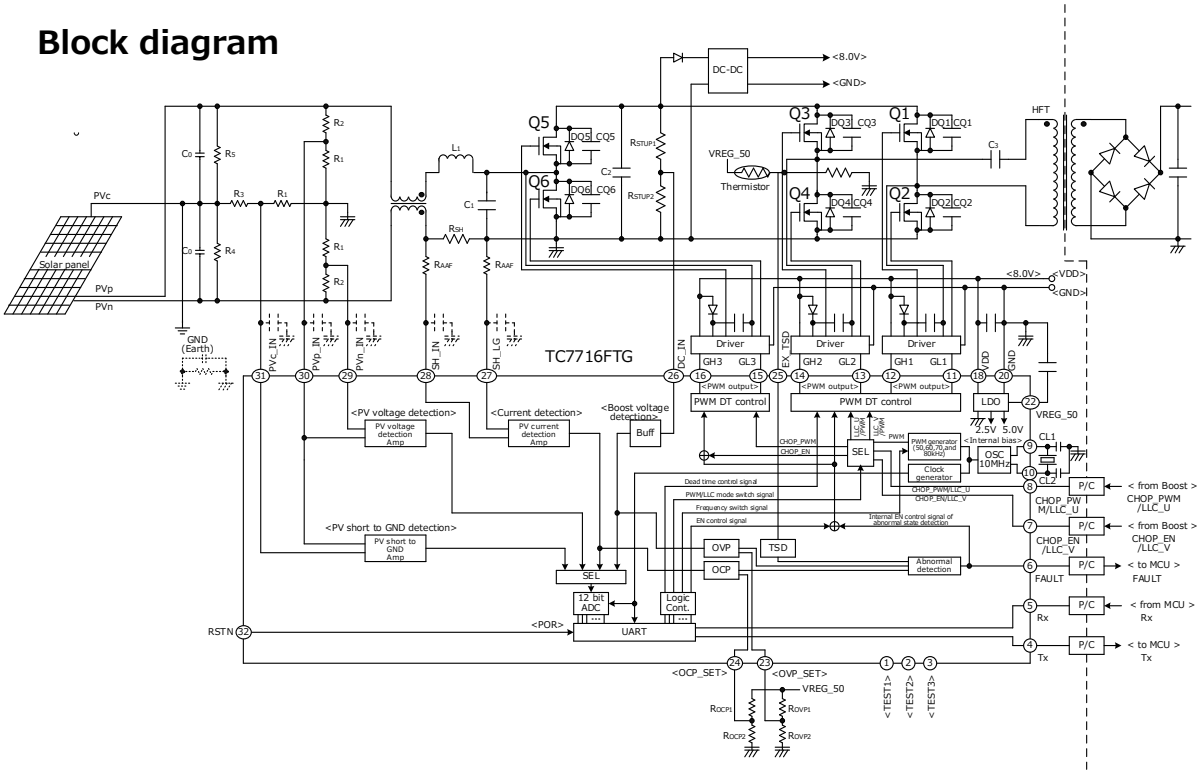


Figure-2

(*) Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Example of application circuit

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Providing these application circuit examples does not grant a license for industrial property rights.

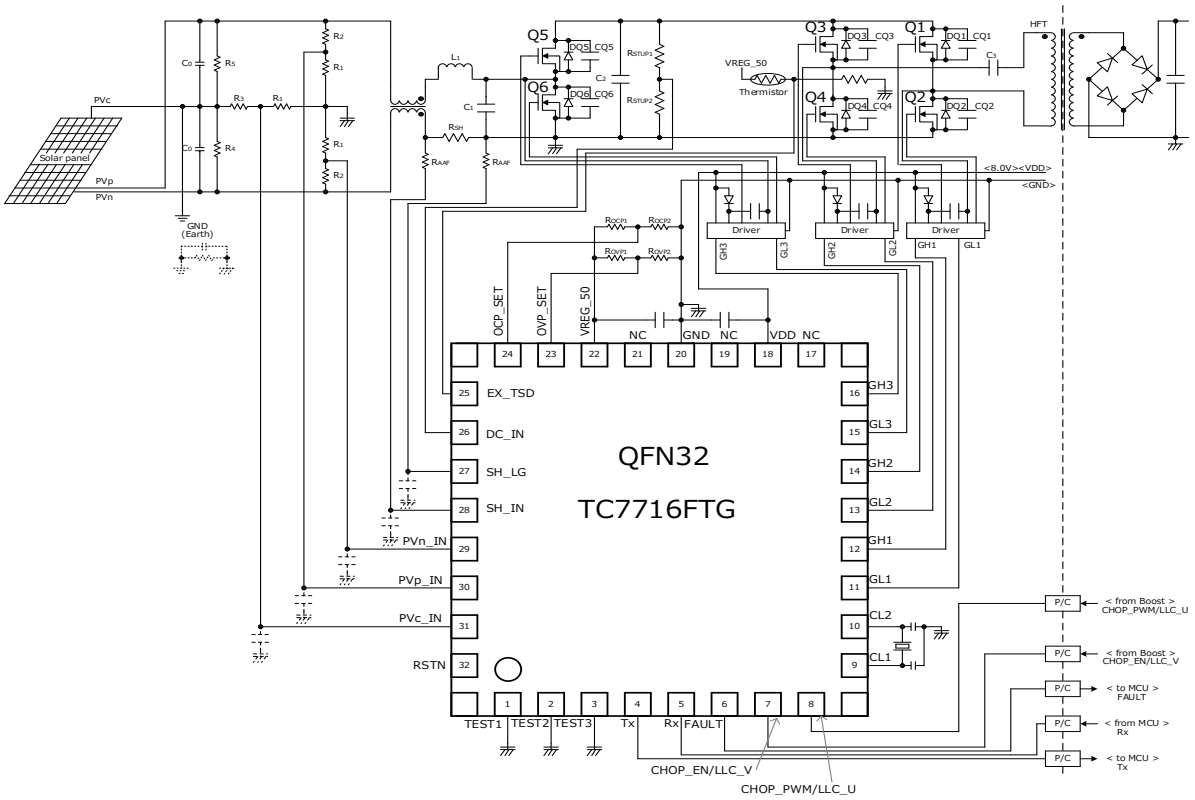


Figure-3

Example of application circuit (Peripheral circuit of photo-coupler)

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Providing these application circuit examples does not grant a license for industrial property rights.

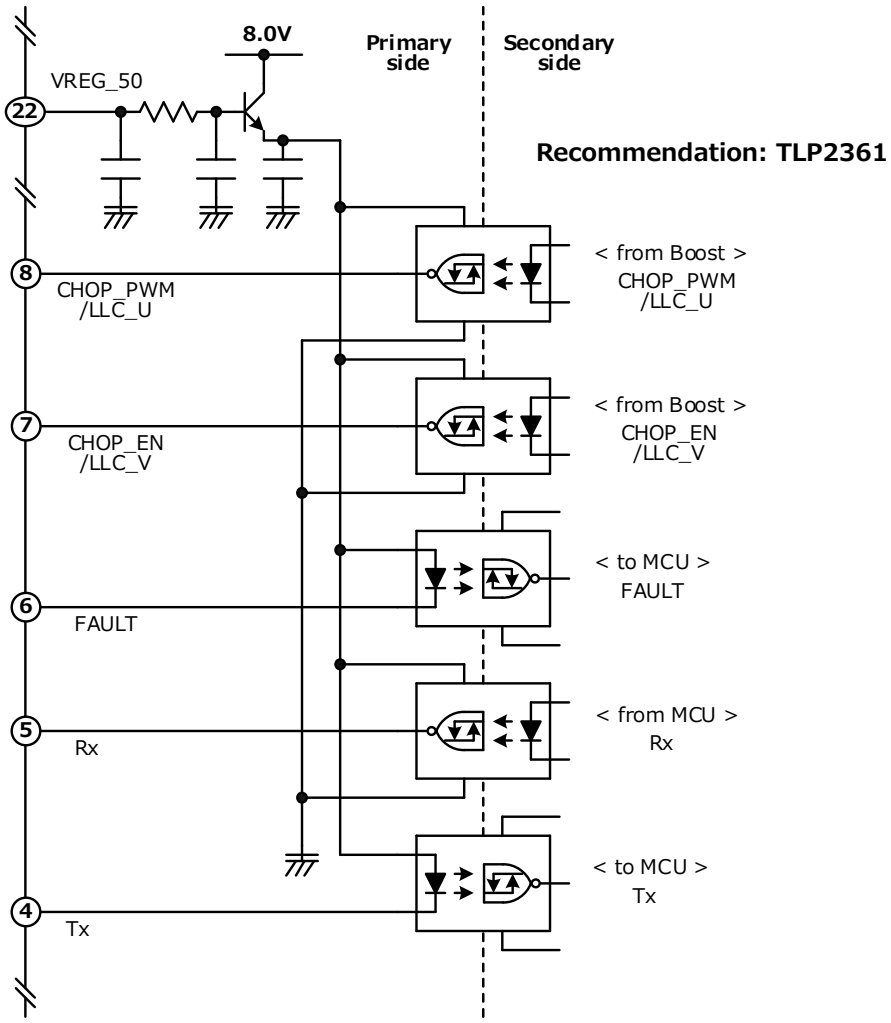


Figure-4

(1) Constant number for detecting voltage input circuit of PV voltage, PV current, and PV short to the power supply or GND, and conversion equation to ADC input voltage

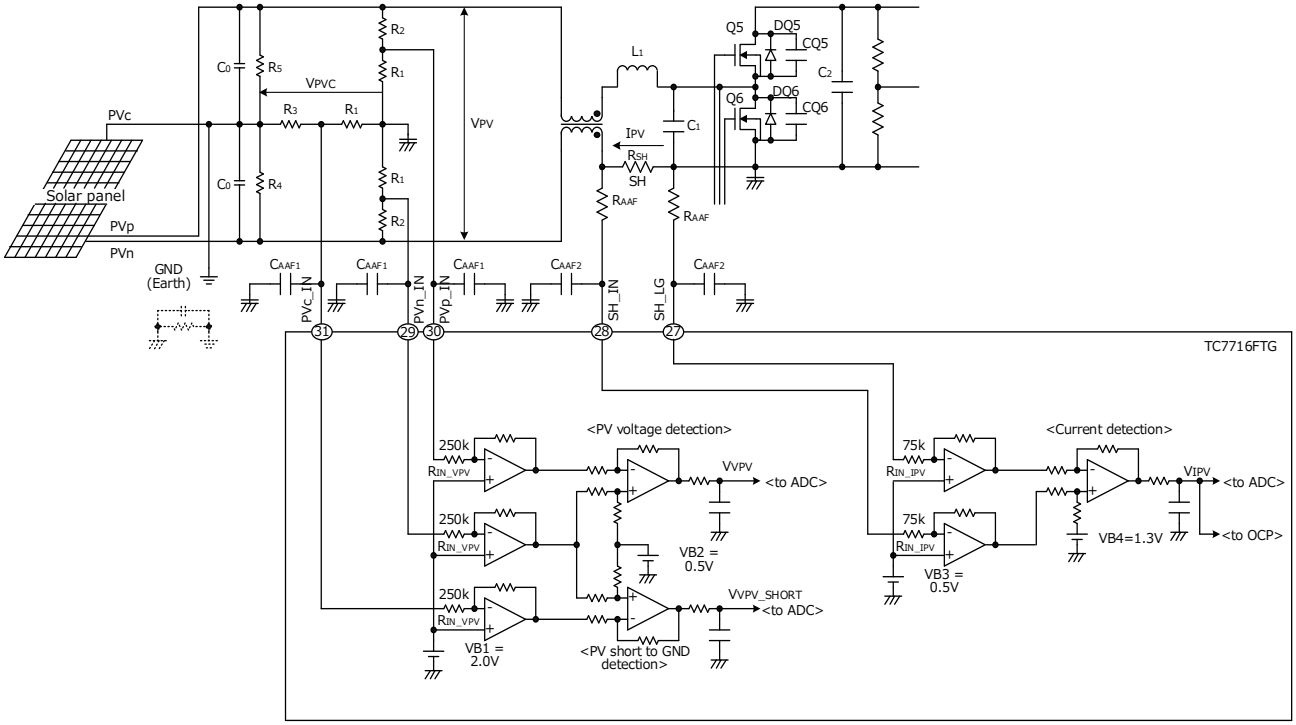


Figure-5

The constant number for detecting voltage input circuit of PV voltage, PV current, and PV short to the power supply or GND, and the equivalent circuit of the ADC input in the IC are shown in the figure 5.
Input voltage for each pin is voltage-converted by the following equation, and is input to the ADC built in the IC.

When R_1 to R_5 (kΩ), R_{SH} (mΩ), R_{AAF} (kΩ), V_{PV} (V), I_{PV} (A), and V_{PVC} (V) are defined, the calculation is performed by the following equations.

1) Detecting voltage of PV voltage: V_{VPV} (V)

$$V_{VPV} = V_{PV} \times \frac{R_1}{R_1 + R_2 + 4R_1 \times R_2 \times 10^{-3}} + 0.5$$

The resistance is set to configure V_{VPV} (V) as follows; 0.452 V ≤ V_{VPV} ≤ 4.548 V (for V_{PV} (V))

2) Detecting voltage of PV current: V_{IPV} (V)

$$V_{IPV} = 1.5 \times R_{SH} \times I_{PV} \times \frac{1}{75 + R_{AAF}} + 1.3$$

The resistance is set to configure V_{IPV} (V) as follows; 0.452 V ≤ V_{IPV} ≤ 4.548 V (for I_{PV} (A))

3) Detecting voltage of PV short to the power supply or GND: V_{VPV_SHORT} (V)

$$V_{VPV\_SHORT} = V_{PVC} \times \frac{R_1}{R_1 + R_2 + 4R_1 \times R_2 \times 10^{-3}} + 0.5$$

The resistance is set to configure V_{VPV_SHORT} (V) as follows; 0.452 V ≤ V_{VPV_SHORT} ≤4.548 V (for V_{PVC} (V))

Then, the middle point voltage of PV (V_{PVC}), K_1 and K_2 are obtained by the following equation.

$$V_{PVC} = V_{PV} \times K_1 \times \frac{R_1 + R_3 + 5\ R_1 \times R_3 \times 10^{-3}}{R_1 + R_3 + 5 \times [R_1 \times R_3 + K_2 \times (R_1 + 200)] \times 10^{-3}}$$

$$K_1 = \frac{R_4}{R_4 + R_5} \qquad K_2 = \frac{R_4 \times R_5}{R_4 + R_5}$$

In the case of $R_4 = R_5$, $K_1 = 0.5$ and $K_2 = 0.5 * R_4$. Therefore the middle point voltage of PV (V_{PVC} (V)) is obtained by the following equation.

$$V_{PVC} = V_{PV} \times 0.5 \times \frac{R_1 + R_3 + 5\ R_1 \times R_3 \times 10^{-3}}{R_1 + R_3 + 5 \times [R_1 \times R_3 + 0.5\ R_4 \times (R_1 + 200)] \times 10^{-3}}$$

Each value of obtained ADC input voltage (V_{VPV} (V), V_{IPV} (V), and V_{VPV_SHORT} (V)) minus 0.452V is converted to 12-bit binary code. And it is transmitted as ADC output from UART Tx pin (4pin).

<Detecting voltage of PV voltage is coded> (V_{VPV}-0.452) -> Converting to 12-bit binary code

<Detecting voltage of PV voltage is coded> (V_{IPV}-0.452) -> Converting to 12-bit binary code

<Detecting voltage of PV short to the power supply or GND is coded > (V_{VPV_SHORT}-0.452)
-> Converting to 12-bit binary code

(2) Constant number for the threshold setting circuit of over voltage detection and voltage booster input circuit, and conversion equation to ADC input voltage

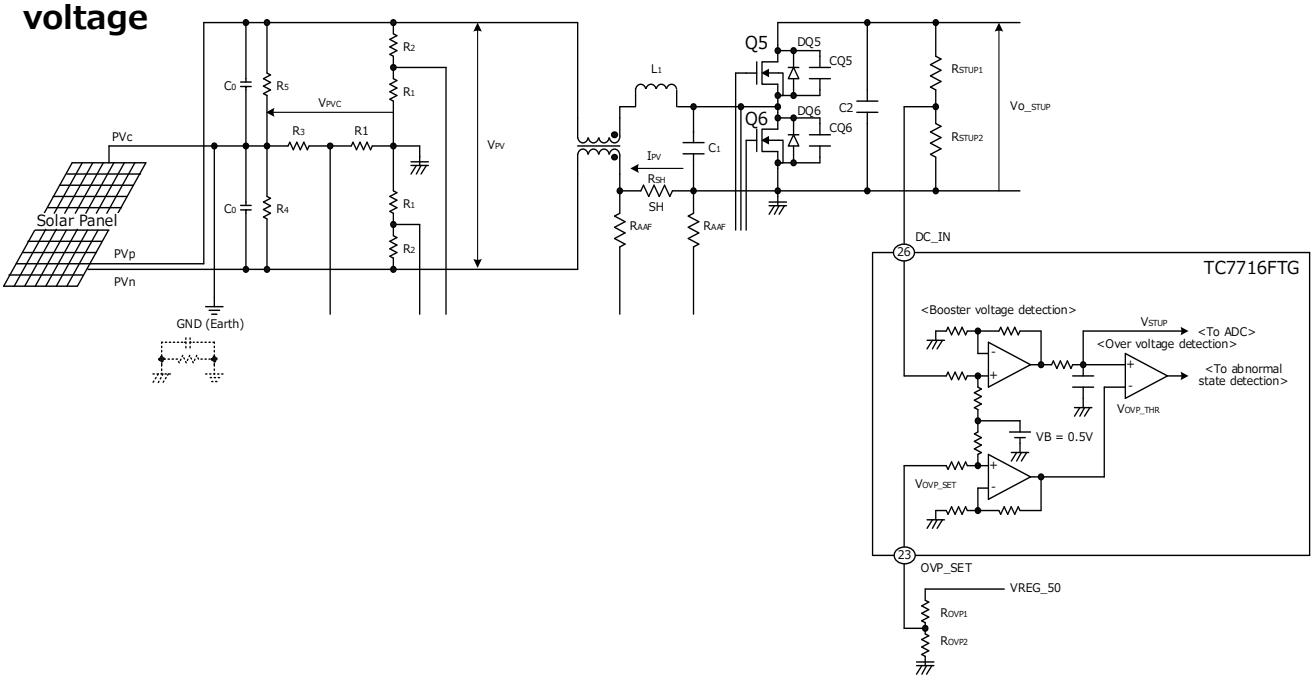


Figure-6

Constant numbers of the threshold setting circuit of over voltage detection and voltage booster input circuit, and the equation circuit to ADC input are shown in the figure 6.

Boosted voltage (V_{O_STUP} (V)) is divided by the dividing resistance ([R_{STUP1} (kΩ)] and [R_{STUP2} (kΩ)]) and is input to DC_IN pin (26pin). The voltage of V_{DC_IN} (V) input by DC_IN pin is voltage-converted to V_{STUP} (V) by the following equation and is supplied to ADC in the IC and OVP detection comparator in each.

$$V_{STUP} = V_{DC\_IN} + 0.5$$

The voltage of V_{DC_IN} (V) is obtained from the following equation.

$$V_{DC\_IN} = V_{O\_STUP} \times \frac{R_{STUP2}}{R_{STUP1} + R_{STUP2}}$$

The resistance is set to configure V_{DC_IN} (V) as follows; $0V \leq V_{DC\_IN} \leq 4.048$ V

The value of voltage-converted V_{STUP} (V) minus 0.452 V is converted to 12-bit binary code. And it is transmitted as ADC output from UART Tx pin (4pin).

<Boosting voltage is coded> (V_{STUP} - 0.452) -> Converting 12-bit binary code

On the other hand, V_{STUP} (V), which is input to OVP detecting comparator, is compared to the threshold value (V_{OVP_THR} (V)) set by OVP_SET pin (23pin). And when the following equation is obtained, the over voltage detecting circuit operates to configure GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) "L" (= 0 V) and stops switching (Latch).

$$V_{STUP} \geq V_{OVP\_THR}$$

The threshold value of V_{OVP_THR} is

$$V_{OVP\_THR} = V_{OVP\_SET} + 0.5$$

Then,

$$V_{DC\_IN} \geq V_{OVP\_SET}$$

OVP threshold setting voltage (V_{OVP_SET} (V)) is obtained by following equation when dividing resistance connected to OVP_SET pin (23pin) is described [R_{OVP1} (kΩ)] and [R_{OVP2} (kΩ)], and the voltage of VREG_50 pin (22pin) is described V_{VREG_50} (= 5.0 V).

$$V_{OVP\_SET} = V_{VREG\_50} \times \frac{R_{OVP2}}{R_{OVP1} + R_{OVP2}} = 5.0 \times \frac{R_{OVP2}}{R_{OVP1} + R_{OVP2}}$$

Therefore, the threshold value of over voltage detection is configured under the condition that satisfies the following equation.

$$V_{DC\_IN} \geq V_{OVP\_SET} = 5.0 \times \frac{R_{OVP2}}{R_{OVP1} + R_{OVP2}}$$

So, the relation of R_{OVP1} and R_{OVP2} is as follows;

$$R_{OVP1} \geq \left(\frac{5.0}{V_{DC\_IN}} - 1 \right) \times R_{OVP2}$$

(3) Constant number setting for threshold setting circuit of over current detection

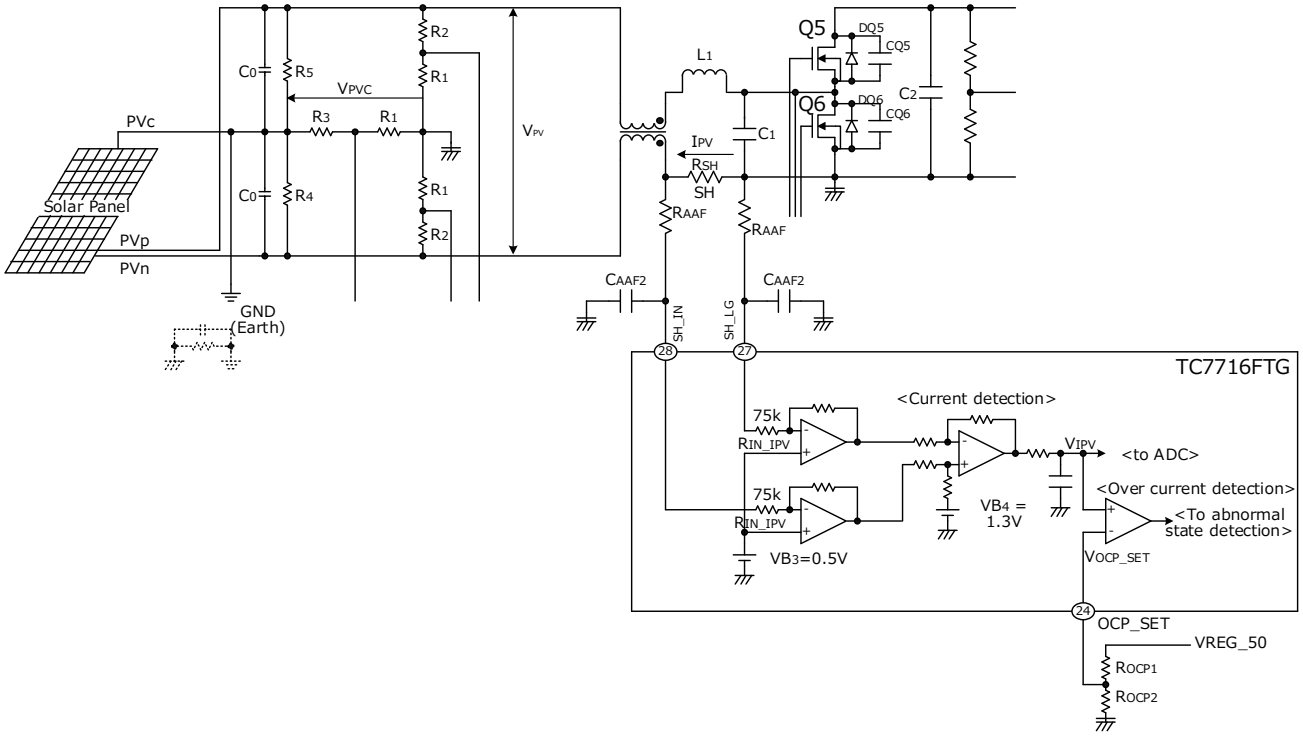


Figure-7

The equivalent circuit for threshold setting circuit of over current detection is shown in Figure-7.

V_{IPV} (V), which is inputted to OCP detecting comparator, is compared to the threshold value (V_{OCP_SET} (V)) set by OCP_SET pin (24pin). And when the following formula is obtained, the over current detection circuit operates to configure GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) "L" (= 0 V) and stops switching.

$$V_{IPV} \geq V_{OCP\_SET}$$

When R_{SH} (mΩ), I_{PV} (A), and R_{AAF} (kΩ) are defined, V_{IPV} is obtained by the following equation.

$$V_{IPV} = 1.5 \times R_{SH} \times I_{PV} \times \frac{1}{75 + R_{AAF}} + 1.3$$

When the voltage between SH_IN pin (28pin) and SH_LG pin (27pin) is defined V_{OCP_IN} (V) (When the current of I_{PV} flows in the direction of the arrow in Figure-7, it is defined V_{OCP_IN} >0). V_{OCP_IN} is obtained by the following equation.

$$V_{OCP\_IN} = \frac{3}{40} \times R_{SH} \times I_{PV} \times \frac{1}{75 + R_{AAF}}$$

$$V_{IPV} = 20 \times V_{OCP\_IN} + 1.3$$

OCP threshold setting voltage (V_{OCP_SET}(V)) is obtained by following equation when dividing resistance connected to OCP_SET pin (24pin) is described [R_{OCP1} (kΩ)] and [R_{OCP2} (kΩ)], and the voltage of VREG_50 pin (22pin) is described V_{VREG_50} (= 5.0 V).

$$V_{OCP\_SET} = V_{VREG\_50} \times \frac{R_{OCP2}}{R_{OCP1} + R_{OCP2}} = 5.0 \times \frac{R_{OCP2}}{R_{OCP1} + R_{OCP2}}$$

Therefore, the threshold value of over current detection is configured under the condition that satisfies the following equation.

(1) In case of focusing on the voltage (V_{OCP_IN} (V)) between SH_IN pin (28pin) and SH_LG pin (27pin),

$$V_{OCP\_IN} \geq \frac{1}{20} \times (V_{OCP\_SET} - 1.3)$$

$$= \frac{1}{20} \times \frac{3.7 \times R_{OCP2} - 1.3 \times R_{OCP1}}{R_{OCP1} + R_{OCP2}}$$

(2) In case of focusing on PV current (I_{PV}(A)),

$$I_{PV} \geq \frac{2}{3} \times \frac{75 + R_{AAF}}{R_{SH}} \times (V_{OCP\_SET} - 1.3)$$

$$= \frac{2}{3} \times \frac{75 + R_{AAF}}{R_{SH}} \times \frac{3.7 \times R_{OCP2} - 1.3 \times R_{OCP1}}{R_{OCP1} + R_{OCP2}}$$

The relation between R_{OCP1} and R_{OCP2} is as follows;

(1) In case of focusing on the voltage (V_{OCP_IN} (V)) between SH_IN pin (28pin) and SH_LG pin (27pin)

$$R_{OCP1} \geq \frac{0.185 - V_{OCP\_IN}}{0.065 + V_{OCP\_IN}} \times R_{OCP2}$$

(2) In case of focusing on PV current (I_{PV}(A)),

$$R_{OCP1} \geq \frac{3.7 \times K - I_{PV}}{1.3 \times K + I_{PV}} \times R_{OCP2}$$

$$*K = \frac{2}{3} \times \frac{75 + R_{AAF}}{R_{SH}}$$

Appendix

Example of calculation

(1) Constant number for detecting voltage input circuit of PV voltage, PV current, and PV short to the power supply or GND, and conversion equation to ADC input voltage

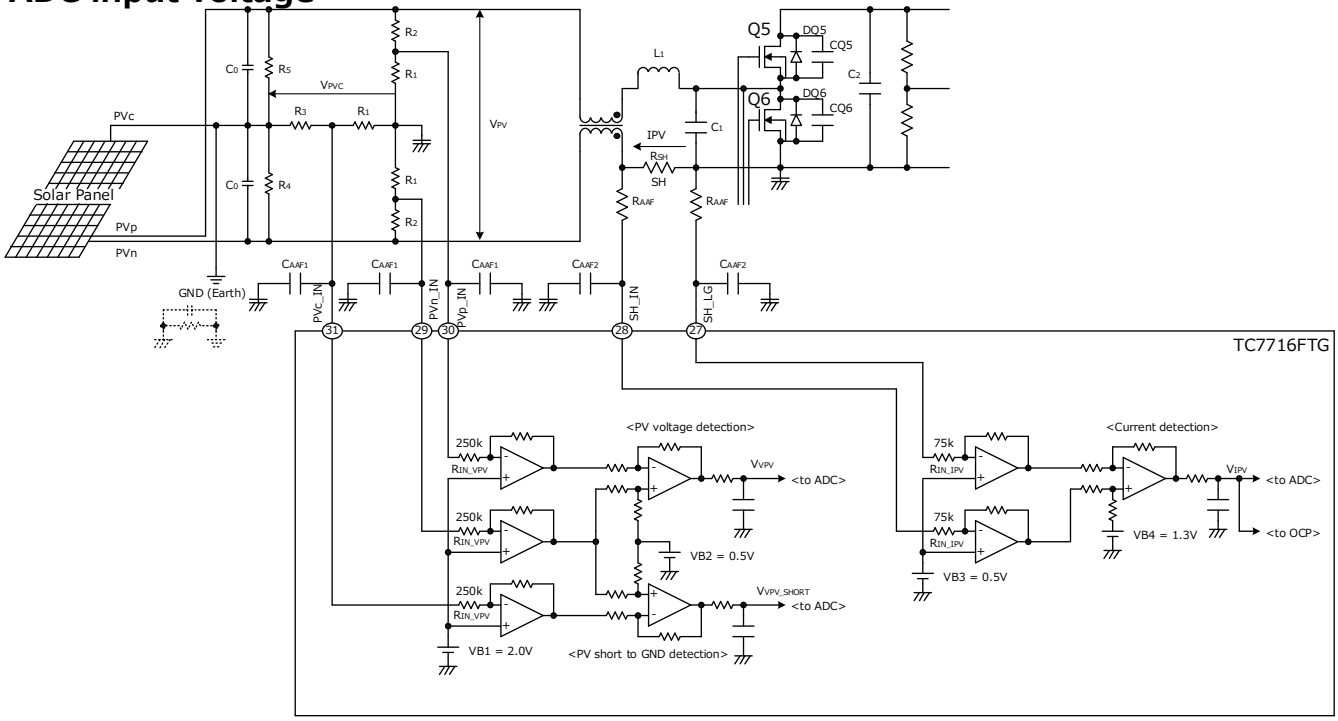


Figure-5 (Re-posting)

When R_1=27 kΩ, R_2=540 kΩ, R_3=540 kΩ, R_4=200 kΩ, R_5=200 kΩ, R_{SH}=12 mΩ, and R_{AAF}=1 kΩ are defined,

1) Detecting voltage of PV voltage: ADC input voltage V_{VPV} (V) is obtained by the following equation.

$$V_{VPV} = V_{PV} \times \frac{R_1}{R_1 + R_2 + 4R_1 \times R_2 \times 10^{-3}} + 0.5$$
$$= \frac{25}{579} \times V_{PV} + 0.5$$

<Detecting voltage of PV voltage is coded>

$$V_{VPV} - 0.452 = \left(\frac{25}{579} \times V_{PV} + 0.5 \right) - 0.452$$
$$= \frac{25}{579} \times V_{PV} + 0.048$$

This value is converted to 12-bit binary code. (Refer to Table-3.)

Table-3

PV voltage (V) (V_{PV})	ADC input voltage (V) (V_{VPV})	ADC output code (Hex)
0.00	0.500	030
22.0	1.450	3E6
27.5	1.687	4D3
52.5	2.767	90B
70.0	3.522	BFE
84.0	4.127	E5B
92.4	4.490	FC6

2) Detecting voltage of PV current: ADC input voltage V_{IPV} (V) is obtained by the following equation.

$$V_{IPV} = 1.5 \times R_{SH} \times I_{PV} \times \frac{1}{75 + R_{AAF}} + 1.3$$
$$= \frac{9}{38} \times I_{PV} + 1.3$$

<Detecting voltage of PV current is coded>

$$V_{IPV} - 0.452 = \left(\frac{9}{38} \times I_{PV} + 1.3 \right) - 0.452$$
$$= \frac{9}{38} \times I_{PV} + 0.848$$

This value is converted to 12-bit binary code. (Refer to Table-4.)

Table-4

PV current (A) (I_{PV})	ADC input voltage (V) (V_{IPV})	ADC output code (Hex)
0.00	1.300	350
7.50	3.076	A40
8.25	3.254	AF2
11.25	3.964	DB8
13.12	4.407	F73

3) Detecting voltage of PV short to the power supply or GND: ADC input voltage V_{VPV_SHORT}(V) is obtained by the following equation.

$$V_{VPV\_SHORT} = V_{PVC} \times \frac{R_1}{R_1 + R_2 + 4R_1 \times R_2 \times 10^{-3}} + 0.5$$

$$= \frac{25}{579} \times V_{PVC} + 0.5$$

Although the middle point voltage of PV (V_{PVC}) is obtained by the following equation: R_4=R_5=200 kΩ

$$V_{PVC} = V_{PV} \times 0.5 \times \frac{R_1 + R_3 + 5R_1 \times R_3 \times 10^{-3}}{R_1 + R_3 + 5 \times [R_1 \times R_3 + 0.5R_4 \times (R_1 + 200)] \times 10^{-3}}$$

$$= \frac{6399}{15068} \times V_{PV}$$

ADC input voltage is obtained by the following equation.

$$V_{VPV\_SHORT} = \frac{25}{579} \times \left(\frac{6399}{15068} \times V_{PV} \right) + 0.5$$

<Detecting voltage of PV short to the power supply and GND is coded>

$$V_{VPV\_SHORT} - 0.452 = \left(\frac{25}{579} \times \left(\frac{6399}{15068} \times V_{PV} \right) + 0.5 \right) - 0.452$$

$$= \frac{25}{579} \times \left(\frac{6399}{15068} \times V_{PV} \right) + 0.048$$

This value is converted to 12-bit binary code. (Refer to Table-5.)

Table-5

PV voltage (V) (V_{PV})	ADC input voltage (V) (V_{VPV_SHORT})	ADC output code (Hex)
0.00	0.500	030
22.0	0.903	1C3
27.5	1.004	228
52.5	1.463	3F3
70.0	1.784	534
84.0	2.040	634
92.4	2.194	6CE

(2) Constant number for the threshold setting circuit of over voltage detection and voltage booster input circuit, and conversion equation to ADC input voltage

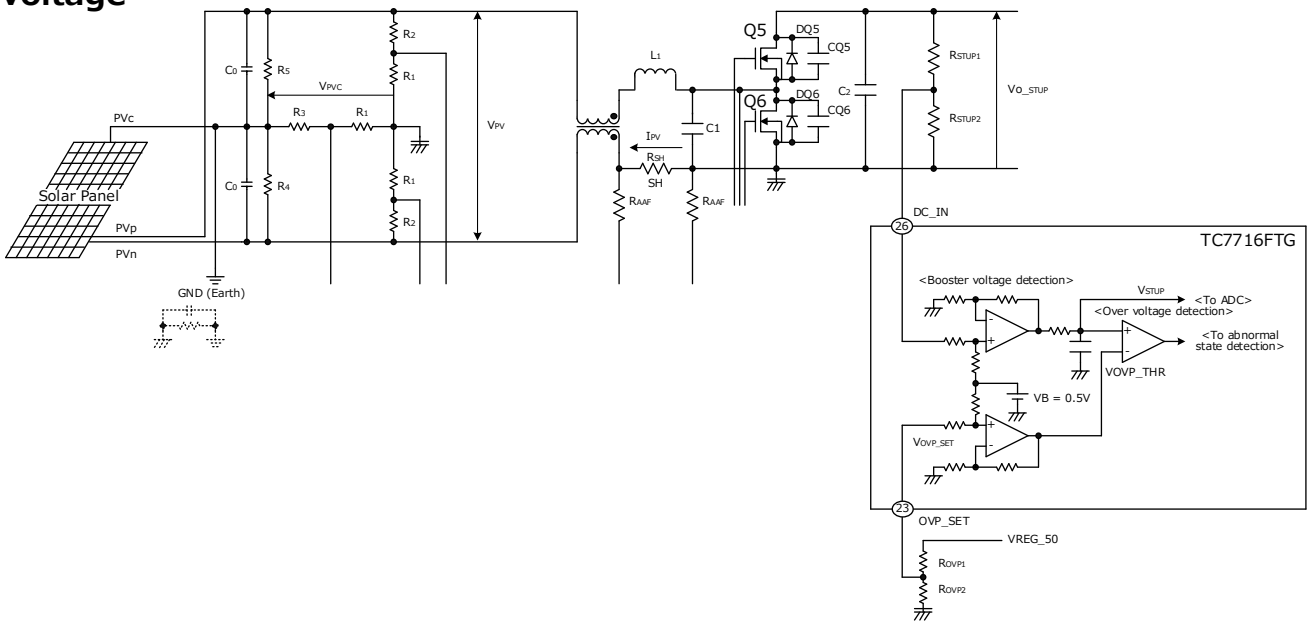


Figure-6 (Re-posting)

1) Detecting voltage of boosting voltage: ADC input voltage V_{STUP} (V) is obtained by

$$V_{STUP} = V_{DC\_IN} + 0.5$$

When R_{STUP1} = 470 kΩ, and R_{STUP2} = 27 kΩ are defined,

$$V_{DC\_IN} = V_{O\_STUP} \times \frac{R_{STUP2}}{R_{STUP1} + R_{STUP2}} = \frac{27}{497} \times V_{O\_STUP}$$

Therefore, ADC input voltage V_{STUP} (V) is obtained by the following equation.

$$V_{STUP} = \left(\frac{27}{497} \times V_{O\_STUP} \right) + 0.5$$

<Voltage boosting is coded>

$$V_{STUP} - 0.452 = \left(\frac{27}{497} \times V_{O\_STUP} + 0.5 \right) - 0.452$$

$$= \frac{27}{497} \times V_{O\_STUP} + 0.048$$

This value is converted to 12-bit binary code. (Refer to Table-6.)

Table-6

Boosting voltage (V) (V_{O_STUP})	ADC input voltage (V) (V_{STUP})	ADC output code (Hex)
0.00	0.500	030
22.0	1.695	4DB
27.5	1.994	606
53.0	3.379	B6F
60.0	3.760	CEC
67.0	4.140	F68
72.0	4.411	F77

2) Threshold voltage setting of over voltage detection

When 120% (= 72 V) of boosting voltage (V_{O_STUP} (V) = 60 V) is regarded the over voltage, the voltage of DC_IN pin (26pin) (V_{DC_IN} (V)) is obtained by the following equation.

$$V_{DC\_IN} = V_{O\_STUP} \times \frac{R_{STUP2}}{R_{STUP1} + R_{STUP2}} = 72 \times \frac{27}{497} \fallingdotseq 3.911$$

*R_{STUP1} = 470 kΩ, R_{STUP2} = 27 kΩ

When R_{OVP2}=47 kΩ is defined, the equation is as follows;

$$R_{OVP1} \geq \left(\frac{5.0}{V_{DC\_IN}} - 1 \right) \times R_{OVP2} \fallingdotseq 0.2783 \times R_{OVP2}$$

The threshold value can be configured by considering $R_{OVP1} \approx$ 13 kΩ from above equation.

(3) Constant number setting for threshold setting circuit of over current detection

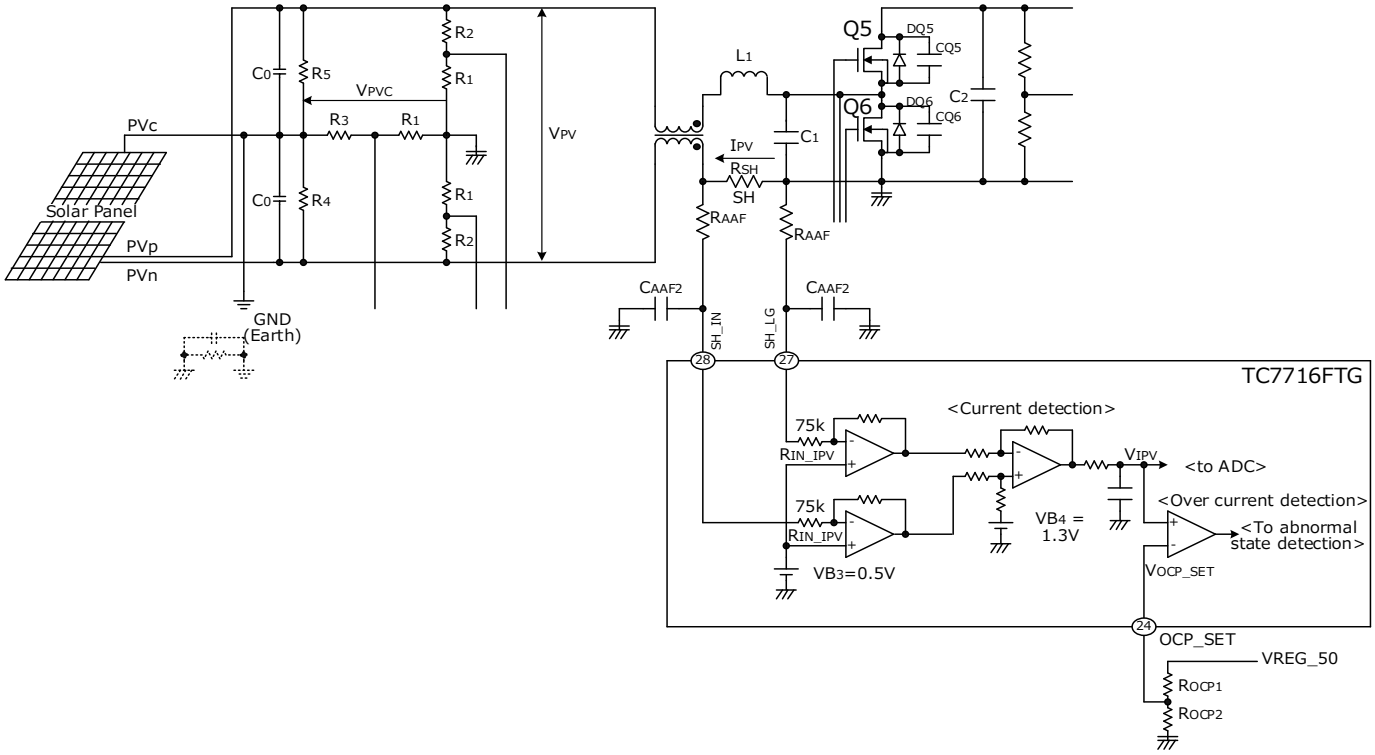


Figure-7 (Re-posting)

When 150% (= 11.25 A) or more of PV current (I_{PV} (A)) 7.5 A is regarded the over current, the voltage (V_{OCP_IN} (V)) between SH_IN pin (28pin) and SH_LG pin (27pin) is obtained by the following equation.

$$V_{OCP\_IN} = \frac{3}{40} \times R_{SH} \times I_{PV} \times \frac{1}{75 + R_{AAF}}$$

$$= \frac{9}{760} \times 11.25$$

*R_{SH}=12 mΩ, R_{AAF}=1 kΩ

When R_{OCP2}=68 kΩ is defined,

$$R_{OCP1} \geq \frac{0.185 - V_{OCP\_IN}}{0.065 + V_{OCP\_IN}} \times R_{OCP2} \fallingdotseq 0.2612 \times R_{OCP2}$$

The threshold value can be configured as R_{OCP1} ≈ 18 kΩ from above equation.

Function description

(1) UVLO (under voltage lockout) function

When the voltage of VDD pin (18pin) becomes 6.5 V (typ.) or more, UVLO is released and the IC operation starts. When the voltage of VDD falls 6.0 V (typ.) or less in the normal operation, UVLO operates and the IC operation stops. However, when it returns to 6.5 V (typ.) or more, the IC operation starts again.

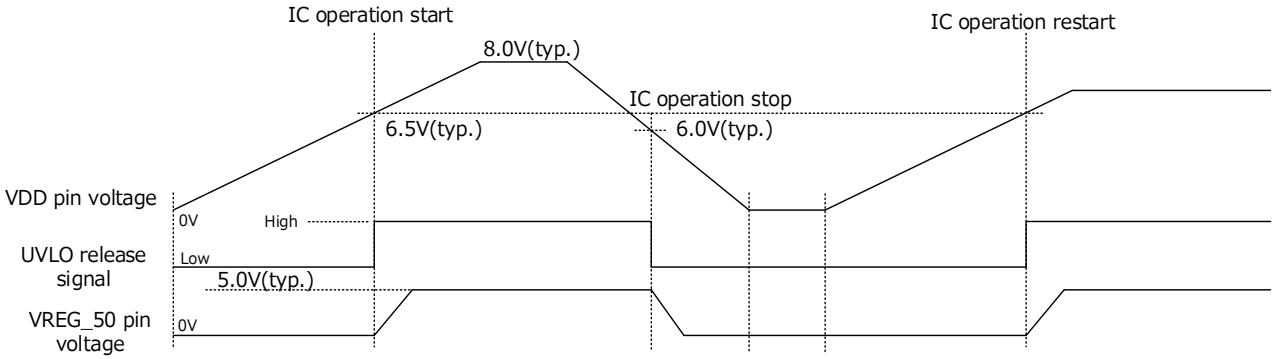


Figure-8

(2) Soft start function

Switching pulse of H-SW starts when Duty is 0%. After 30 s passes, the duty becomes 25% by the soft start function. After the information that the duty becomes 25% is sent to microcomputer through UART, the control microcomputer transmits the command (D2 = [1] in the receiving protocol Byte_1) that the duty should be extended to 50% through UART. Then, the duty increases from 25% to 50% 30 s after the command is received by the soft start function. (As for detailed communication flow with the control microcomputer, refer to Figure-17.)

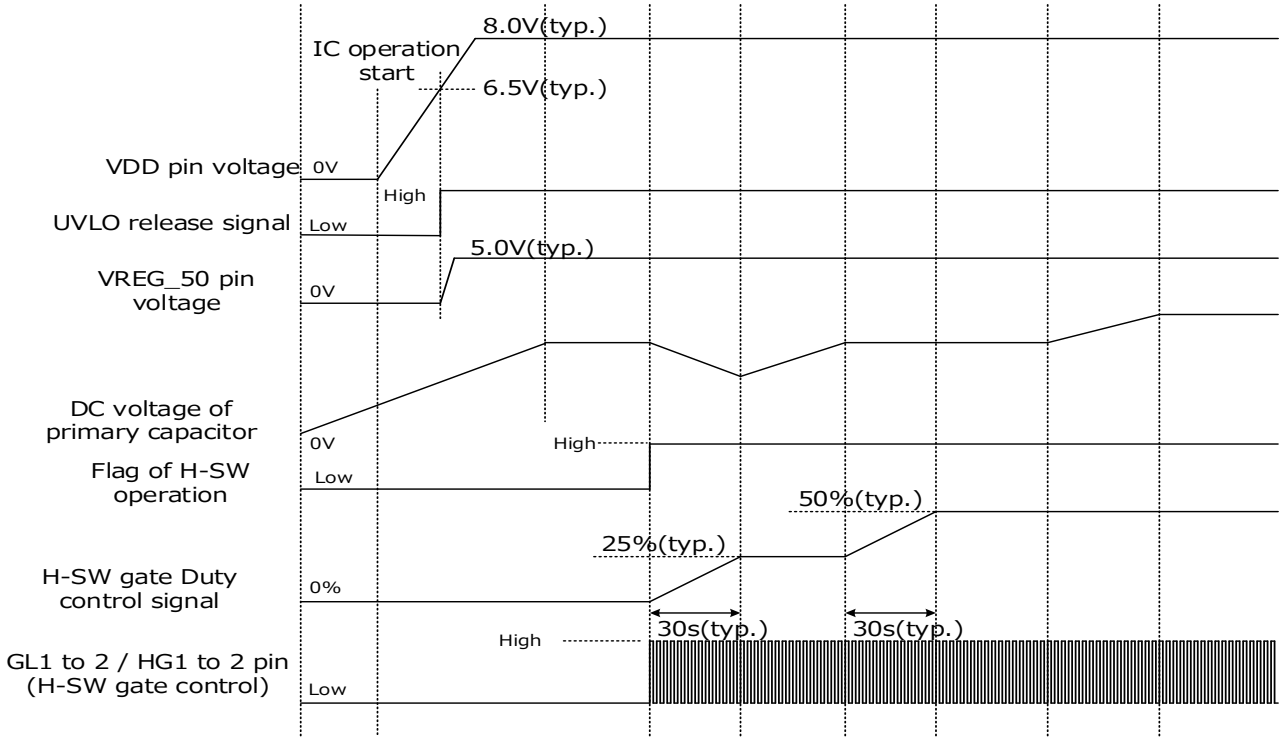


Figure-9

(3) Over voltage protection (OVP) function (operation sequence-1)

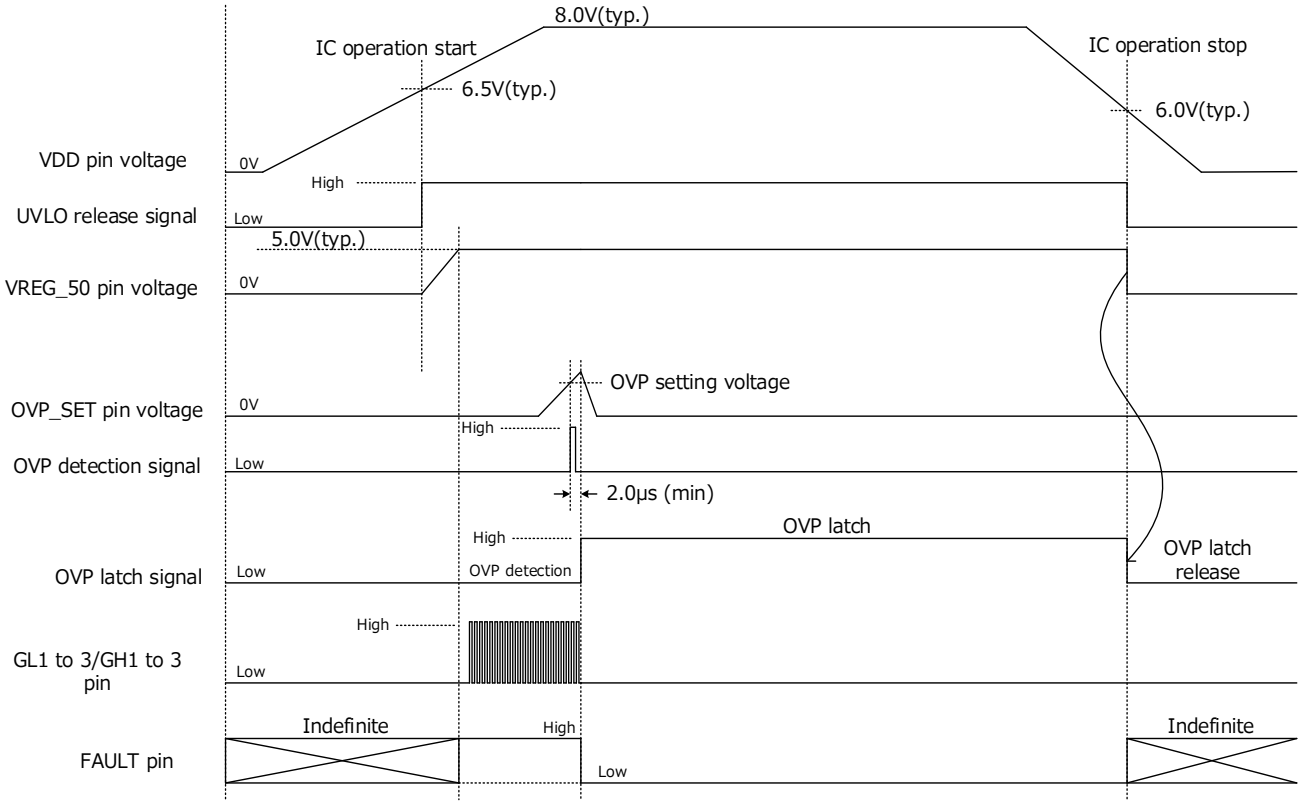


Figure-10

OVP operates under the condition that the boosting voltage exceeds the over voltage detection threshold for 2 μs or more because the temporary blackout or open state are generated at the system connection side (secondary side) in the normal operation after completing IC power on. GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) are configured “L” (= 0V) and switching operation is stopped (Latch).

(4) Over voltage protection (OVP) function (operation sequence-2)

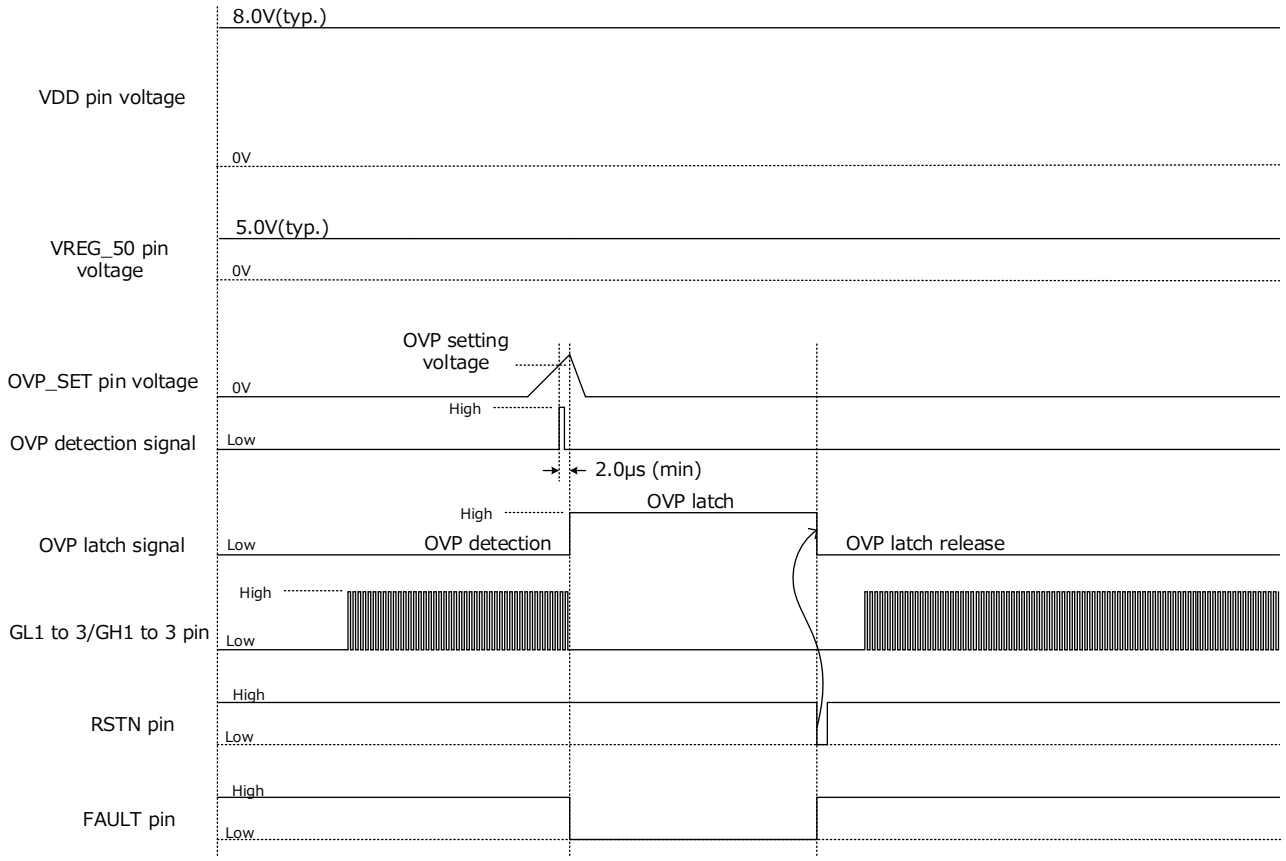


Figure-11

When OVP operates to configure GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) “L” (= 0 V) and stops switching (latch), latch is released and the operation starts again by configuring RSTN pin (32pin) “L” (≤ 1.0 V).
After the IC operation starts again, FAULT pin (6pin) outputs “L” to “H” again.

(5) Over current protection (OCP) function

It limits the current flowing in the voltage booster circuit.
When the voltage between SH_IN pin (28pin) and SH_LG pin (27pin) exceeds the threshold value set by OCP_SET pin (24pin), OCP circuit operates to configure GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) "L" (= 0 V) and stops switching.
In this time, the voltage of FAULT pin (6pin) becomes "H" (= 5.0 V pull-up) to "L" and it informs the microcomputer for system control that the OCP operates.
1.0 ms (typ.) passes after the over current state is released, OCP is released and the IC re-starts operation without soft start. When it re-starts, FAULT pin (6pin) outputs "L" to "H".
When system failure is not cleared and "stop" and "re-start" repeat N times, the microcomputer for system control judges that this state is system malfunction. Then it transmits stop command through UART and stops IC operation (latch).

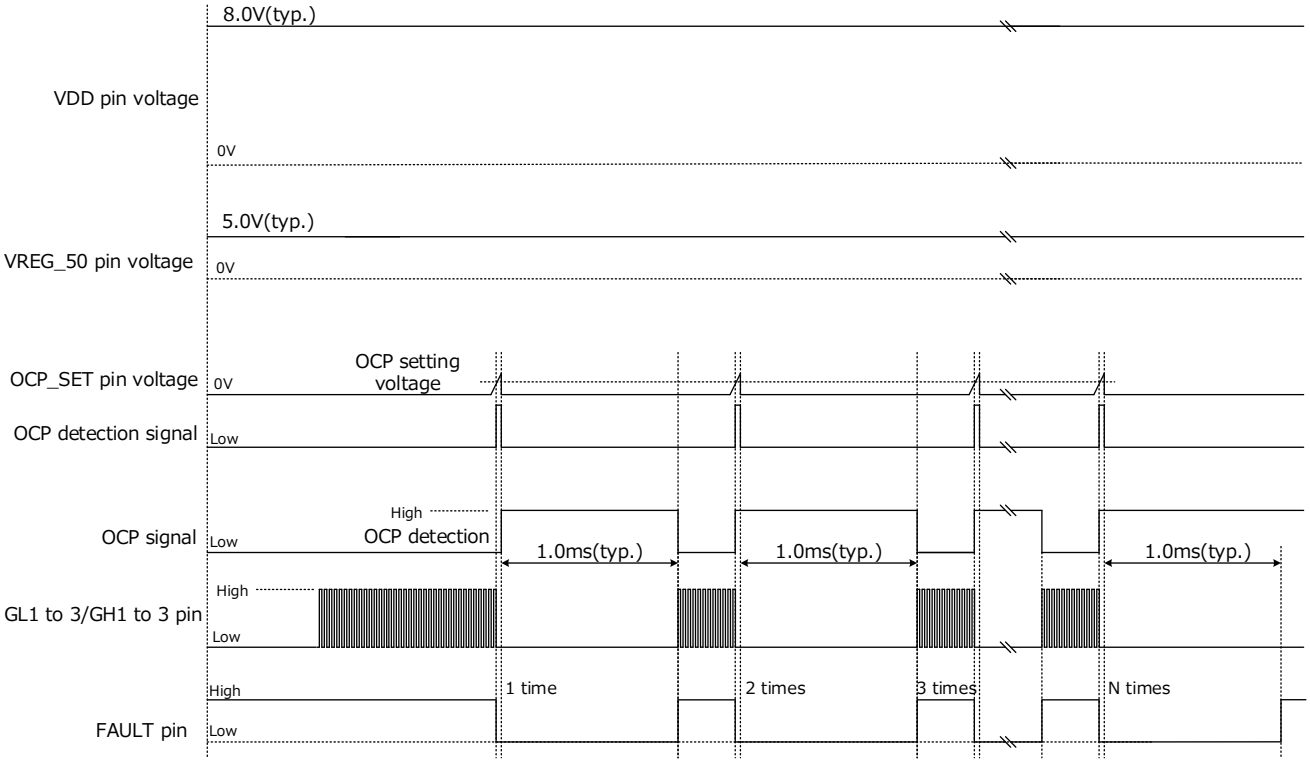


Figure-12

(6) Thermal shutdown (TSD) function

When ambient temperature rises, the resistance of the thermistor decreases and the pin voltage rises. The pin voltage rises to the threshold value which corresponds to TSD operation temperature or more, TSD circuit operates and configures GL1 pin (11pin), GH1 pin (12pin), GL2 pin (13pin), GH2 pin (14pin), GL3 pin (15pin), and GH3 pin (16pin) "L" (= 0 V) and stops switching.
In this time, FAULT pin (6pin) outputs "H" (= 5.0 V pull up) to "L" and it informs the microcomputer for system control that TSD operates.
When the ambient temperature falls to the threshold value which corresponds to TSD release temperature or less, TSD is released and the IC re-starts operation by soft start.
When the IC re-starts operation, FAULT pin (6pin) outputs "L" to "H".
When system failure is not cleared and "stop" and "re-start" repeat N times, the microcomputer for system control judges that this state is system malfunction. Then it transmits stop command through UART and stops IC operation (latch).

General description of startup sequence of solar power system

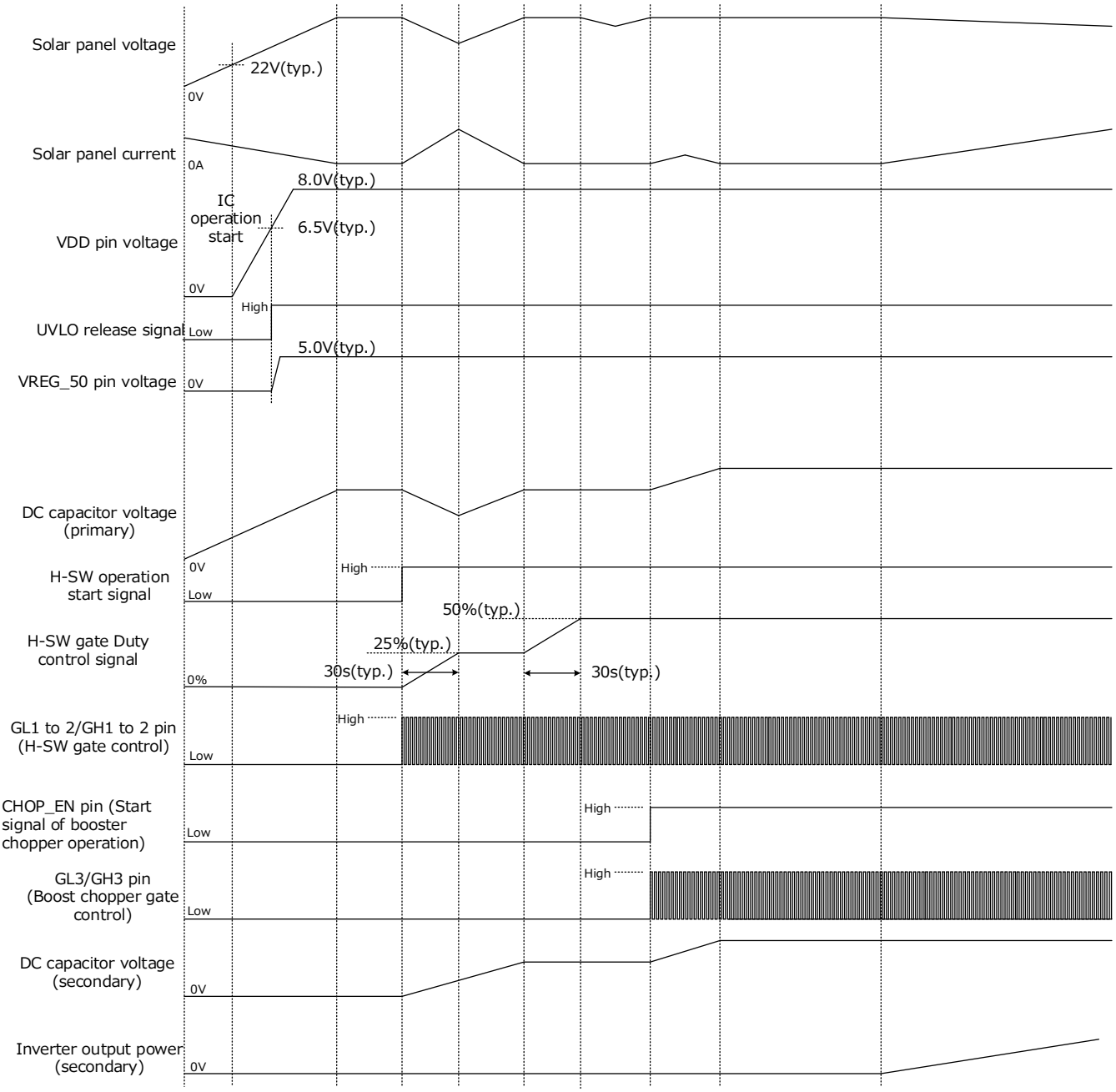
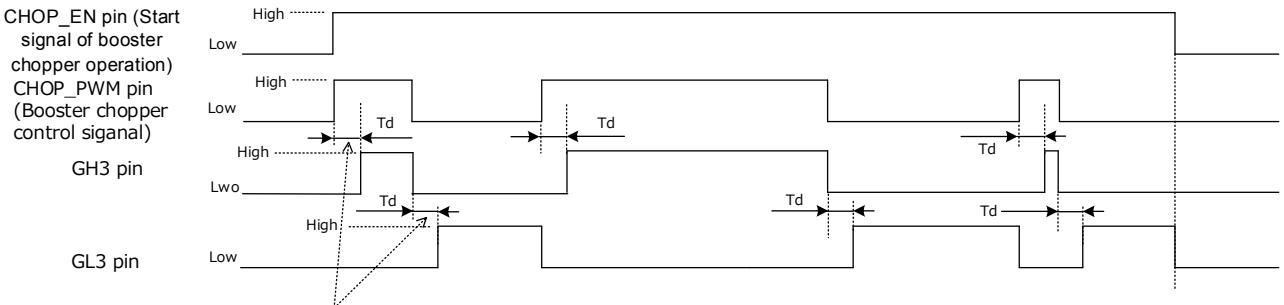


Figure-13(1)

Details of booster converter operation



When the GH3 and GL3 pins output H level by the booster chopper control signal, the dead time, Td is output as the head period. When the pulse width of the booster chopper control signal is shorter than Td, the booster chopper signal inputs enough longer time width than Td because the GH3 and GL3 pins do not output H level.

Figure-13(2)

Resonance control mode -> Shift sequence of LLC control mode (Example of control by external input signal)

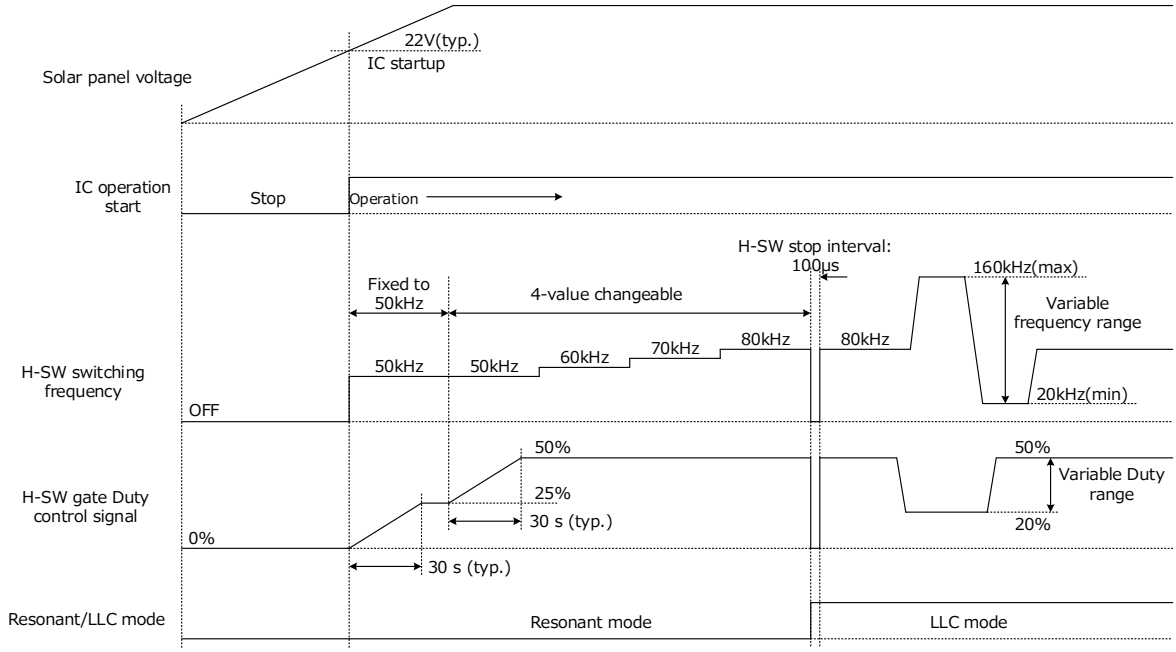


Figure-14

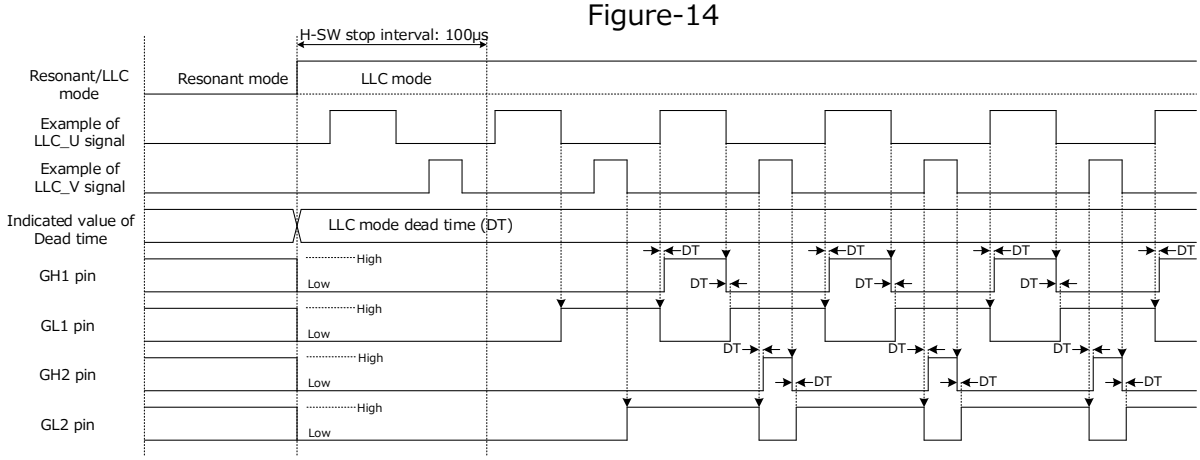


Figure-15

Changing sequence of dead time during operation in LLC control mode

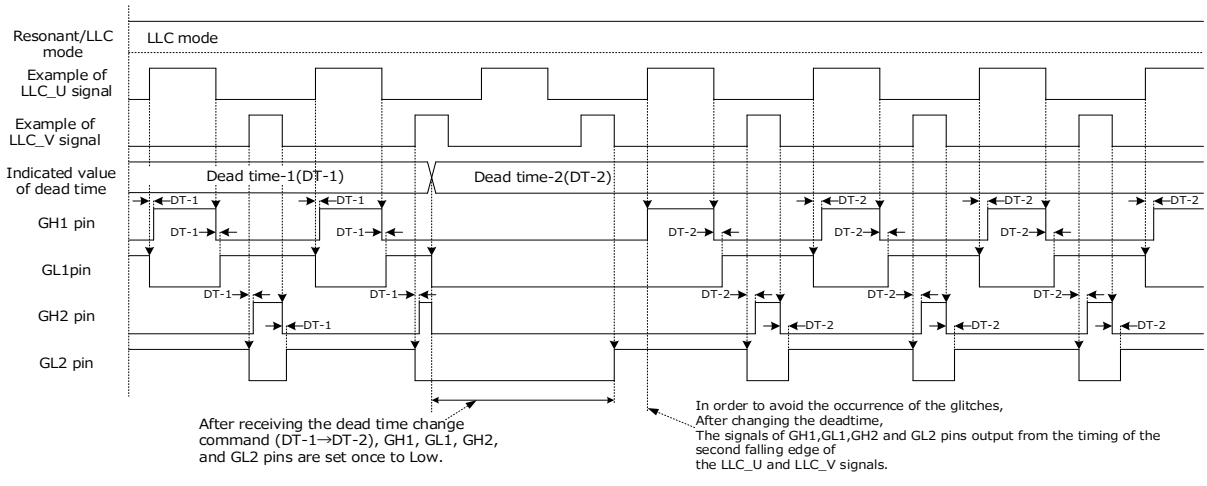


Figure-16

Communication flow between TC7716FTG and Control MCU in startup

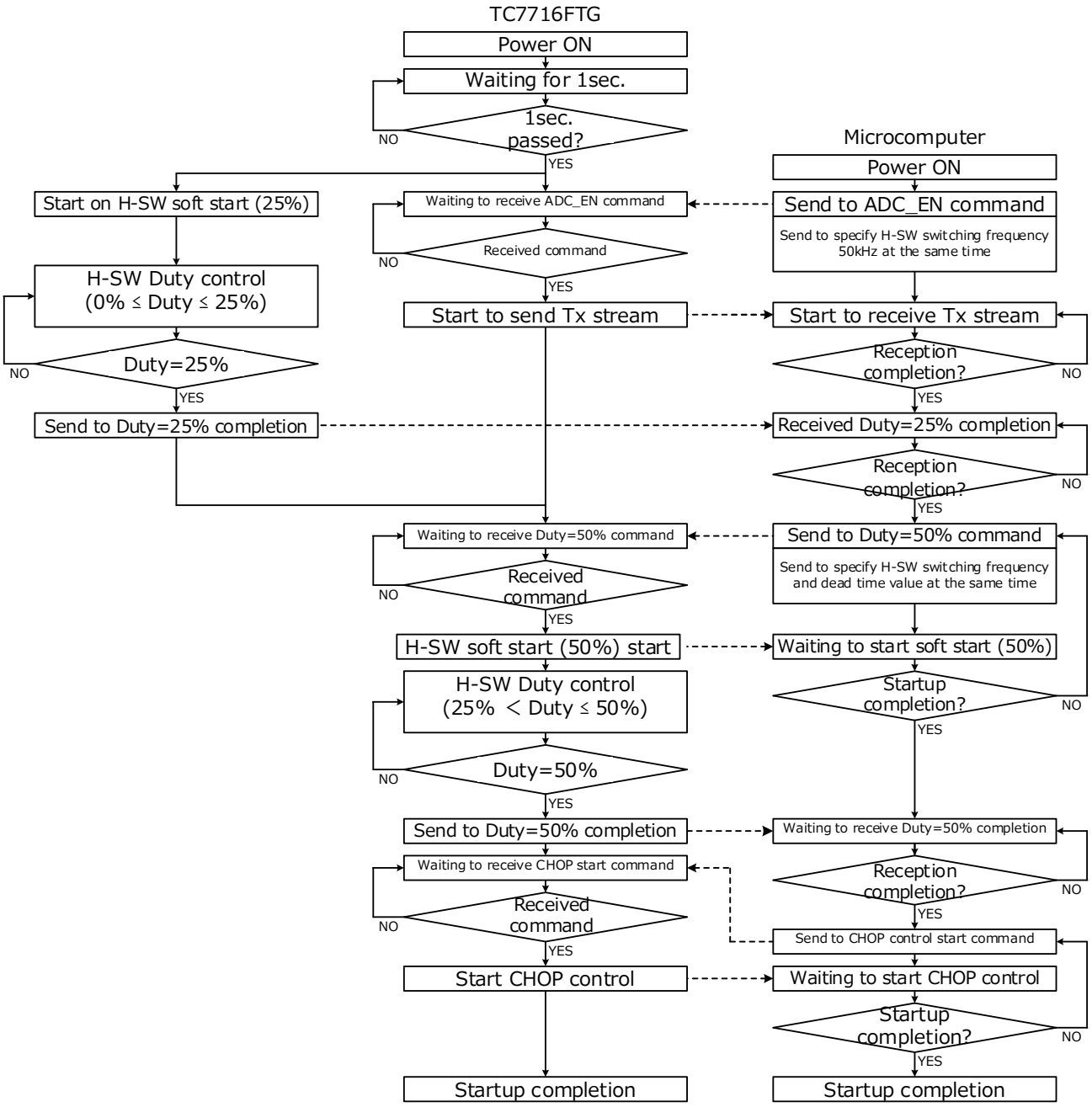
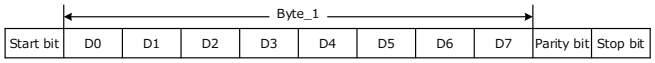


Figure-17

(*) During soft start (Duty change), do not change switching frequency of H-SW and designated value of dead time.

UART transmitting protocol

Information of data transmission times to MCU

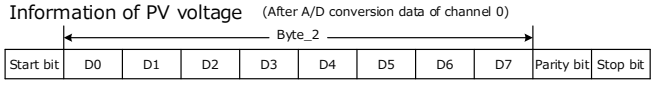


Transmission speed: 500 kbps (2μs / bit)
Parity : Even

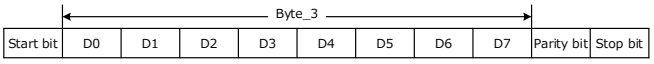
D0 =
D1 =
D2 =
D3 =
D4 =
D5 =
D6 =
Index: This register is counted up every transmitting 11-byte data from Byte_1 to Byte_11 per 500μs. It counts to 127 times and returns to 0 at the 128th time.

D7 = [1] Discrimination of the head byte: Head byte [1], Others: [0]

Information of PV voltage (After A/D conversion data of channel 0)

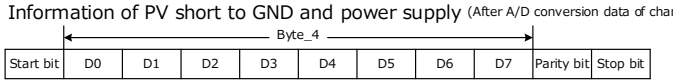


D0 = 7bit
D1 = 8bit
D2 = 9bit
D3 = 10bit
D4 = 11bit
After A/D conversion data of channel 0
D5 = [0]
D6 = [0]
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

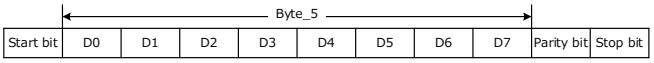


D0 = 0bit
D1 = 1bit
D2 = 2bit
D3 = 3bit
D4 = 4bit
D5 = 5bit
D6 = 6bit
After A/D conversion data of channel 0
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

Information of PV short to GND and power supply (After A/D conversion data of channel 1)

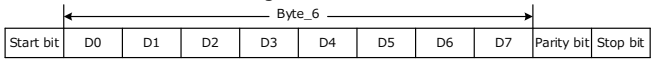


D0 = 7bit
D1 = 8bit
D2 = 9bit
D3 = 10bit
D4 = 11bit
After A/D conversion data of channel 1
D5 = [0]
D6 = [0]
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

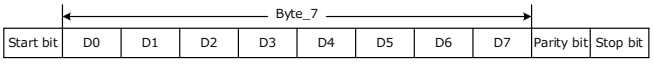


D0 = 0bit
D1 = 1bit
D2 = 2bit
D3 = 3bit
D4 = 4bit
D5 = 5bit
D6 = 6bit
After A/D conversion data of channel 1
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

Information of booster voltage (After A/D conversion data of channel 2)

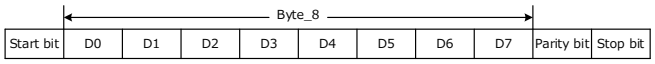


D0 = 7bit
D1 = 8bit
D2 = 9bit
D3 = 10bit
D4 = 11bit
After A/D conversion data of channel 2
D5 = [0]
D6 = [0]
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

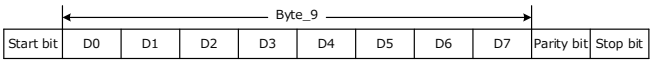


D0 = 0bit
D1 = 1bit
D2 = 2bit
D3 = 3bit
D4 = 4bit
D5 = 5bit
D6 = 6bit
After A/D conversion data of channel 2
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

Information of PV current (After A/D conversion data of channel 3)

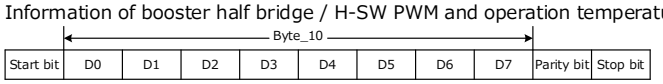


D0 = 7bit
D1 = 8bit
D2 = 9bit
D3 = 10bit
D4 = 11bit
After A/D conversion data of channel 3
D5 = [0]
D6 = [0]
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]



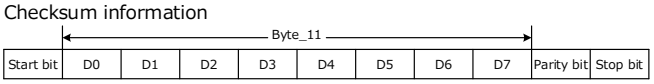
D0 = 0bit
D1 = 1bit
D2 = 2bit
D3 = 3bit
D4 = 4bit
D5 = 5bit
D6 = 6bit
After A/D conversion data of channel 3
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

Information of booster half bridge / H-SW PWM and operation temperature



D0 = H-SW gate pulse Duty 25% [1], Others [0]
D1 = H-SW gate pulse Duty over 25% to less than 50% [1], Others [0]
D2 = H-SW gate pulse Duty 50% [1], Others [0]
D3 = Booster gate pulse output enable [1], Disable [0]
D4 = Detection of abnormal temperature [1], Normal temperature [0]
D5 = LLC mode [1], Booster resonance control mode [0]
D6 = Protection circuit invalid [1], Normal operation [0]
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

Checksum information

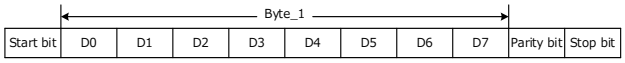


D0 = CS0
D1 = CS1
D2 = CS2
D3 = CS3
D4 = CS4
D5 = CS5
D6 = CS6
Checksum (7 bits) Checksum: MOD (- (Byte_1 + Byte_2) , 128)
D7 = [0] Discrimination of the head byte: Head byte [1], Others: [0]

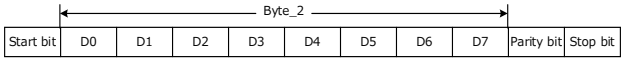
Figure-18

UART receiving protocol

Control state information

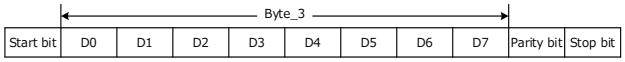


D0 = [1] Discrimination of the head Byte: Head Byte [1] , Others [0]
D1 = H-SW gate pulse Duty 50% enable: [1] Enable, [0] Disable
D2 = Boosting chopper control enable: [1] Enable, [0] Disable
D3 = H-SW operation mode selection: [1] LLC mode, [0] Booster resonation mode
D4 = Protection circuit invalidation: [1] Invalidation, [0] Normal operation
D5 = ADC output enable: [1] Enable, [0] Disable
D6 = H-SW control enable: [1] Enable, [0] Disable
D7 = [0]



D0 = [0] Discrimination of the head Byte: Head Byte [1] , Others [0]
D1 = DT0
D2 = DT1
D3 = DT2 H-SW dead time adjusting (4bits) -> Refer to Table-7.
D4 = DT3
D5 = SF1
D6 = SF2 H-SW switching frequency change (2 bits) -> Refer to Table-8.
D7 = [0]

Checksum information



D0 = [0]Discrimination of the head Byte: Head Byte [1] , Others [0]
D1 = CS0
D2 = CS1
D3 = CS2
D4 = CS3
D5 = CS4 Checksum (7 bits) Checksum: MOD (- (Byte_1 + Byte_2) , 128)
D6 = CS5
D7 = CS6

Transmission speed: 500 kbps (2μs / bit)

Parity: Even

Figure-19

Table-7

H-SW dead time adjusting (4 bits)

D4	D3	D2	D1	H-SW dead time [μs]
[0]	[0]	[0]	[0]	0.9
[0]	[0]	[0]	[1]	1.0
[0]	[0]	[1]	[0]	1.1
[0]	[0]	[1]	[1]	1.2
[0]	[1]	[0]	[0]	1.3
[0]	[1]	[0]	[1]	1.4
[0]	[1]	[1]	[0]	1.5
[0]	[1]	[1]	[1]	1.6
[1]	[0]	[0]	[0]	1.7
[1]	[0]	[0]	[1]	1.8
[1]	[0]	[1]	[0]	1.9
[1]	[0]	[1]	[1]	2.0
[1]	[1]	[0]	[0]	2.1
[1]	[1]	[0]	[1]	2.2
[1]	[1]	[1]	[0]	2.3
[1]	[1]	[1]	[1]	2.4

Table-8

H-SW switching frequency change (2 bits)

D6	D5	H-SW switching frequency [kHz]
[0]	[0]	50.000
[0]	[1]	59.524
[1]	[0]	69.444
[1]	[1]	80.645

Absolute maximum ratings (Unless otherwise specified, Ta=25°C)

Table-9

Characteristics	Symbol	Rating	Unit
Power supply voltage	Vdd	15.0	V
Maximum applied voltage for each pin	ViMAX	(*1)	V
Minimum applied voltage for each pin	ViMIN	GND-0.3(*2)	V
Power dissipation (*3)	P_D	3025	mW
Operating temperature	T_{opr}	- 40 to 85	°C
Storage temperature	T_{stg}	- 55 to 150	°C
Junction temperature	T_j	150	°C

*1:

Table-10(Maximum applied voltage for each pin)

Pin No.	Symbol	Rating	Unit
1	TEST1	V_{VREG_50} + 0.5	V
2	TEST2	V_{VREG_50} + 0.5	
3	TEST3	V_{VREG_50} + 0.5	
4	Tx	V_{VREG_50} + 0.5	
5	Rx	V_{VREG_50} + 0.5	
6	FAULT	V_{VREG_50} + 0.5	
7	CHOP_EN / LLC_V	V_{VREG_50} + 0.5	
8	CHOP_PWM / LLC_U	V_{VREG_50} + 0.5	
9	CL1	V_{VREG_50} + 0.5	
10	CL2	V_{VREG_50} + 0.5	
11	GL1	V_{VREG_50} + 0.5	
12	GH1	V_{VREG_50} + 0.5	
13	GL2	V_{VREG_50} + 0.5	
14	GH2	V_{VREG_50} + 0.5	
15	GL3	V_{VREG_50} + 0.5	
16	GH3	V_{VREG_50} + 0.5	

Pin No.	Symbol	Rating	Unit
17	NC	-	V
18	VDD	15.0	
19	NC	-	
20	GND	-	
21	NC	-	
22	VREG_50	(*4)	
23	OVP_SET	V_{VREG_50} + 0.5	
24	OCP_SET	V_{VREG_50} + 0.5	
25	EX_TSD	V_{VREG_50} + 0.5	
26	DC_IN	V_{VREG_50} + 0.5	
27	SH_LG	V_{VREG_50} + 0.5	
28	SH_IN	V_{VREG_50} + 0.5	
29	PVn_IN	V_{VREG_50} + 1.0	
30	PVp_IN	V_{VREG_50} + 1.0	
31	PVc_IN	V_{VREG_50} + 1.0	
32	RSTN	V_{VREG_50} + 0.5	

*2: 29pin (PVn_IN), 30pin (PVp_IN), and Pin 31pin (PVc_IN): GND - 2.0 V

*3: Board conditions: □76(mm)-1.6(mm)t-4 layer FR-4 board, internal layer 100%, external layer 3.5% (only pin assignment) In case of Ta = 25 °C or more, the power dissipation of 24.2 mW is decreased per 1 °C rising.

*4: Do not apply voltage from outside of the IC.

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

Package power dissipation (PD-Ta)

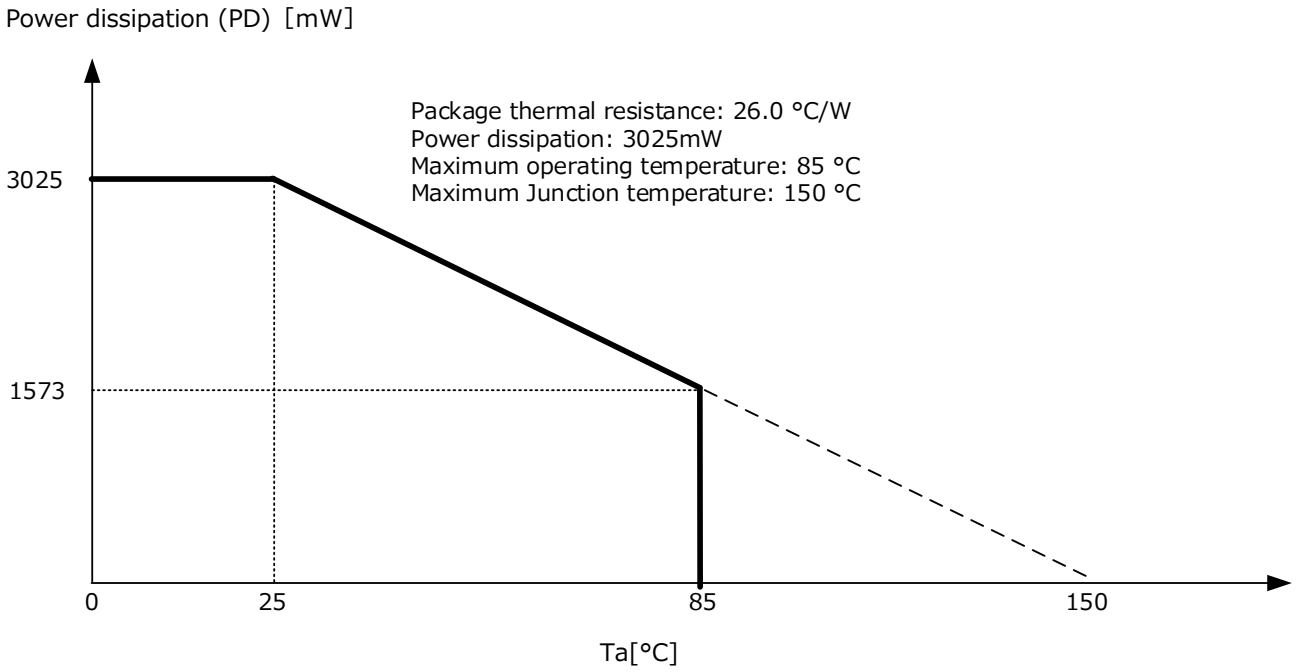


Figure-20

Operating condition (Ta = 25 °C)

Table-11

Characteristics	Symbol	Remarks	Min	Typ.	Max	Unit
Power supply voltage (Note)	Vdd	VDD pin	7.2	-	14.0	V

Note: Though it is a necessary power supply voltage range to operate the IC in stable, the IC starts operation at Startup voltage (Vstr).

Electrical characteristics (1) (Unless otherwise specified, Ta = 25 °C, Vdd = 8.0 V)

Table-12

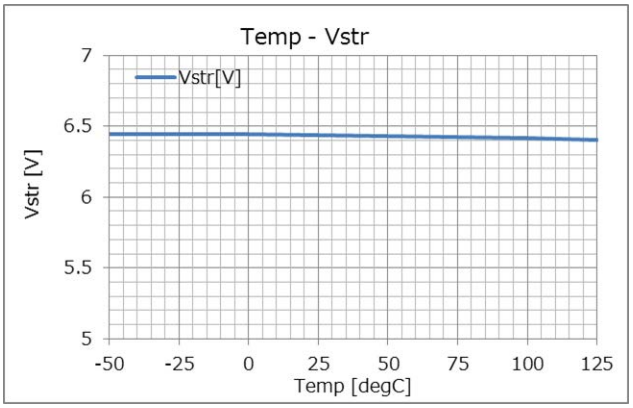
Characteristics	Symbol	Remarks	Min	Typ.	Max	Unit
Startup voltage (UVLO release voltage)	Vstr		6.0	6.5	7.0	V
UVLO operation voltage	Vuvlo		5.5	6.0	6.5	V
Consumption current	Idd	Pulse output pin: Open Switching frequency:50 kHz	-	-	30	mA
Reset voltage	Vrston	RSTN pin voltage	1.0	-	-	V
Reset release voltage	Vrstoff		-	-	4.0	
VREG_50 output voltage	VREG_50		4.75	5.00	5.25	V
VREG_50 output current	Ireg50		-	-	3.0	mA
I/O characteristics of digital interface block (Tx, Rx, FAULT, CHOP_EN/LLC_V, CHOP_PWM/LLC_U each pin)						
High level input voltage	VIH_PC		3.15	-	-	V
Low level input voltage	VIL_PC		-	-	0.90	V
High level input current	IIH_PC	Pin voltage: 5.0 V	-1.0	-	-	μA
Low level input current	IIL_PC	Pin voltage: GND	-	-	1.0	μA
High level output voltage	VOH_PC	Isource = 10 mA	4.50	-	-	V
Low level output voltage	VOL_PC	Isink = 10 mA	-	-	0.25	V
Booster DC-DC block						
Maximum voltage of output pulse	VOH_GHL3	GH3, GL3 pin: Isource = 5.0mA	4.5	-	-	V
Minimum voltage of output pulse	VOL_GHL3	GH3, GL3 pin: Isink = 5.0mA	-	-	0.5	
Dead time	Td	Crystal oscillator (10 MHz)	180	200	220	ns
Pin input current	IDC_IN	DC_IN pin voltage: 5.0 V	- 1.0	-	1.0	μA
OVP operation voltage	VOVP-on	DC_IN pin voltage when OVP_SET pin voltage is 3.5 V.	3.15	3.50	3.85	V
Starting time of OVP operation	TOVP-on	DC_IN pin voltage rises from 3.0 V to 4.0 V (Step) when OVP_SET pin voltage is 3.5 V.	2.8	4.3	5.8	μs
OCP operation voltage	VOCP-on	Voltage (V_{OCP_IN}) between SH_IN and SH_LG when OCP_SET pin voltage is 3.5 V.	99	110	121	mV
OCP release time	TOCP-off		-	1.0	-	ms
Thermal shutdown block						
Thermal shutdown voltage	VTTSD-on	EXT_TSD pin voltage	-	-	4.4	V
Thermal shutdown release voltage	VTTSD-off		3.8	-	-	
Flowing current of input pin	ITSD_IN	Applied voltage of EXT_TSD pin: 4.5 V	- 1.0	-	1.0	μA

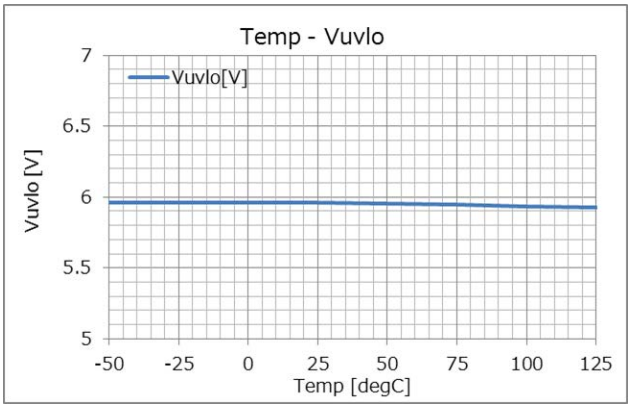
Electrical characteristics (2) (Unless otherwise specified, Ta = 25 °C, Vdd = 8.0 V)

Table-13

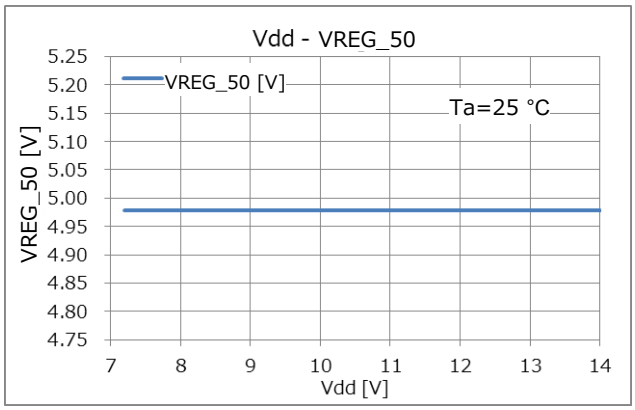
Characteristics	Symbol	Remarks	Min	Typ.	Max	Unit
H-SW block						
Switching frequency	Fhsw_50	Crystal oscillator (10 MHz) UART receiving Byte_2 : D6 = 0, D5 = 0	-	50.000	-	kHz
	Fhsw_60	UART receiving Byte _2 : D6 = 0, D 5=1	-	59.524	-	
	Fhsw_70	UART receiving Byte _2 : D6 = 1, D 5=0	-	69.444	-	
	Fhsw_80	UART receiving Byte _2 : D6 = 1, D5 = 1	-	80.645	-	
Soft start time	Tss	1st and 2nd each soft start time	-	30	-	s
Maximum voltage of output pulse	VOH_ GHL12	GH1, 2, and GL1, 2 pin: Isource=5.0 mA	4.5	-	-	V
Minimum voltage of output pulse	VOL_ GHL12	GH1, 2, and GL1, 2 pin: Isink=5.0 mA	-	-	0.5	
PWM pulse duty	DGHL12	Fixed value	-	50	-	%
Dead time adjusting range	Tdmin	UART receiving Byte _2 D4 = 0, D3 = 0, D2 = 0, D1 = 0	0.85	0.90	0.95	μs
	Tdmax	D4 = 1, D3 = 1, D2 = 1, D1 = 1	2.28	2.40	2.52	
Dead time adjusting step	Tdsetp	Adjusting step per 1 bit (4 bits)	-	100	-	ns
PV voltage detection block						
Maximum voltage of difference input	ΔVdif_PVp	Between PVp_IN and PVn_IN	0	-	4.0	V
Offset voltage of difference input	ΔVPVp	AD output conversion in short between PVp_IN and PVn_IN	- 100	0	100	mV
Pin input current	IPVp_IN	Applied voltage of PVp_IN pin: - 1.0 V	9	12	15	μA
		Applied voltage of PVp_IN pin: V_{VREG_50} + 1.0V	- 20	- 16	- 12	
	IPVn_IN	Applied voltage of PVn_IN pin: - 1.0 V	9	12	15	
		Applied voltage of PVn_IN pin: V_{VREG_50}+1.0V	- 20	- 16	- 12	
PV short to GND detection block						
Maximum voltage of difference input	ΔVdif_PVc	Between PVc_IN and PVn_IN	0	-	4.0	V
Offset voltage of difference input	ΔVPVc	AD output conversion in short between PVc_IN and PVn_IN	- 100	0	100	mV
Pin input current	IPVc_IN	Applied voltage of PVc_IN pin: - 1.0 V	9	12	15	μA
		Applied voltage of PVc_IN pin: V_{VREG_50} + 1.0V	- 20	- 16	- 12	
PV current detection block						
Maximum voltage of difference input	Vdif_SH	Between GNDs	- 0.36	-	0.24	V
	ΔVdif_SH	Between SH_IN and SH_LG	- 0.16	-	0.04	
Offset voltage of difference input	ΔVSH	AD output conversion in short between SH_IN and SH_LG	- 5.0	0	5.0	mV
Pin input current	ISH_IN	Applied voltage of SH_IN: - 0.36 V	9.2	11.5	14.9	μA
		Applied voltage of SH_IN: 0.24 V	2.8	3.5	4.5	
	ISH_LG	Applied voltage of SH_LG: - 0.36 V	9.2	11.5	14.9	
		Applied voltage of SH_LG: 0.24 V	2.8	3.5	4.5	
ADC block (Reference data: characteristics of ADC only)						
Integration non-liner error	INL	VREG_50 = 5.0 V	- 5	-	5	LSB
Differensiation non-liner error	DNL	VREG_50 = 5.0 V	- 4	-	4	LSB

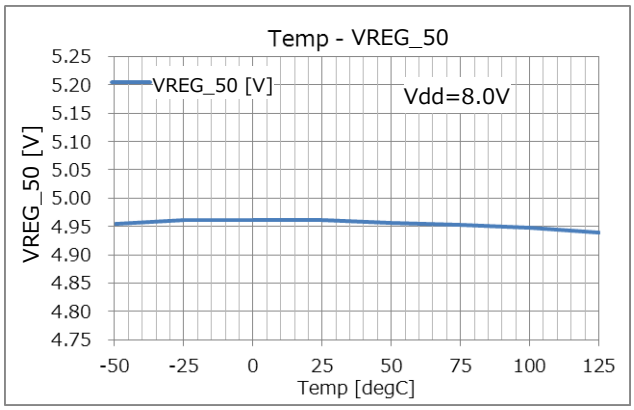
Temperature characteristics of startup and stop voltage

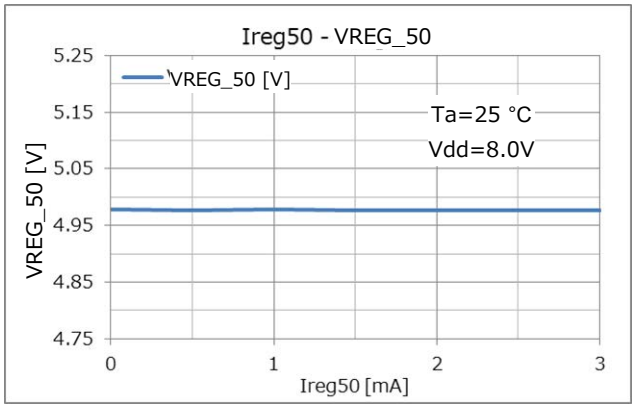




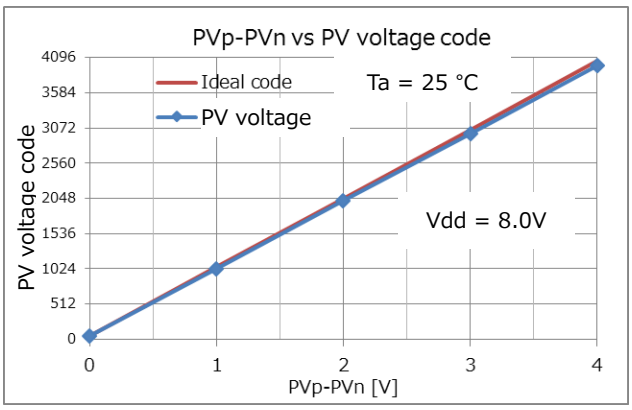
Output voltage characteristics of VREG_50 pin

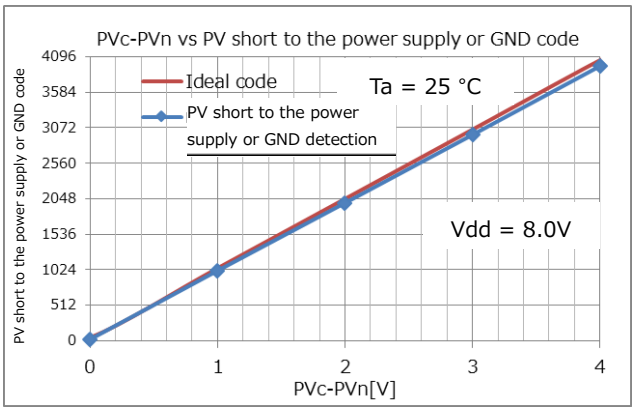


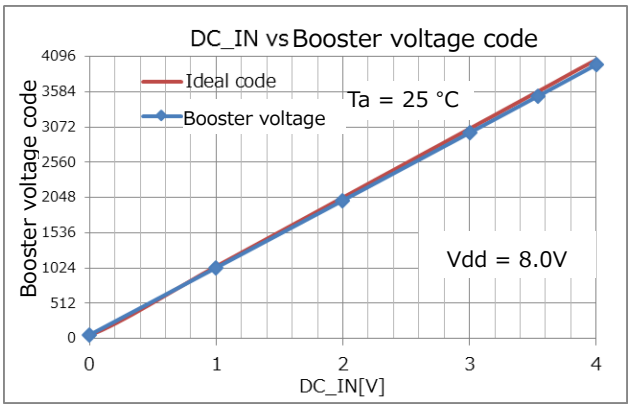


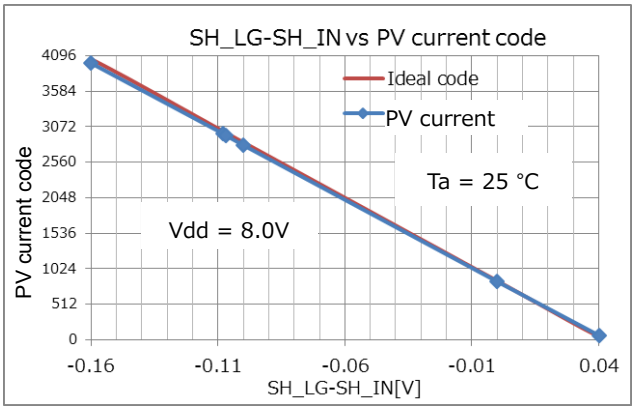


ADC characteristics





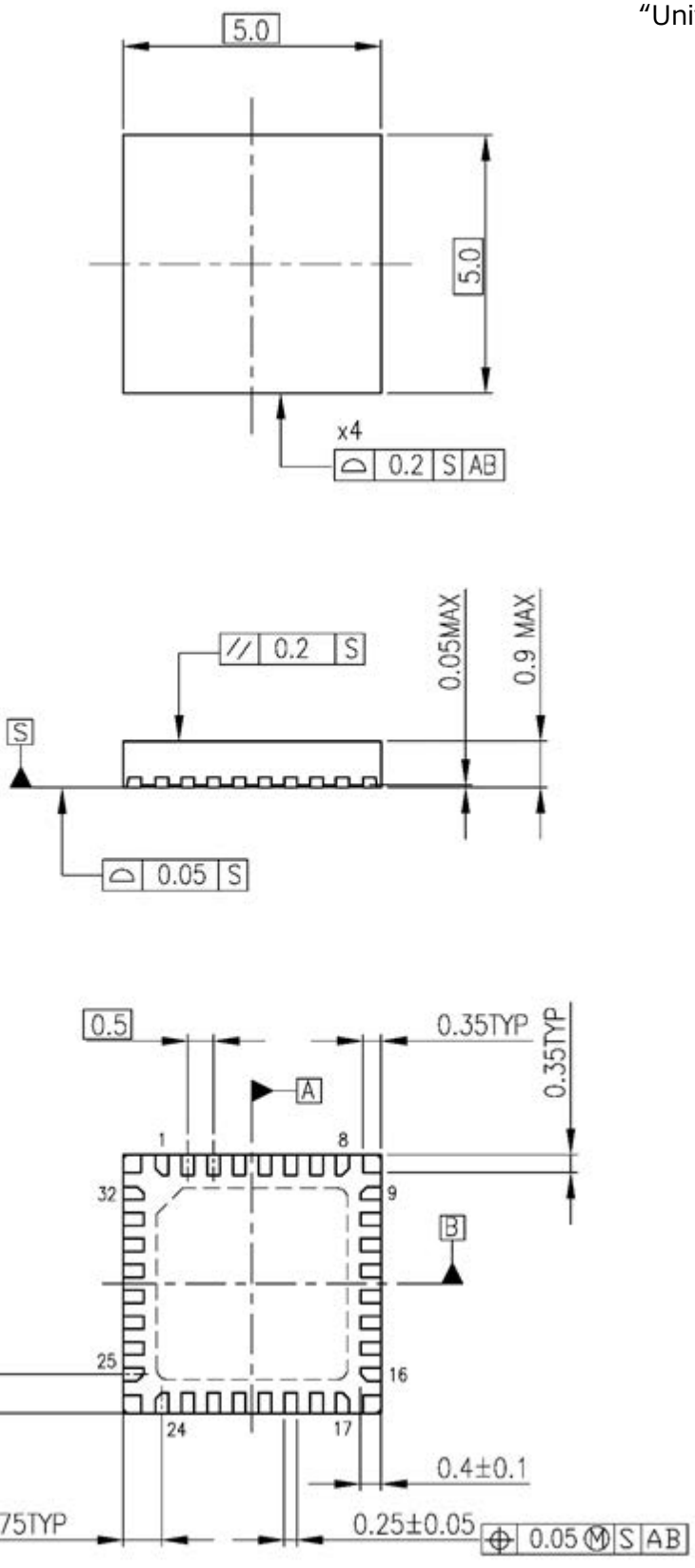




Package dimensions

P-VQFN32-0505-0.50-002

"Unit: mm"



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