Hints and Tips for Thermal Design for Discrete Semiconductor Devices

Description

This document describes how to reduce the chip temperature of discrete semiconductor devices.

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1. Comparison of MOSFET chip temperatures in different packages

At present, MOSFETs are available in many types of packages. Because each package has different thermal paths, the temperatures of MOSFET chips in different packages will not be the same even when they are operated at the same power. Table 1 lists Toshiba's major package offerings.

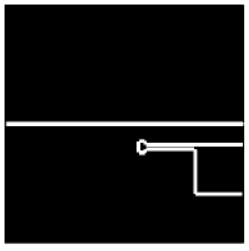
Semiconductor chip temperatures are trending upward. Major causes of this include a reduction in self-heat dissipation caused by a reduction in size of electronic devices, high-density board assembly, an increase in the ambient temperature of the operating environment, and an increase in the power losses incurred to achieve high-speed operation. These trends are driving the need for surface-mount packages with the optimal thermal performance.

Table 1 - Toshiba's major packages for discrete semiconductor devices

Pin count	Surface-mount packages			Through-hole packages		
2	CST2B US2H M-FLAT	CST2C US-FLAT	USC S-FLAT	TO-220-2L	TO-220F-2L	
3	CST3 SOT23 PW-Mini	UFM SOT-23F DPAK+	TSM S-Mini TO-220SM(W)	IPAK I2PAK TO-3P(L)	TO-220 TO-247	TO-3P(N) TO-220SIS
4	–			TO-247-4L		
6	ES6 UDFN6B	UF6 TSOP6F	UDFN6 VS-6	–		
8	VS-8 PS-8 DFN8 x 8	TSON Advance DSOP Advance SOP Advance	SOP-8	–		

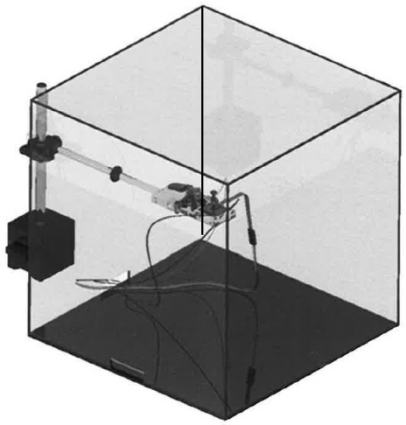
Figure 1 shows the results of measurement of chip temperatures of Toshiba's major MOSFET devices housed in various packages. The test conditions are as follows:

Power losses: 1 W
Test board: Toshiba's standard board
Measurement environment: JEDEC-compliant chamber with natural convection (JEDEC standard: JESD51-2A)
Others: Toshiba's unique board fixture, no heatsink



25.4×25.4×1.6
(Unit: mm)

Toshiba's standard board for chip temperature measurement (single-sided FR4 board)



Natural convection chamber

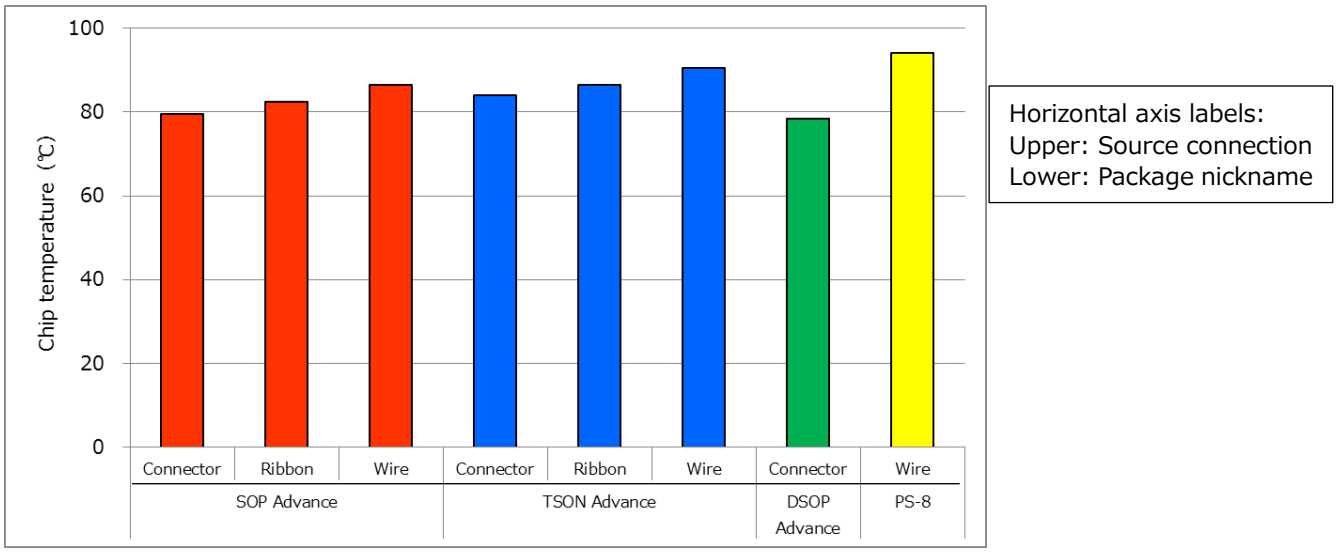


Figure 1 - Results of measurement of chip temperatures of Toshiba's major surface-mount MOSFETs

Chip temperature depends on the physical configuration of a package and the internal structure of a device. The power consumption of a device, the mounting conditions on a printed circuit board, and the environmental conditions affect thermal loads on the device. It should be noted, therefore, that chip temperature changes constantly in response to the load conditions. Obviously, a device must be used within the ranges of the maximum ratings. Generally, the higher the temperature, the shorter the lifetime of a semiconductor device. It is also important to reduce chip temperature in order to maintain device reliability.

2. Benefits of a heatsink

2.1. Size of a heatsink

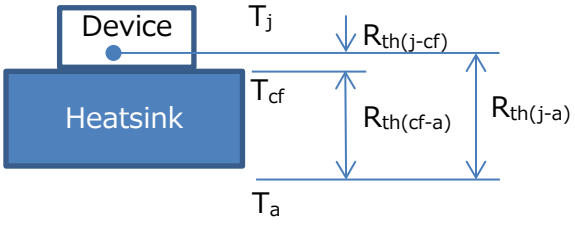
First, chip temperature can be reduced by using a heatsink. A heatsink transfers heat by conduction from a heat source to air. The choice of material, fin design and surface treatment are among the factors that determine the performance of a heatsink.

Heatsinks are generally made of metals such as aluminum that are easy to process and relatively inexpensive. Anodized coating (an electrolytic passivation process used to form an oxide layer on the surface of aluminum) allows a heatsink to dissipate heat more effectively. In addition, the thermal conductivity of aluminum is affected by processing methods. Common fin arrangements include straight fins and pin fins. The more surface area a heatsink has, the better the heat transfer performance it exhibits and the more effective it is in reducing chip temperature.

Figure 2 shows thermal resistance versus surface area curves for heatsinks with 1-mm- and 2-mm-thick aluminum fins. You can read an approximate thermal resistance of a heatsink from these curves. The thermal characteristics data for heatsinks are available on the websites of their manufacturers.

[Selecting a heatsink]

Power losses: P
Chip (junction) temperature: T_j
Temperature at the interface between a device and a heatsink: T_{cf}
Ambient temperature: T_a
Junction-to-case/fin thermal resistance: $R_{th(j-cf)}$
Case/fin-to-ambient thermal resistance: $R_{th(cf-a)}$



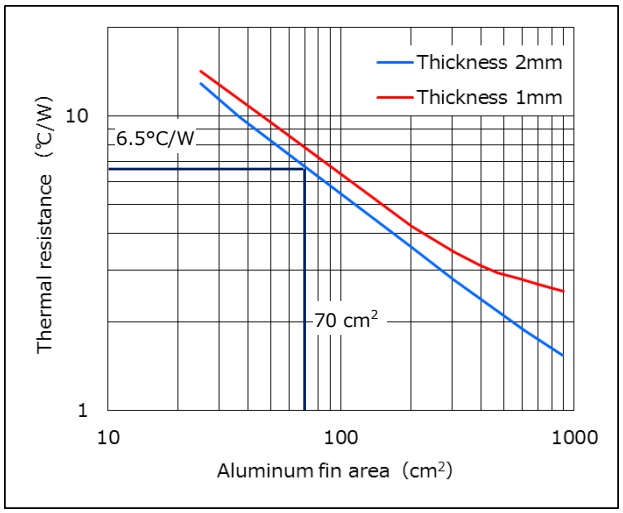


Figure 2 - Heatsink surface area vs. thermal resistance (example)

In the above figure, thermal resistance, power and temperature have the following relationship:

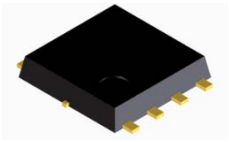
$(R_{th(j-cf)} + R_{th(cf-a)}) \times P = (T_j - T_a)$ Hence,

$R_{th(cf-a)} = ((T_j - T_a)) / P) - R_{th(j-cf)}$

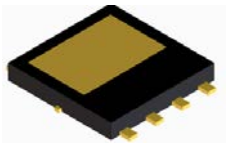
When $T_j = 120°C$, $T_a = 50°C$, $P = 10$ W and $R_{th(j-cf)} = 0.5°C/W$ (ignoring the contact thermal resistance between the device and the heatsink), $R_{th(cf-a)}$ is calculated to be 6.5°C/W. Therefore, the thermal performance requirement can be satisfied by using a heatsink with a $R_{th(cf-a)}$ lower than 6.5°C/W. Figure 2 shows that the surface area of this heatsink becomes approximately 70 cm^2 if you use one with 2-mm-thick aluminum fins.

2.2. Double-sided-cooling packages

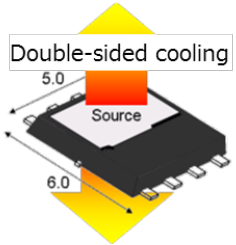
Figure 3 shows two types of Toshiba's major surface-mount packages: SOP Advance and DSOP Advance. While SOP Advance is a typical surface-mount package that dissipates heat only from the bottom surface, DSOP Advance effectively dissipates heat from both the top and bottom surfaces.



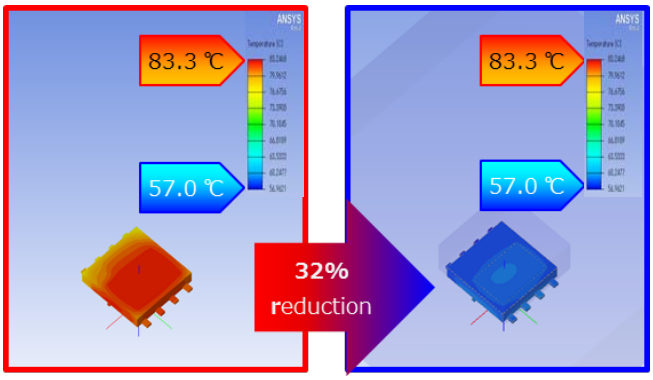
SOP Advance package



DSOP Advance package



Heat dissipation from the top and the bottom surface of DSOP Advance



Benefit of the double-sided-cooling DSOP Advance (Simulation)

Figure 3 - SOP Advance and DSOP Advance packages, and double-sided cooling

Our simulation shows that the chip temperature can be reduced approximately 32% by attaching a heatsink on the top of the DSOP Advance package, compared to the case without a heatsink. In cases where heat can hardly be dissipated from the bottom of a package (i.e., when it is difficult to add thermal vias or copper inlay), attaching a heatsink at the top of the package will provide an equivalent heat removal capability. Figure 3 indicates that a double-sided-cooling package obviously helps reduce chip temperature.

It is also beneficial to use thermal grease (a thermal interface material, or TIM) for the thermal interfacing between a heatsink and the top surface of a device. Figure 4 shows the curves of chip temperature measured for different TIM thicknesses. The higher the power losses, the higher the chip temperature becomes. At 2.5 W, the chip temperature was the lowest when the package had the thinnest TIM with a thickness of 0.05 mm. A thick TIM might have a contrary effect because the TIM does not have high thermal conductivity. The role of TIM is to fill the uneven interface between a heatsink and a device in order to eliminate air gaps or spaces and thereby increase thermal conductivity. It is therefore important to apply TIM evenly on the interface area.

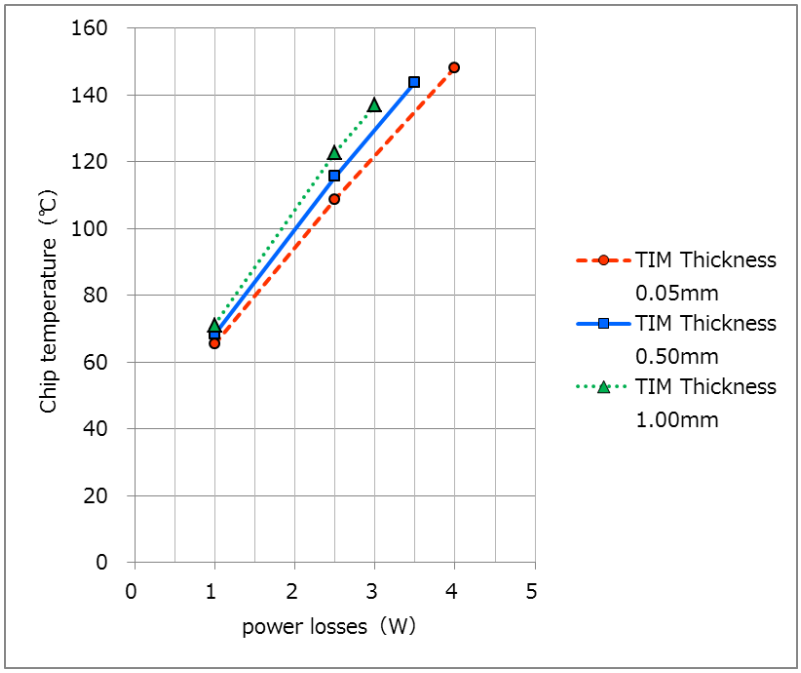


Figure 4 - Effect of the thickness of a TIM between a heatsink and the package top surface

3. Effects of a printed circuit board on chip temperature

3.1. Number of board layers

As the downscaling of semiconductor devices advances to increase the density of board assembly, their surface areas have become progressively smaller, degrading the heat dissipation capability. As a result, it is becoming difficult to reduce chip temperature only through device improvement.

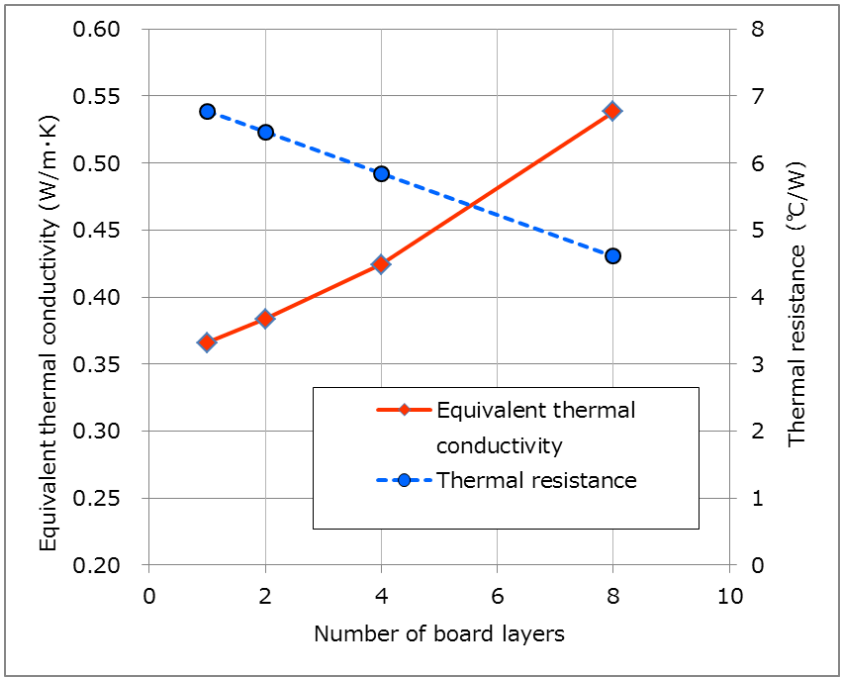
Most of the heat generated by a device is transferred to a printed circuit board via the drain frame

(E-pad). Part of this heat is dissipated by convection from the interface with the surrounding air, and part of it is transferred to air by radiation. However, most of the generated heat is dispersed by thermal conduction to the top and bottom surfaces and internal structures of a board.

In order to improve heat dissipation from a board and thereby reduce chip temperature, heatsinks can be directly mounted on the board.

Heatsinks are generally attached on the backside of a board. It is therefore desirable to use a board with high thermal conductivity in order to allow heat to be effectively transferred from the top surface of the board with semiconductor devices to the heatsinks on the backside. However, the choice of materials that can be used is restricted by costs.

The equivalent thermal conductivity can be increased by using a multilayer board with copper trace layers, which helps increase the amount of heat transferred to the heatsinks on the backside of the board. Figure 5 shows the equivalent thermal conductivities calculated for boards with different numbers of copper trace layers, and a thermal resistance curve calculated based on them. As shown in Figure 5, as the number of copper trace layers increases, the equivalent thermal conductivity of a board increases, and its thermal resistance decreases.



Board size: 25.4×25.4 mm, 1.6-mm thick
Copper trace thickness: 70 μm (2 ounces)
Thermal conductivity:
Copper traces = 388 W/m·K
FR4 substrate = 0.35 W/m·K
Board structure: Copper and FR4 layers with the same thickness
Other: The shapes of copper traces are not considered. The assumption is that copper covers the entire board.
Equation for calculating thermal resistance

$$R_{th} = \frac{T}{\lambda \cdot S}$$

T: Thickness (m)
λ: Thermal conductivity (W/m·K)

Figure 5 - Example of calculation results for the equivalent thermal conductivity and thermal resistance of a board

Figure 6 shows the results of chip temperature measurement using two boards with different numbers of layers. For this measurement, we used a double-sided-cooling DSOP Advance package to remove heat from both sides of the package and experimented with different TIM thicknesses. For all TIM thicknesses, the chip temperature is lower on the four-layer board than on the standard single-layer board. Because we used the same heatsink on both boards, it is considered that a difference in board structure caused the difference in chip temperature.

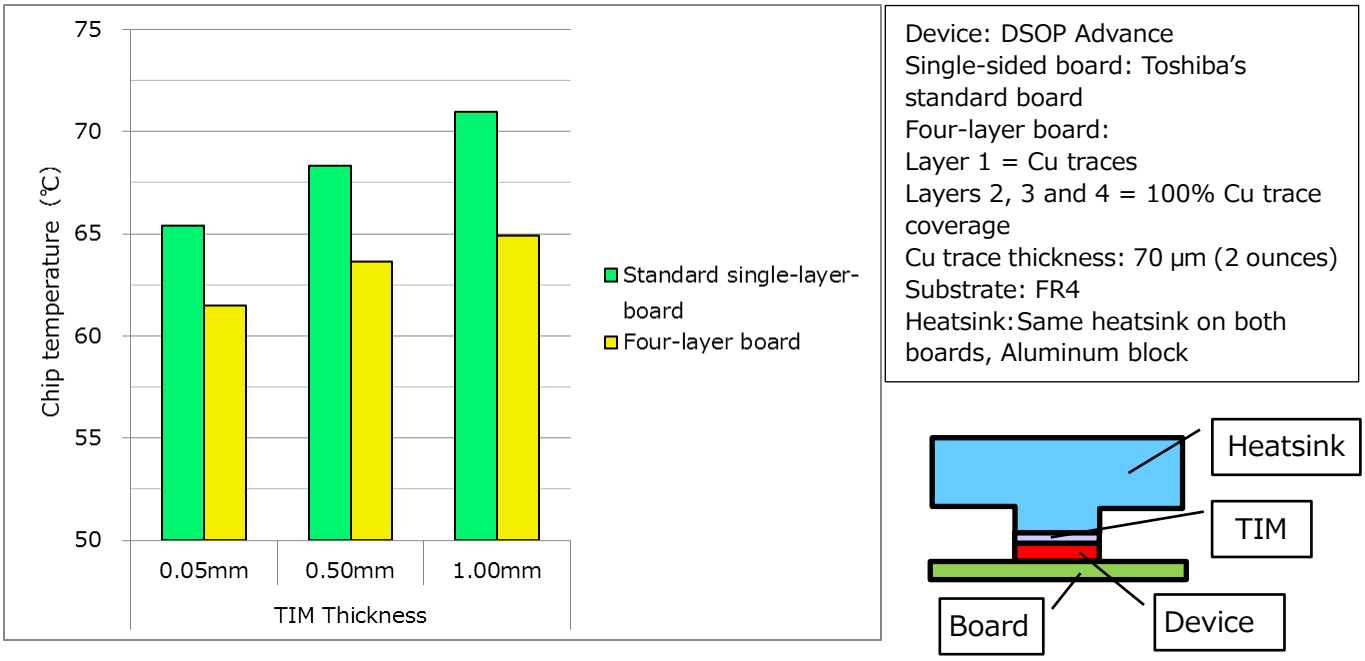


Figure 6 - Effects of multilayer boards on chip temperature

3.2. Benefits of thermal vias #1

In addition to the use of a multilayer board, the thermal performance of a board can be improved by adding thermal vias. A thermal via is a hole drilled through the board that is made conductive by electroplating a metal with high thermal conductivity such as copper into the hole barrels. Thermal vias provide thermal paths from the top to the bottom surface of a board, increasing the area from which heat is dissipated. In addition, thermal vias make it easy to create thermal conduction paths to heatsinks attached on the backside of the board. Heat dispersion using thermal vias is indispensable for space-critical boards. Typically, thermal vias have a diameter of roughly 0.3 mm. Smaller vias tend to cause misalignment between layers during the electroplating process. Conversely, larger vias might cause solder to flow into vias during board assembly, decreasing the wetting of solder on devices and thereby increasing thermal resistance.

Figure 7 shows the results of chip temperature measurement for SOP Advance packages having different numbers of thermal vias through the drain pattern.

As shown in Figure 7, the more thermal vias the drain pattern has, the lower the chip temperature.

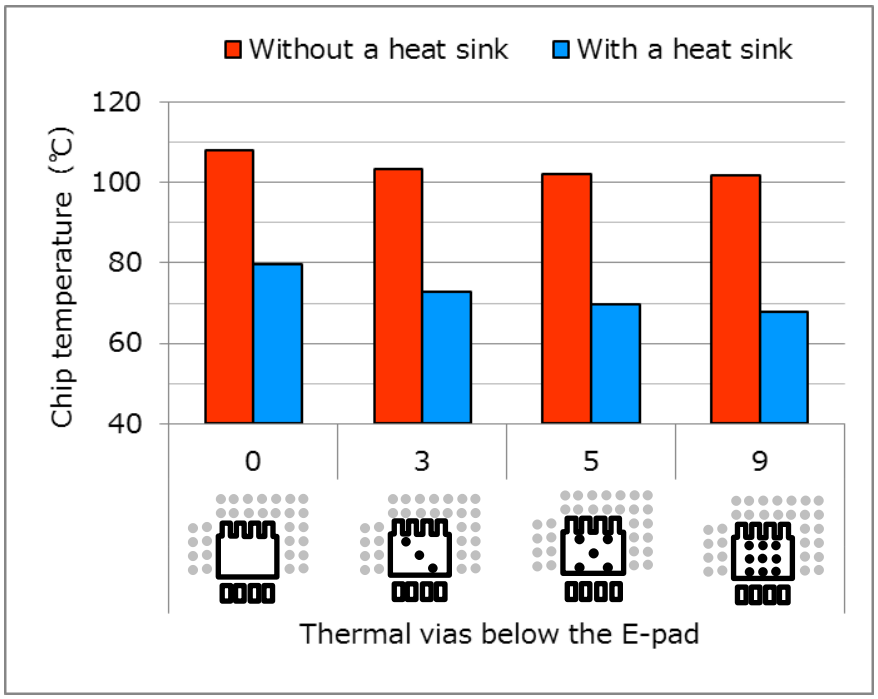


Figure 7 - Benefits of thermal vias just below the E-pad

3.3. Benefits of thermal vias #2

Care should also be exercised as to the arrangement of thermal vias around semiconductor devices. Figure 8 shows the results of chip temperature measurement for different arrangements of thermal vias in and around the drain pattern. A device with a row of peripheral vias exhibited a chip temperature slightly lower than a device without peripheral vias. However, adding one more row of peripheral vias around a device did not help to further reduce chip temperature. This indicates that peripheral vias are less effective than the vias just below the E-pad in reducing chip temperature. The combined use of thermal vias and heatsinks is more effective.

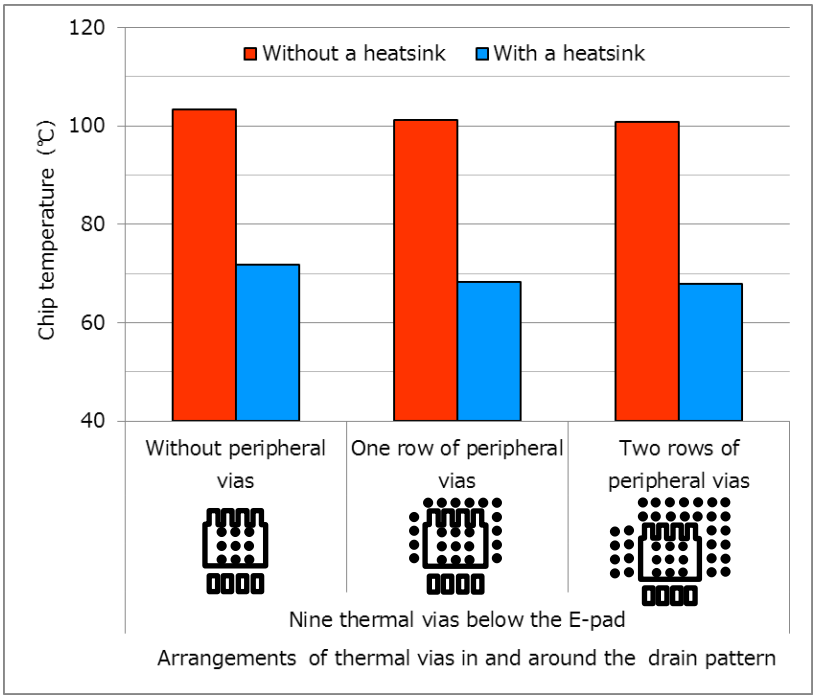
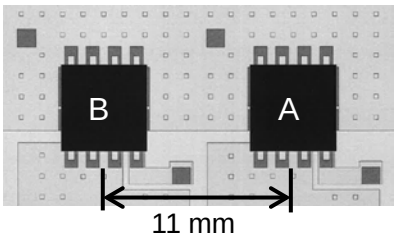


Figure 8 - Arrangements of thermal vias versus chip temperatures

4. Thermal interference between semiconductor devices

When multiple heat-generating devices are mounted on a board, thermal interference occurs, depending on the distances between them.

Care should be exercised when placing two devices that will be heated to a high temperature in close proximity because their temperatures further increase in the event of thermal interference. Figure 9 shows two devices placed with a center-to-center distance of 11 mm. The right-hand bar graph compares thermal resistance for cases in which only Device A is operated and both A and B are operated simultaneously. These thermal resistance values were calculated based on temperature measurements. The bar graph shows that thermal interference causes the thermal resistance to increase when two devices are operated at the same time.



Single-device operation: Only A is operated.
Dual-device operation: Both A and B are operated.

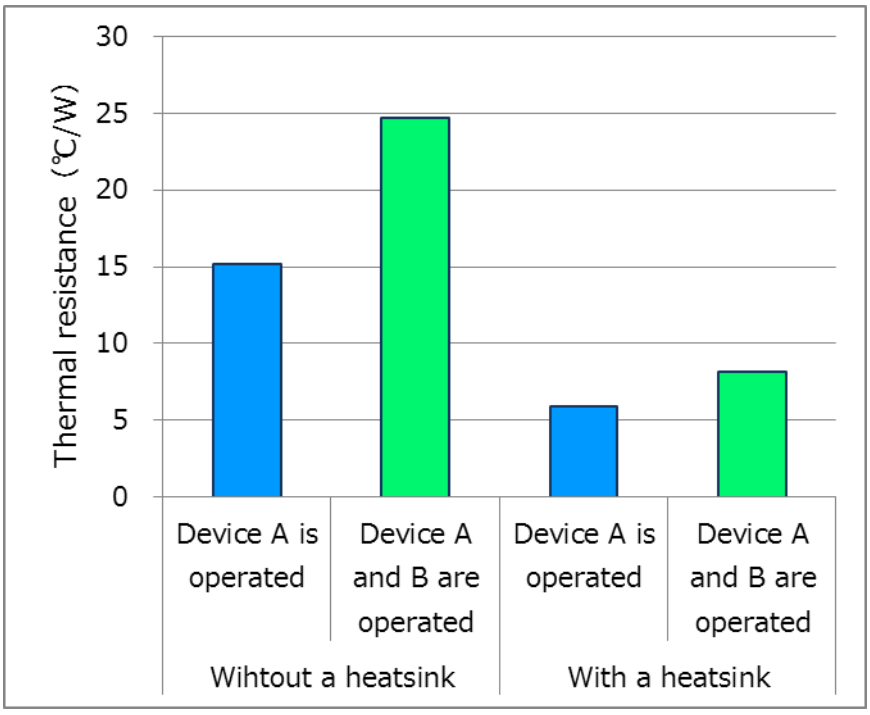


Figure 9 - Influence of thermal interference on thermal resistance

Figure 10 shows the temperatures of three devices when they are placed side by side with a center-to-center distance of 11 mm.

When A and B were operated simultaneously without a heatsink, their chip temperatures exceeded 85ºC. When A and C, which are further apart from each other, were operated simultaneously, their chip temperatures did not reach 85ºC.

As demonstrated by this example, two devices placed in proximity might suffer considerable thermal interference. The devices might be damaged if their temperatures increase more than expected. To prevent thermal interference, devices that generate a lot of heat should be placed as far apart as possible. In addition, it is important to use heatsinks and other cooling devices.

Heatsinks help reduce chip temperature and therefore thermal interference between devices.

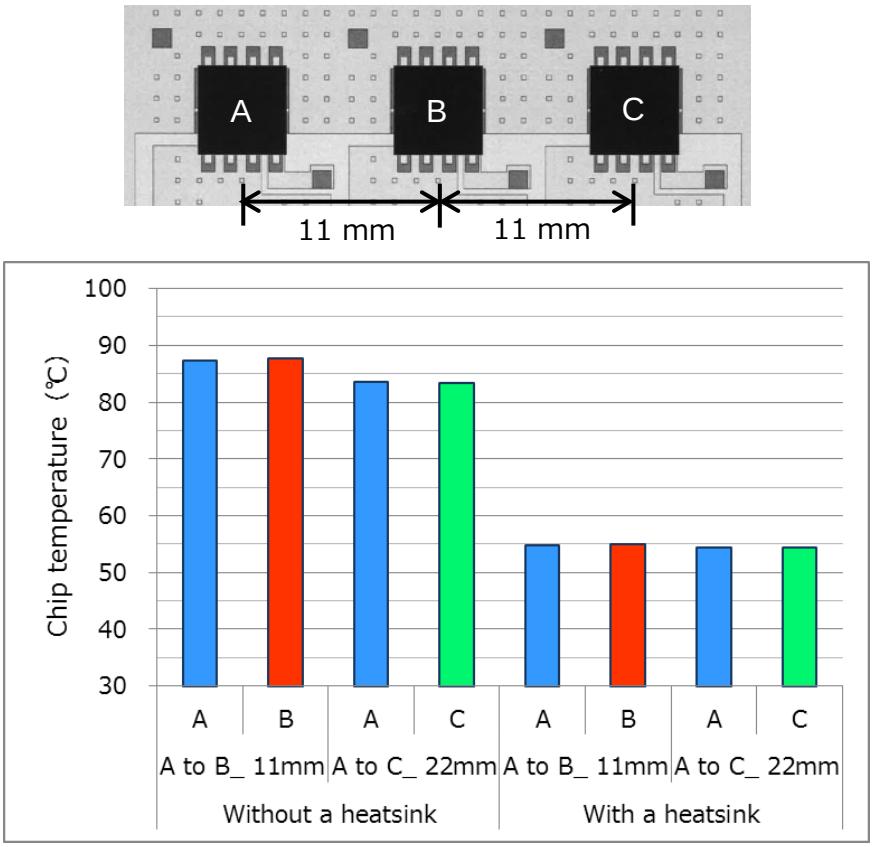
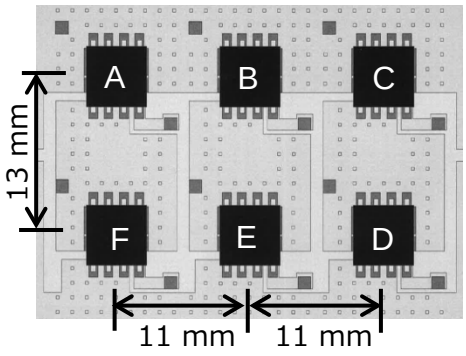


Figure 10 - Thermal interference: Impact of device-to-device distances

Figure 11 shows a board with six devices and their temperatures on the package top surface when they were operated simultaneously. A heatsink is attached on the back of this board. As shown in the right-hand bar graph, thermal vias and the heatsink help reduce the chip temperature of each device. However, the temperatures of Device B and Device D in the middle became higher than those of the other devices. This indicates that care should be exercised concerning the devices between heat sources.



Device arrangement

·The drain leads of A, B and C are connected to the same trace.
·The source leads of D, E and F are connected to the same trace.
·The six devices are connected in a two-in-series, three-in-parallel configuration.
·Current flows thru all six devices.

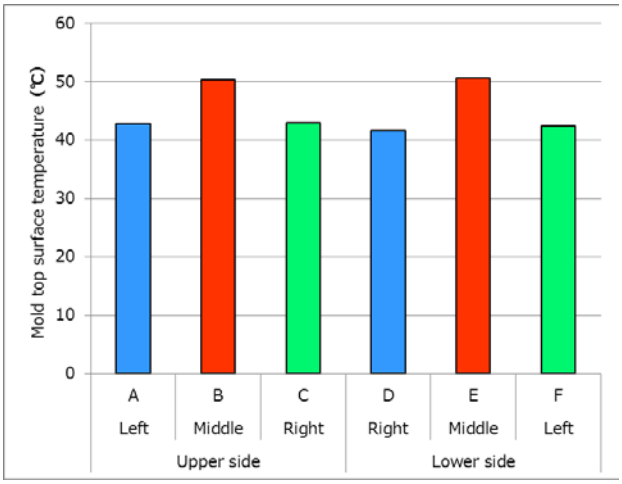


Figure 11 - Temperatures on the top surface of packages during operation

5. Effect of the copper trace coverage

Chip temperature can also be reduced by increasing the area of copper traces. Figure 12 shows the changes in chip temperature when the copper coverage of Layer 1 is changed on Toshiba's standard board (25.4 mm × 25.4 mm, t = 1.6 mm, Cu trace thickness = 70 μm, single trace layer). This board model has no thermal via and has 98% Cu trace coverage. From the copper traces, heat disperses into the board and to its backside. There is a difference of roughly 30°C in chip temperature between boards with copper coverage of 98% and 33%. A board with greater copper coverage is more desirable in terms of heat dissipation.

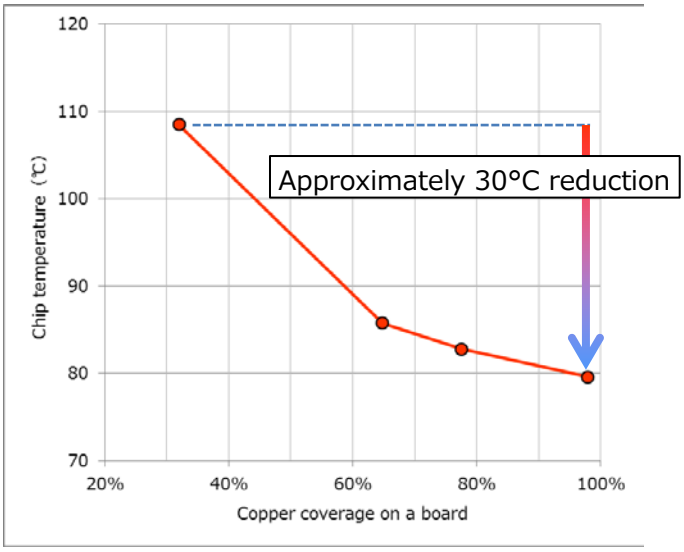
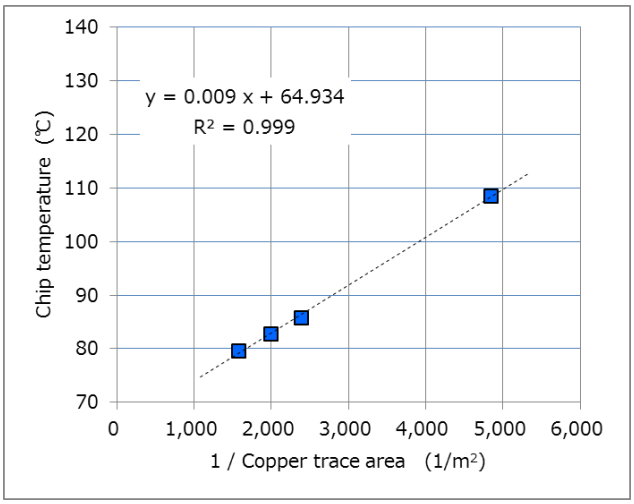


Figure 12 - Copper coverage on a board versus chip temperature



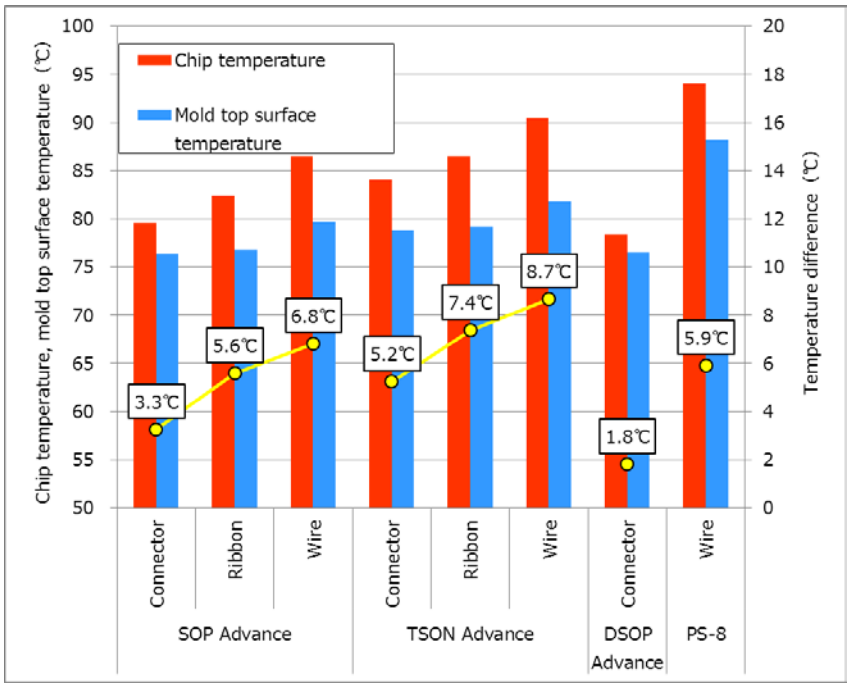
The relationship between the reciprocal of the trace area and chip temperature is linearly approximated as shown above.

In other words, chip temperature decreases in inverse proportion to the trace area.

6. Relationship between package and chip temperatures

Care should be exercised as to chip temperature in using semiconductor devices. However, technical datasheets for semiconductor devices can be used only as a reference in estimating chip temperature. Because thermal resistance is affected by ambient conditions, a circuit board and other factors, datasheet values cannot be used as-is for real-world applications. A workaround for this problem is to use a thermocouple to directly measure the temperature on the top surface of a device's package mold. Figure 13 shows chip temperatures versus temperatures on packages' mold top surface.

The temperatures on the mold top surface were measured with a thermocouple as shown below. As shown in Figure 13, differences between chip temperature and the temperature on the mold top surface resulted from differences in device structure. Connector bonding resulted in a temperature difference of 3 to 5°C and ribbon bonding led to a temperature difference of 5 to 7°C. Wire bonding produced a temperature difference of 7 to 9°C. Wire-bonded packages require special care for measurement as they exhibit a significant difference in temperature.



Test conditions
Test board: Toshiba's standard board (Cu covered)
Board size: 25.4×25.4mm
Board thickness: 1.6 mm
Copper traces: Single layer,
Thickness = 70 μm (2 ounces)
Environment: Equivalent to the standard JEDEC natural convection condition (JEDEC-specified chamber)
Power losses: 1.0 W

Horizontal axis labels:
Upper: Source connection
Lower: Package nickname

Figure 13 - MOSFET chip temperatures versus packages' mold top surface temperatures

7. Measuring the temperature on the top surface of the package mold

As shown in the previous section, wire-bonded packages had a significant difference between chip temperature and the mold top surface temperature. Because thermal paths in wire-bonded packages are thinner than those in other types of packages, high-temperature areas tend to be localized in wire-bonded packages. Heat concentrates on the portions just above a chip and in the vicinity of bonding wires. Consequently, heat becomes unevenly distributed across the top surface of the package mold. As shown in Figure 14, a fine-wire thermocouple, which is used to prevent heat dissipation, causes variations in measurement results, depending on positions where measurements are taken. As a workaround, metal tape with high thermal conductivity (e.g., aluminum tape) can be affixed on the mold top surface. Variations in temperature measurement can be reduced to a certain degree by attaching a thermocouple to the metal tape. The position at the highest temperature should be measured properly. However, if it is difficult to do so, a measurement error can be reduced by using this workaround.

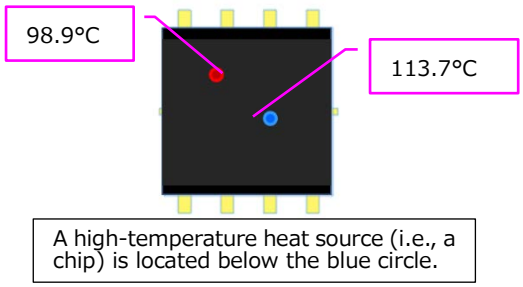


Figure 14 - Mold top-surface temperature

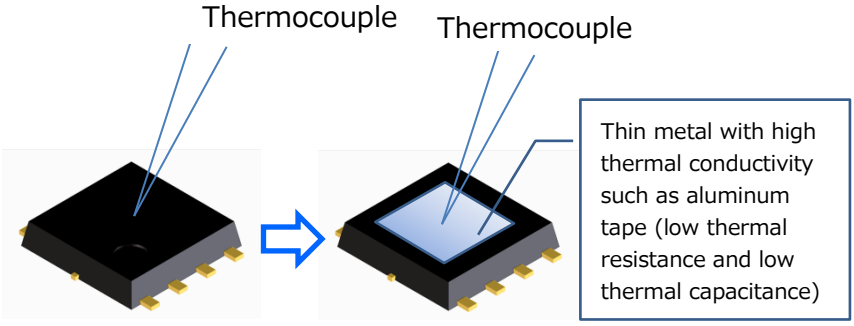


Figure 15 - Measuring the temperature of the mold top

8. Simulation using a simple tool

Toshiba can perform a simplified thermal simulation. Figure 16 shows an example of thermal analysis using a simplified simulation. Simulation allows you to quickly estimate chip temperature.

[Internal device temperatures and temperature distribution on the board surface]

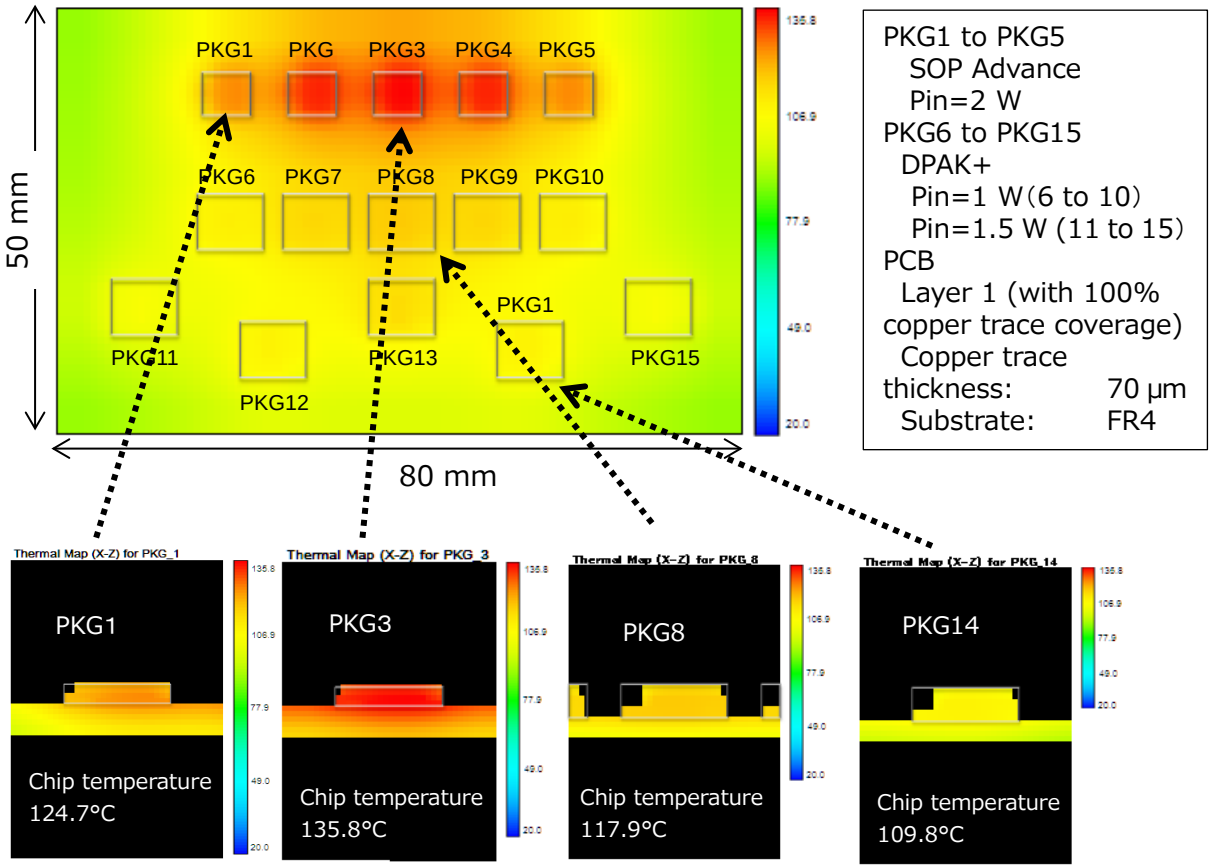


Figure 16 - Example of a simplified simulation of internal device temperatures and temperature distribution on the board surface

* The power losses to the devices are arbitrary.

In this example, the temperature of PKG3 is so high that countermeasures are necessary to reduce its temperature.

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