Parasitic Oscillation and Ringing of Power MOSFETs

Description

This document describes the causes of and solutions for parasitic oscillation and ringing of power MOSFETs.

Table of Contents

1. Parasitic oscillation and ringing of a standalone MOSFET

This section discusses parasitic oscillation and ringing of a MOSFET in switching applications. The oscillation and ringing of the gate voltage could cause false switching, increase power losses and lead to permanent damage of a MOSFET.
Major causes of the oscillation and ringing of a MOSFET are as follows:

(1) Forming of an oscillation circuit

An oscillation network is formed in a circuit and leads to parasitic oscillation of a MOSFET.

(2) Surge voltage across the drain and source

The ringing voltage between the drain and the source during turn-off could return to the gate terminal through a positive feedback loop via the gate-drain capacitance C_{gd} and cause the gate voltage to oscillate.

(3) Source inductance

A voltage induced by the di/dt of the drain-source current during turn-off and the source lead and wire stray inductances could cause the gate-source loop of a MOSFET to go into LCR resonance. (Ringing induced by the source inductance)

Other factors could also cause oscillation and ringing, but stray inductance is of primary importance in using MOSFETs.

2. Forming of an oscillation network

2.1. Oscillation phenomenon

Oscillation is a phenomenon whereby an electronic circuit causes voltage and current vibration on its own without receiving vibration energy from an external source. In reality, since a circuit has electric resistance, oscillations decay with time unless the lost energy is supplied to the circuit.
The conditions for oscillation are:
(1) Phase condition

The feedback signal from the output to the input is in phase with the input signal at the oscillation frequency. (Positive feedback loop)

(2) Amplitude condition

The loss caused by passive elements in a circuit is lower than the gain obtained by an amplifier.

Oscillation occurs when a circuit has a positive feedback and provides a gain that compensates for a loss.

2.1.1. Feedback circuit (positive and negative feedback)

Figure 2.1 shows a feedback circuit (in which part of the output is fed back to the input).

v_i = input voltage, v_o = output voltage, A = loop gain, and H: feedback factor

v_1 = input voltage applied to the amplifier, v_2 = feedback voltage

The open-loop gain G_O of this circuit must be calculated to verify its operation. For this purpose, the feedback loop is usually cut as shown in Figure 2.2.

G_o is calculated as follows:

Since $v_2=AHv_1$

$G_O=v_2/v_1=AH$

The loop gain in a feedback system (called closed-loop gain, G_C) can be expressed as follows using $G_O=AH$:

$v_o=A \cdot v_1$ (1)

$v_1=v_i+H \cdot v_o$ (2)

From Equations (1) and (2),

$v_o=A(v_i+H \cdot v_o)$

$=[A/(1-AH)]v_i$ (3)

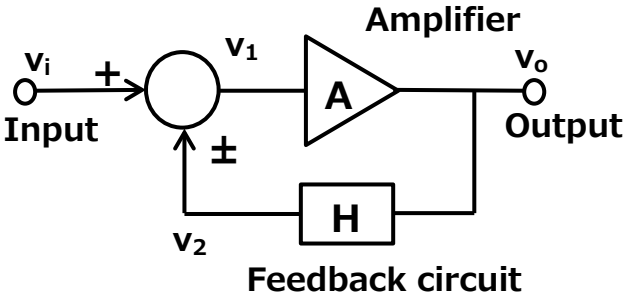

Figure 2.1 Feedback circuit

From this equation, the overall gain of the circuit is calculated as:

$G_C=v_o/v_i=A/(1-AH)$ (4)

Equation (4) shows that a positive feedback loop is created when AH is positive and that a negative feedback loop is created when AH is negative.

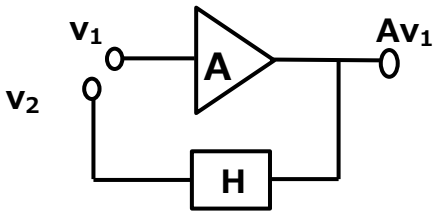

Figure 2.2 Loop gain

2.1.2. Conditions for oscillation

A positive feedback loop becomes unstable and oscillates when it has a gain AH of 1 or greater.

Therefore, a positive feedback loop is not generally used in amplifiers; it is commonly used in oscillators (such as Wien bridge oscillators, Colpitts oscillators and Hartley oscillators).
Here, let's confine our discussion to positive feedback loops. Then, when AH=1 in Equation (4), G_C becomes infinite, causing a feedback circuit to go into oscillation.

The loop gain AH of a positive feedback loop in an oscillator is expressed using a complex number. In a complex number $a + bi$, a is the real part and b is the imaginary part. Let the real part be Re(AH) and the imaginary part be Im(AH). Then, the conditions for oscillation are:

$$AH=Re(AH)+jIm(AH)$$
$$Re(AH)\geq 1$$

2.2. MOSFET oscillation

Power MOSFETs have a large transconductance g_m and parasitic capacitances. Therefore, wire and other stray inductances (inductances between the gate, source, and drain circuits and in the associated interconnects) could form a positive feedback circuit, causing parasitic oscillation.

The oscillating voltage could produce voltage overshoot on the positive feedback loop and the gate, leading to permanent damage of the MOSFET.

When a power MOSFET is in the steady on or off state, parasitic oscillation does not occur because its transconductance g_m becomes zero or negligibly small. A power MOSFET is susceptible to parasitic oscillation: **1) when its load is short-circuited; and 2) during transient switching periods in which g_m becomes large**. Since the MOSFET is operating in linear mode (i.e., v_{DS} and i_D are being applied simultaneously), a positive feedback path can be formed by electromagnetic induction, parasitic capacitance and other factors. MOSFETs with a high g_m go into parasitic oscillation when their loop gain is 1 or greater.

2.2.1. MOSFET feedback loop

Oscillation does not occur without a feedback loop. The following paragraphs discuss the conditions necessary for oscillation to occur, using a circuit shown in Figure 2.3. Assuming that X_1 to X_3 are the ideal reactances, their losses can be ignored. In this case, current i is considered not to flow from the MOSFET to each reactance. Therefore, the circuit of Figure 2.3 can be approximated as shown in Figure 2.4.

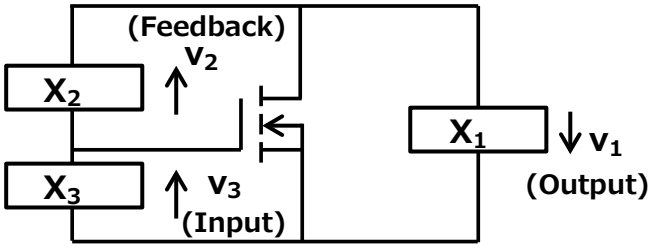

Figure 2.3 Schematic of an oscillation model

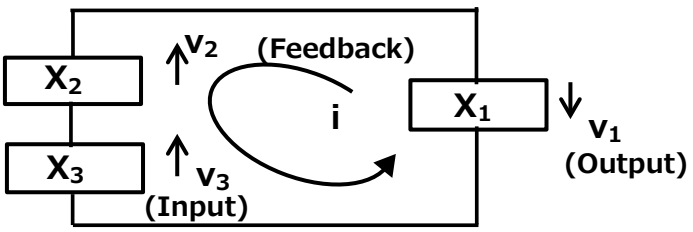

Figure 2.4 Current flowing through the oscillation circuit

According to Kirchhoff's circuit laws,

$$v_1+v_2+v_3=i(X_1+X_2+X_3)=0$$

Here, $i \neq 0$.

Hence, $X_1+X_2+X_3=0$

There is a positive feedback loop when the circuit is oscillating. This means that v_3 (input) is in phase with v_1 (output) in Figure 2.3 and Figure 2.4. Therefore, X_3 and X_1 are reactances of the same property; X_2 is not.

Typical oscillators include Colpitts oscillators (Figure 2.5) and Hartley oscillators (Figure 2.6).

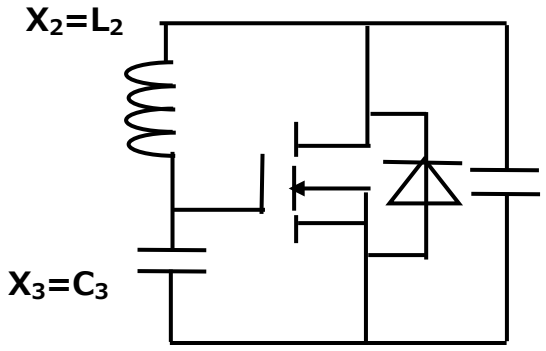

Figure 2.5 Colpitts oscillator

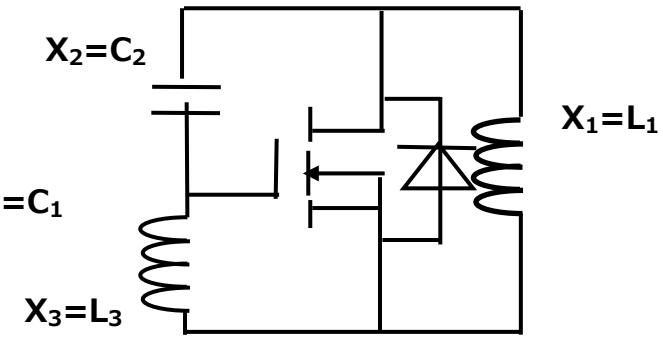

Figure 2.6 Hartley oscillator

2.2.2. Colpitts oscillators

Figure 2.7 shows basic Colpitts oscillators.

The equivalent circuit model of Colpitts oscillators is shown in Figure 2.8. Its oscillation frequency and the gain ($g_m \cdot r_d$) necessary to sustain oscillation can be determined by calculating a loop gain. Since the gate current is zero, the wire from v_2 to v_1 can be ignored.

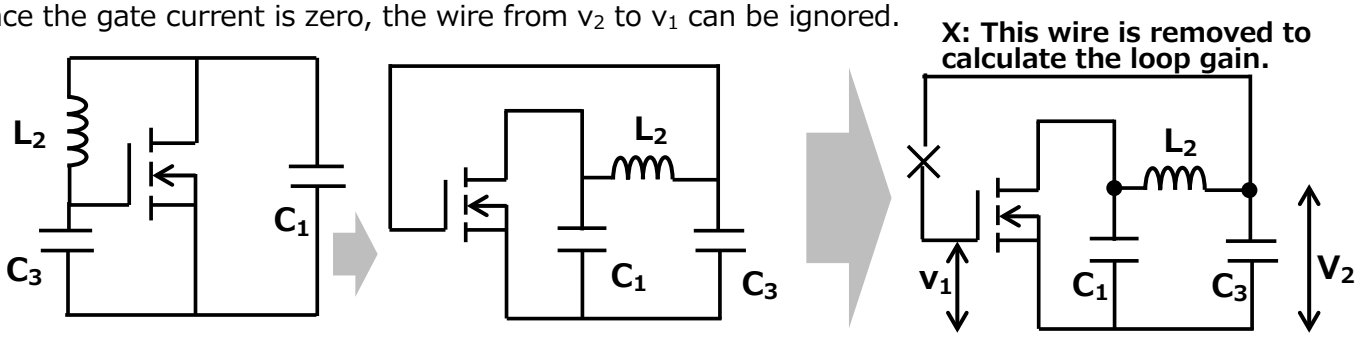

Figure 2.7 Basic Colpitts oscillators

$$v_2 = (-g_m \cdot v_1)\frac{1}{\frac{1}{r_d}+j\omega C_1+\frac{1}{j\omega L_2+\frac{1}{j\omega C_3}}} \times \frac{\frac{1}{j\omega C_3}}{j\omega L_2+\frac{1}{j\omega C_3}}$$

$$= (-g_m \cdot v_1)\frac{r_d}{1-\omega^2 L_2 C_3+j\omega(C_1+C_3-\omega^2 L_2 C_1 C_3)r_d}$$

$$AH = \frac{v_2}{v_1} = \frac{-g_m \cdot r_d}{1-\omega^2 L_2 C_3+j\omega(C_1+C_3-\omega^2 L_2 C_1 C_3)r_d} \qquad (6)$$

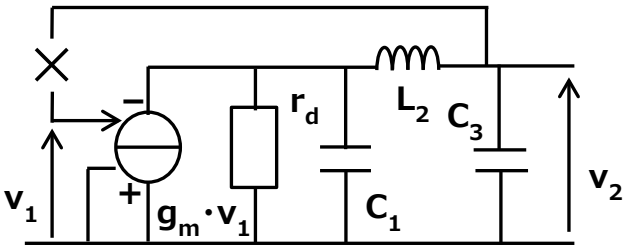

Figure 2.8 Equivalent circuit of a Colpitts oscillator

From this equation, the oscillation frequency and the gain can be calculated as follows:

Oscillation frequency

Im(AH)=0

The Colpitts oscillator is most susceptible to oscillation at a frequency at which the phase of a signal that has looped around the circuit once is delayed by 0° or 360°. Hence,

$C_1 + C_3 - \omega^2 L_2 C_1 C_3 = 0$ (By dividing both sides of the equation by $j\omega C_1 j\omega C_3$, $1/j\omega C_1 + 1/j\omega C_2 + j\omega L_2 = 0$ is obtained.)

$$\omega^2 = \frac{C_1 + C_3}{L_2 C_1 C_3} \quad (7) \qquad \omega = \sqrt{\frac{C_1 + C_3}{L_2 C_1 C_3}} \quad (8)$$

Gain: Substituting Equation (7), $\omega^2 = (C_1+C_2)/L_2C_1C_3$, into $Re(AH) \geq 1$:

$$\frac{-g_m \cdot r_d}{1 - \frac{C_1 + C_3}{L_2 C_1 C_3} L_2 C_3} = \frac{g_m \cdot r_d}{\frac{C_3}{C_1}} \geq 1 \qquad \therefore g_m \cdot r_d \geq \frac{C_3}{C_1} \quad (9)$$

($g_m \cdot r_d$: Voltage loop gain)

2.2.3. Hartley oscillators

Figure 2.9 shows basic Hartley oscillators.

As is the case with Colpitts oscillators, the oscillation frequency of a Hartley oscillator and the gain ($g_m \cdot r_d$) necessary to sustain oscillation can be determined by calculating a loop gain. The equivalent circuit of Hartley oscillators is shown in Figure 2.10.

$$\omega = \frac{1}{\sqrt{(L_1 + L_3)C_2}} \quad (10) \qquad g_m \cdot r_d \geq \frac{L_1}{L_3} \quad (11)$$

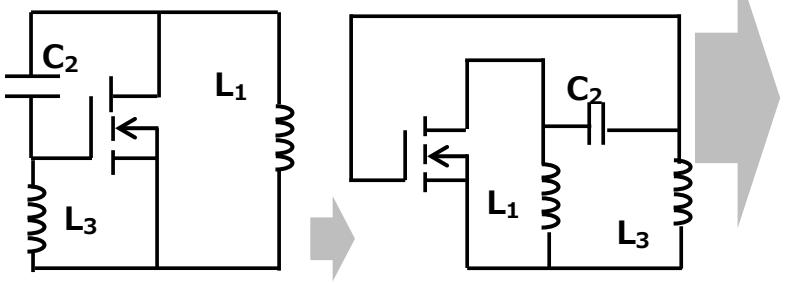

Figure 2.9 Basic Hartley oscillators

X: This wire is removed to calculate the loop gain.

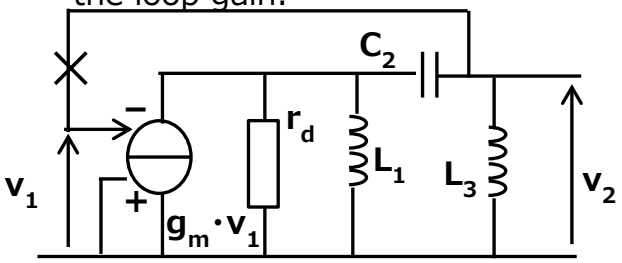

Figure 2.10 Equivalent circuit of a Hartley oscillator

2.3. Parasitic oscillation of MOSFETs for switching applications (standalone MOSFET operation)

As described above, when a power MOSFET is in the steady on or off state, parasitic oscillation does not occur because its transconductance g_m becomes zero or negligibly small.

When a MOSFET switches a resistive load, the circuit connected to the drain terminal has a low Q factor* (quality factor). Because of a low loop gain at the parasitic oscillation frequency, a typical parasitic oscillation does not occur. When a MOSFET switches an inductive load, a parasitic oscillation circuit might be formed. However, a positive feedback loop necessary for parasitic oscillation is not formed when a freewheel diode is off.

Suppose that the freewheel diode (FWD) in the equivalent circuit shown in Figure 2.11 is off. Then, since an inductive load does not conduct a current at the parasitic oscillation frequency, the equivalent circuit can be approximated as shown in Figure 2.12 by ignoring the internal inductances of the MOSFET. Note that this circuit consists of only stray inductances of the gate and source wires and internal parasitic capacitances of the MOSFET. The LC tank consisting of the capacitor C_{gs} and the

inductor L_1 becomes capacitive or inductive, depending on the frequency as shown in Figure 2.13 and Figure 2.14, neither of which has a positive feedback loop. Therefore, they are not susceptible to parasitic oscillation (see Section 2.2.1, "MOSFET feedback loop," for positive feedback loops).

* Q factor: Applicable to resonant circuits consisting of inductors and capacitors

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

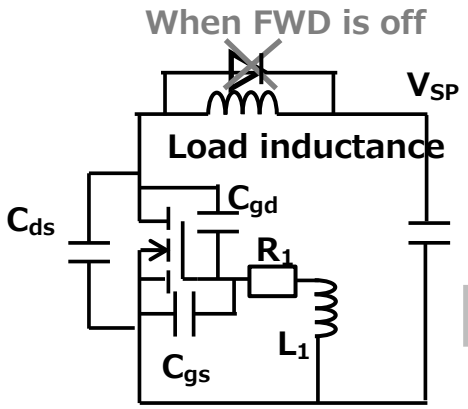

Figure 2.11
FWD conduction circuit

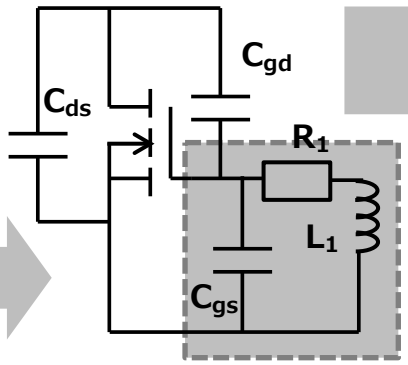

Figure 2.12
Equivalent circuit

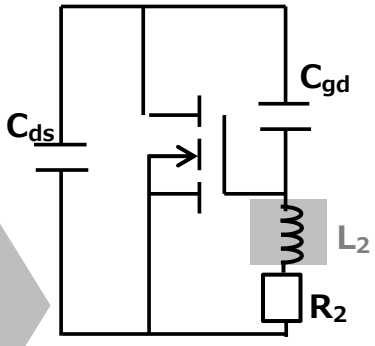

Figure 2.13
Equivalent circuit (a)

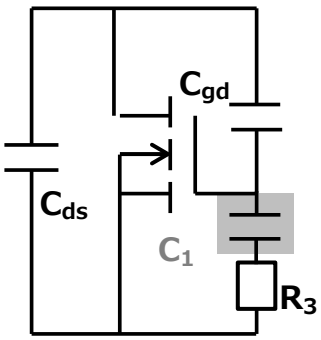

Figure 2.14
Equivalent circuit (b)

2.3.1. Parasitic oscillation circuits (parasitic oscillation loops)

When the following conditions are met, a parasitic oscillation loop (i.e., a loop that conducts a signal at the oscillation frequency) is formed across the drain and source terminals, making a MOSFET susceptible to oscillation.

① The freewheel diode is in conduction (i.e., when it is forward biased or during reverse recovery).

When a freewheel diode is in conduction, a drain-source current passes the capacitor C_1 between V_{DD} and GND, bypassing a reactor load. Therefore, a parasitic oscillation loop is formed.

② The load is short-circuited.

When the load is short-circuited, the drain and source terminals of the MOSFET are connected via the capacitor C_1 between V_{DD} and GND. As a result, a parasitic oscillation loop is formed as shown by the dashed line in Figure 2.16.

③ There is a large parasitic capacitance C_2 between the drain and the source.

If there is a large parasitic capacitance C_2 between the drain and the source due to multilayer wiring in a laminated printed circuit board, a parasitic oscillation loop is formed as shown by the dashed line in Figure 2.17. Then, all conditions for parasitic oscillation are met.

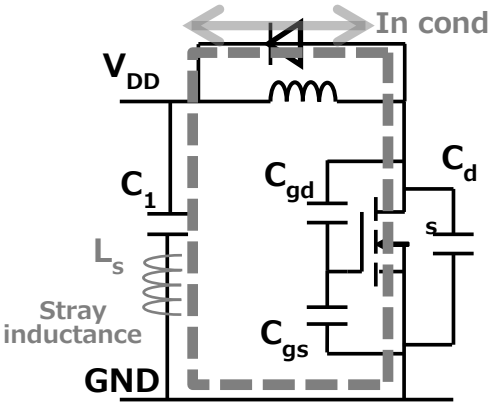

Figure 2.15
① FWD in conduction

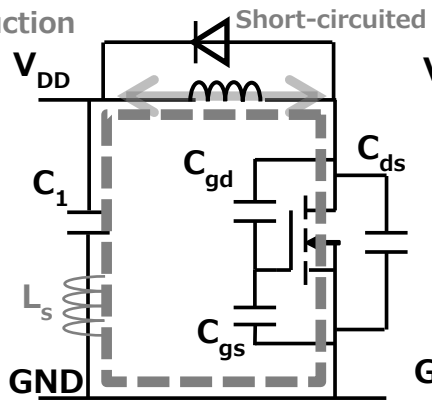

Figure 2.16
② Short-circuited load

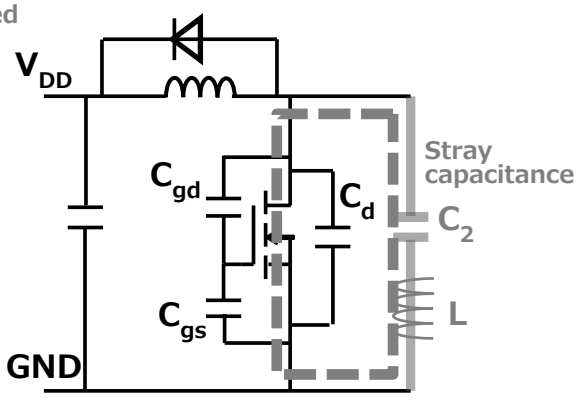

Figure 2.17
③ Parasitic capacitance between drain and source

Since the capacitor C_1 in Figure 2.15 and Figure 2.16 and C_2 in Figure 2.17 are large, they can be considered to be in a current conduction path at the parasitic oscillation frequency. Figure 2.18 shows an equivalent circuit. In reality, this circuit has a resistance R_1 of the gate circuit and a parasitic inductance L_1 of the gate wire. Figure 2.19(a) shows an equivalent circuit, with the gate circuit added.

In Figure 2.19(a), if the impedance of C_3 (i.e., C_1 in Figure 2.15 and Figure 2.16 and C_2 in Figure 2.17) is sufficiently low at the parasitic oscillation frequency, C_3 can be considered to be short-circuited. At this time, the equivalent circuit can be remodeled as shown in Figure 2.19(b). The ratio of L_{s1} and L_{s2} varies according to the position of the drain-source path to which the gate is connected. Either C_{gd} or C_{gs} forms a parallel resonant circuit with L_1, depending on the L_{s1}/L_{s2} ratio.

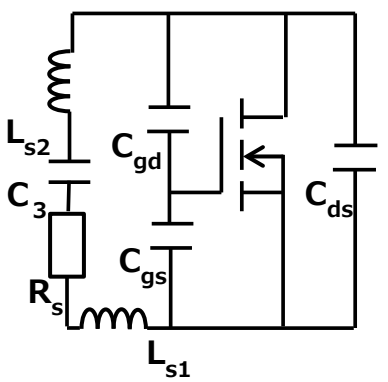

Figure 2.18 Equivalent circuit

(a) With a gate circuit added

(b) Circuit model at the parasitic oscillation frequency

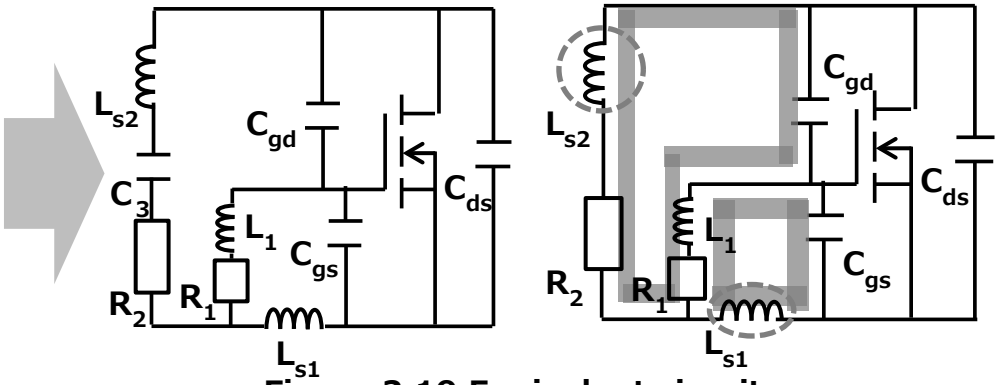

Figure 2.19 Equivalent circuits with a gate circuit added

L_{s1}, L_{S2}: The parasitic inductances L_{s1} and L_{S2} are the equivalent series inductance (ESL) of the capacitor between V_{DD} and GND and the parasitic inductance of the drain-source wire.

R_2: R_2 is the on-resistance of the freewheel diode and the equivalent series resistor (ESR) of the capacitor between V_{DD} and GND

When the source wire inductance L_{s1} is larger than the drain wire inductance L_{s2} in Figure 2.19(b), the gate is connected to the drain, not the source, at the parasitic oscillation frequency. Figure 2.20 shows this equivalent circuit.

For the circuit of Figure 2.20 to form a resonant circuit, Resonant Circuit #1 formed by L_1 and C_{gd} must be inductive at the parasitic oscillation frequency ω_{OSC}, and Resonant Circuit #2 formed by C_{ds} and L_s must be capacitive at ω_{OSC}.

In this case, the equivalent circuit can be remodeled as shown in Figure 2.21, which is basically a Colpitts oscillator.

The gate resistor R_1 and the drain resistor R_2 have been converted to the drain-source resistance of a MOSFET as represented by R_3 in Figure 2.21. L_2 is an inductance in Resonant Circuit #1, and C_4 is a capacitance in Resonant Circuit #2.

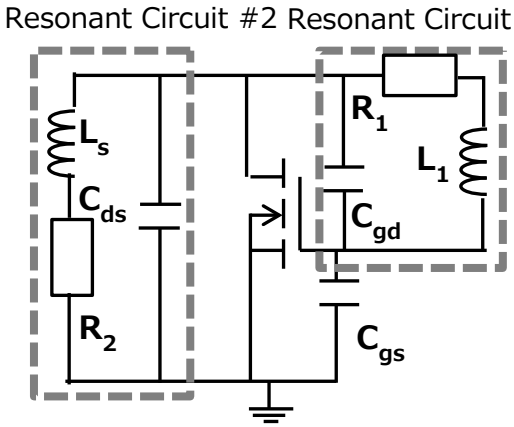

Figure 2.20 Equivalent circuit

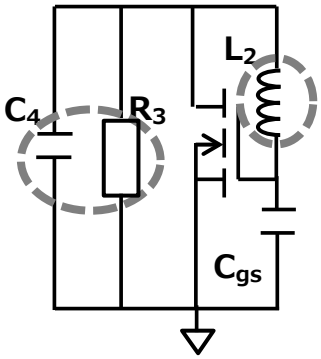

Figure 2.21 Equivalent circuit model for parasitic oscillation

This section has discussed a situation where the source wire inductance L_{s1} is larger than the drain wire inductance L_{s2} in Figure 2.19. In contrast, when the source wire inductance L_{s1} is smaller than the drain wire inductance L_{s2}, a resonant circuit is formed between the gate and the source. If this resonant circuit becomes inductive and the resonant circuit between the drain and the source becomes inductive, a Hartley oscillator is formed. In this case, the circuit in Figure 2.19 might also oscillate.

2.3.2. Condition for parasitic oscillation

When a Colpitts oscillator is formed (See Equation (9) in Section 2.2.2, “Colpitts oscillators.”)

The circuit shown in Figure 2.21 goes into oscillation when it has a loop gain of 1 or greater. The condition for parasitic oscillation is expressed as:

$$g_m \cdot R_3 \cdot C_4/C_{gs} \geq 1$$

Hence, $g_m \geq (C_{gs}/C_4)/R_3$

where, R_3 is the equivalent drain-source resistance.

Substituting C_{ds} for C_4, the following equation is obtained:

$$\mathbf{g_m \geq (C_{gs}/C_{ds})/R_3} \qquad (12)$$

Parasitic oscillation occurs when this equation is met.

2.4. Mitigating parasitic oscillation

· A Colpitts oscillator is not formed when the wire inductances shown in Figure 2.19(a) satisfy $L_{s1}<L_{s2}$.

(The assumption is that a Hartley oscillator is not formed.)

· Equation (12) shows that a MOSFET with a large C_{gs}/C_{ds} ratio is less susceptible to parasitic oscillation.

· The gate resistance R_1 and the drain resistance R_2 shown in Figure 2.20 can be replaced with the drain resistance R_3 as shown in Figure 2.21. Generally, increasing R_1 decreases R_3. Therefore, this makes parasitic oscillation less likely to occur due to a loop gain.

3. Voltage ringing induced by the drain inductance

The di/dt of the drain current during turn-off and the stray inductances of the drain terminal and the connected wire cause a voltage surge across the drain and the source. The surge voltage is fed back to the gate terminal of a MOSFET and might cause ringing of the gate voltage. A large ringing voltage superimposed on the gate voltage might cause the MOSFET to turn on and off repeatedly, leading to oscillation of the MOSFET.

3.1. Mechanism

When the MOSFET in the circuit shown in Figure 3.1 turns off, the di/dt of the drain current and the stray inductances of the drain lead and wire cause a voltage surge across the drain and the source. The surge voltage is expressed as:

$$V_{Surge}=L_{S2}\times di/dt \qquad (13)$$

Suppose that the diode in the drain-source loop is in conduction in the circuit shown in Figure 3.2 (i.e., energy from L is being recirculated). Then, the circuit causes ringing since the surge voltage resonates with the C_{ds} of the MOSFET and the stray inductance L_{S2}. (Since the impedance of C_1 is sufficiently low for parasitic oscillation frequency, it can be considered to be short-circuited.)

The surge voltage is superimposed on the v_{GS} voltage via the gate-drain capacitance C_{gd} of the MOSFET. As a result, it might also affect the gate inductance as shown in Figure 3.3, causing ringing of the gate voltage.

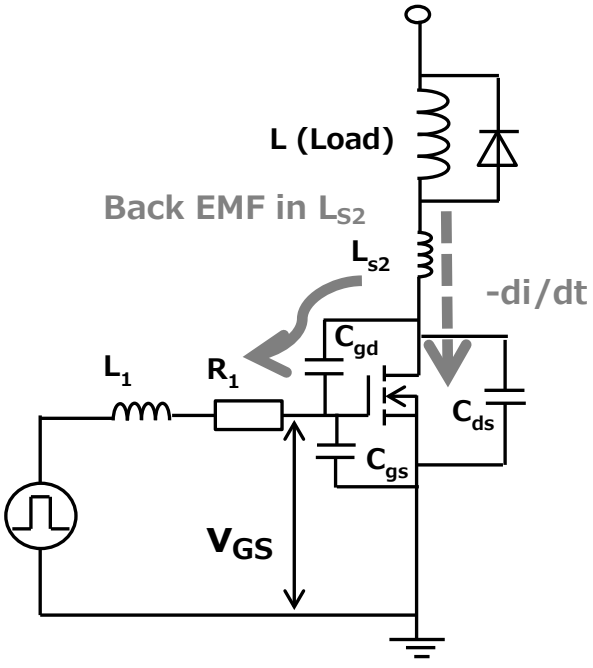

Figure 3.1 Occurrence of a voltage surge

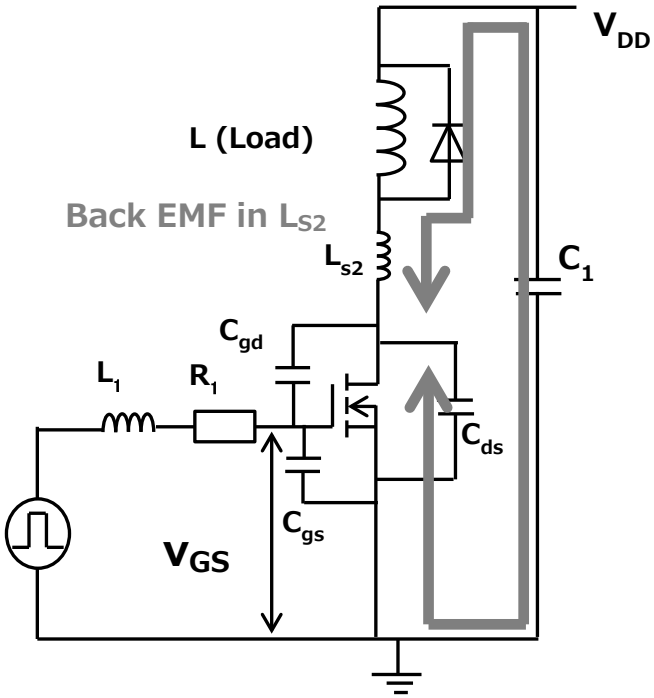

Figure 3.2 Drain-source resonance loop

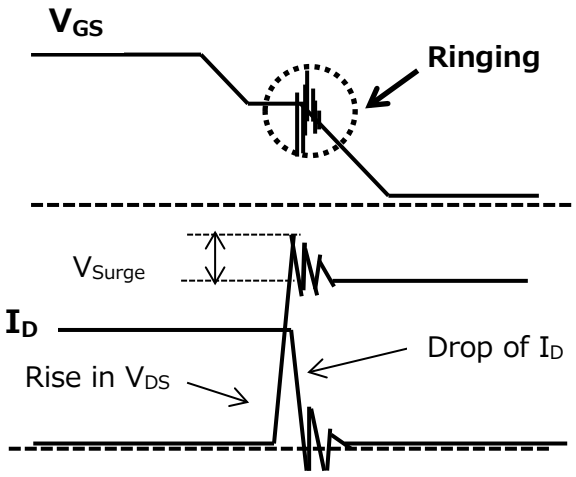

Figure 3.3 Ringing waveforms

3.2. Mitigating the ringing

In order to damp a surge voltage across the drain and source terminals, it is most important to reduce wire inductances. The amplitude of the surge voltage can also be reduced by increasing the gate resistance. In addition, the ringing of the gate voltage can be suppressed by reducing the gate stray inductance.

4. Voltage induced by the source lead and wire stray inductances

A voltage induced by the di/dt of the drain current during turn-off and the stray inductances of the source lead and wire cause LCR resonance of the gate-source loop of a MOSFET, leading to ringing of the gate voltage.

If a large ringing voltage is superimposed on the gate voltage, the MOSFET might turn on and off repeatedly, leading to oscillation of the MOSFET. The gate voltage V_{GS} that turns off the MOSFET decays and reaches the Miller period (during which V_{GS} is constant), causing the drain-source voltage V_{DS} to gradually increase. At the same time, the drain current I_D begins to decrease. (The energy of load L flows through the freewheel diode.) (Figure 4.2)

As V_{DS} of the MOSFET increases, the drain-source capacitance C_{ds} decreases. Therefore, a large voltage variation dv/dt is generated between drain and source of the MOSFET. Consequently, the current decreases sharply (i.e., the di/dt increases).

When there is a stray inductance L_{S1} on the source lead and wire, a back-EMF is generated at the source inductance by the di/dt:

$$V=L_{S1}\times di/dt \qquad (14)$$

The back-EMF voltage might cause ringing of the gate-source voltage.

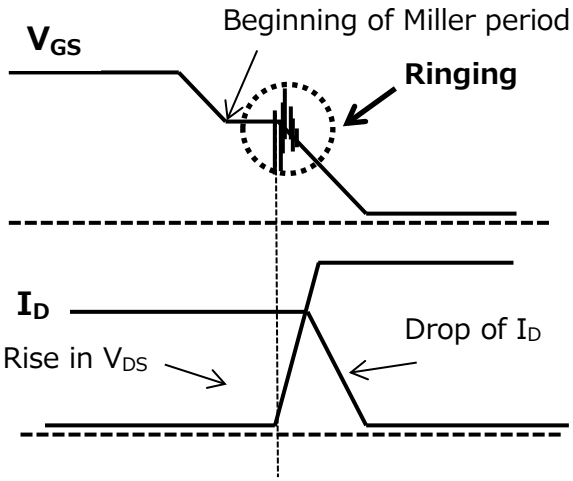

Figure 4.1 Ringing voltage

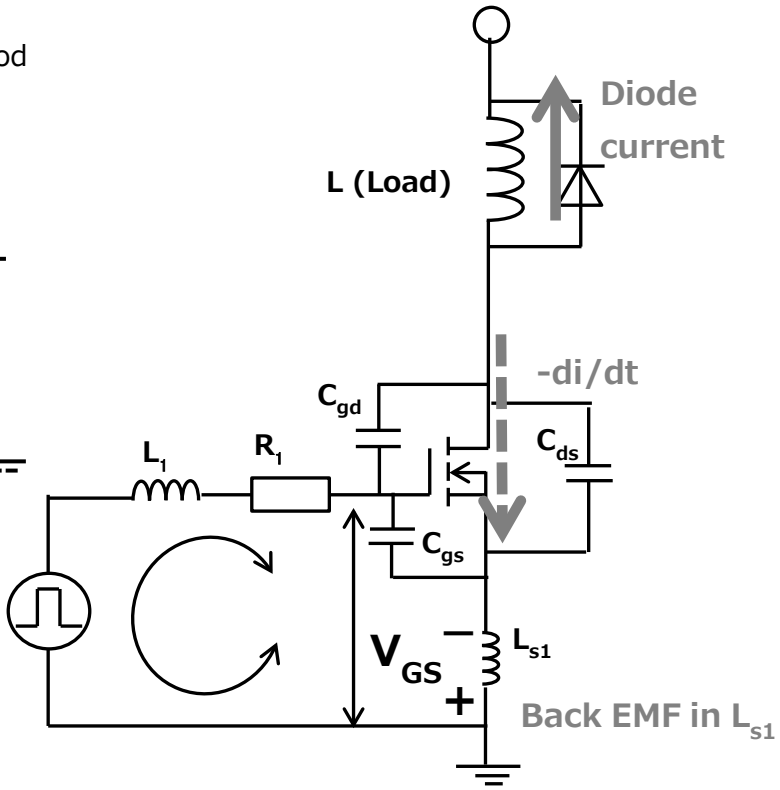

Figure 4.2. Circuit

4.1. Mitigating the ringing

In order to damp a surge voltage across the drain and source terminals, it is most important to reduce the stray inductances of the source lead and wire. The amplitude of the surge voltage can also be reduced by increasing the gate resistance R_1. In addition, ringing can be suppressed by reducing L_1.

5. Simulating and reducing oscillation and ringing of a MOSFET

We simulated to find out how the oscillation and ringing phenomena occur and how to mitigate them.

Since the purpose of this simulation was to investigate the phenomena, the actual component values to be used are different.

5.1. Oscillator

5.1.1. Oscillation phenomenon

The oscillation of a circuit shown in Figure 5.1 was analyzed using the following component values. These are component values that caused oscillation. In order to simulate oscillation, the gate stray inductance L_1 and the gate resistance were intentionally set to zero.

Drain stray inductance L_{S2}=20 nH

Source stray inductance: L_{S1}=20 nH

Gate stray inductance L_1=0 nH

Gate resistance R_1=0 Ω

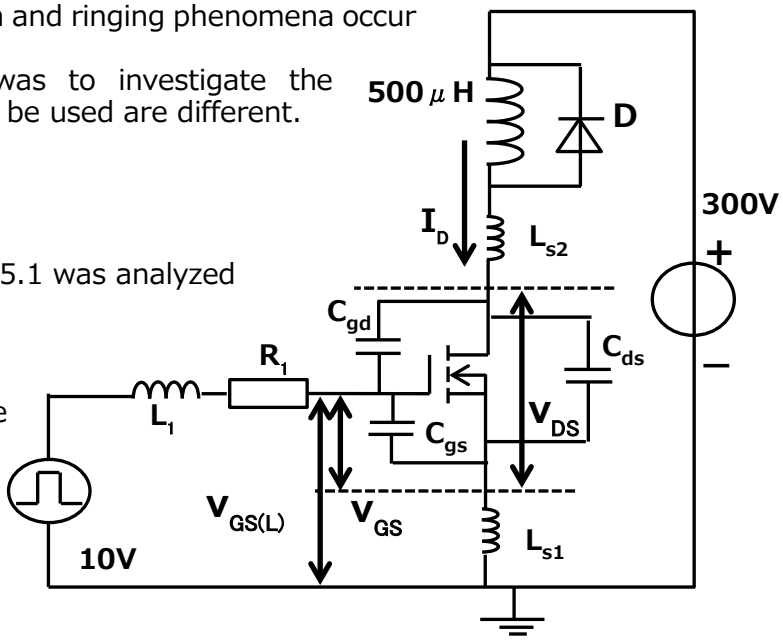

Figure 5.1 Test circuit for oscillation

Figure 5.2 shows the waveforms of the gate voltage, drain voltage and drain current of the MOSFET.

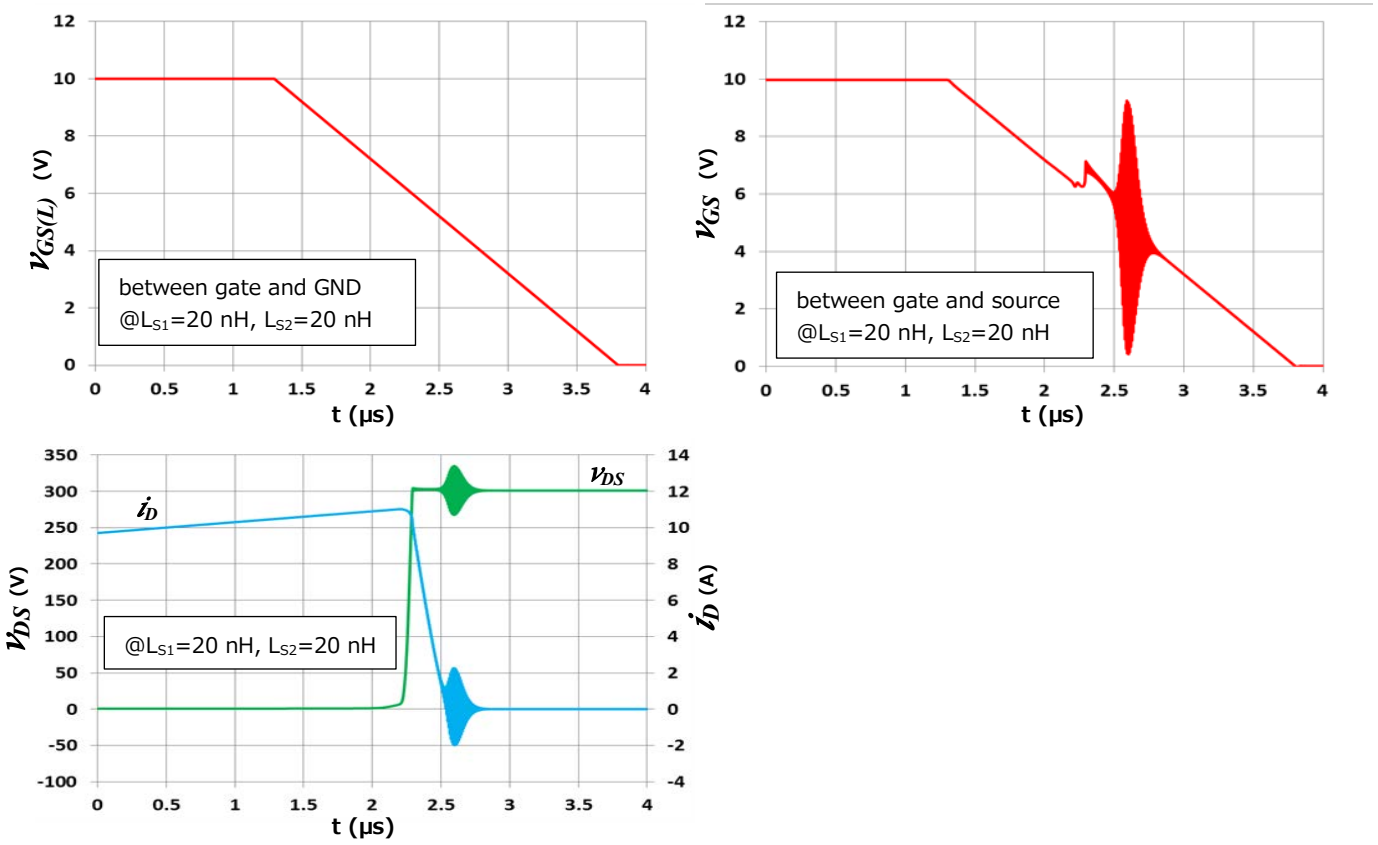

Figure 5.2 Oscillation waveforms

5.1.2. Mitigating oscillation

As described in Section 2.4, "Mitigating parasitic oscillation," in order to prevent the forming of a Colpitts oscillator, it is most important to ensure that wire inductances satisfy the following relationship: $L_{s1} < L_{s2}$.

As another solution, our simulation showed that changing the gate resistance and gate inductance also helps mitigate MOSFET oscillation.

(1) Increasing the gate resistance

We changed the gate resistor value in Figure 5.1. Figure 5.3 shows the simulation results. Increasing the gate resistor value R_1 helped mitigate the oscillation compared with the waveforms of Figure 5.2.

The gate resistance R_1 was changed from 0 Ω to 10 Ω.

L_{S1}=20 nH, L_{S2}=20 nH, L_1=0 nH

(2) Increasing the gate stray inductance

We increased the gate stray inductance in Figure 5.1. Figure 5.4 shows the simulation results. Increasing the gate stray inductance L_1 helped mitigate the oscillation compared with the waveforms of Figure 5.2.

The gate stray inductance L_1 was increased from 0 nH to 20 nH.

Gate resistance R_1=0 Ω, L_{S1}=20 nH, L_{S2}=20 nH,

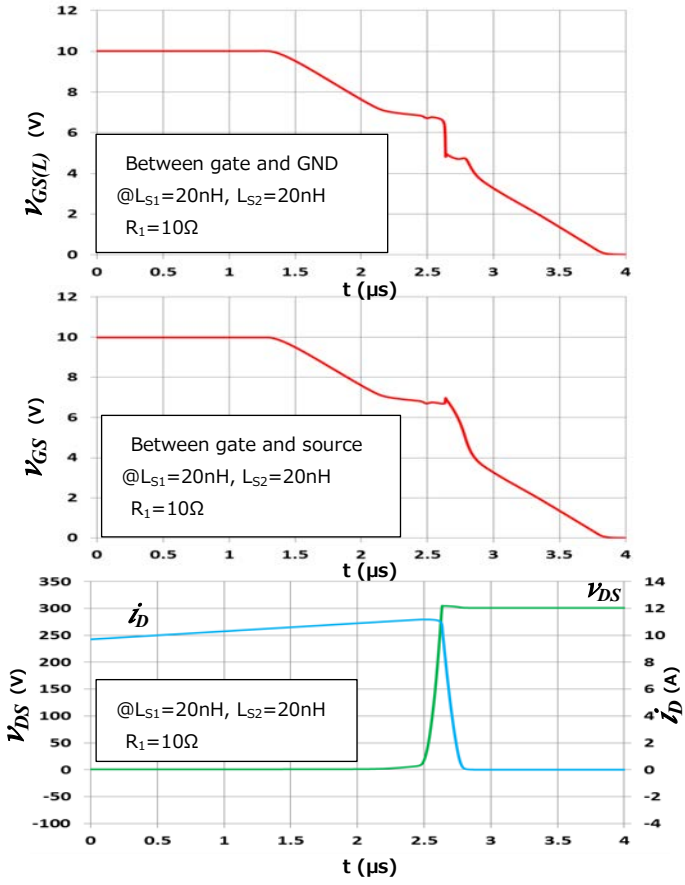

Figure 5.3 Waveforms with the increased R_1

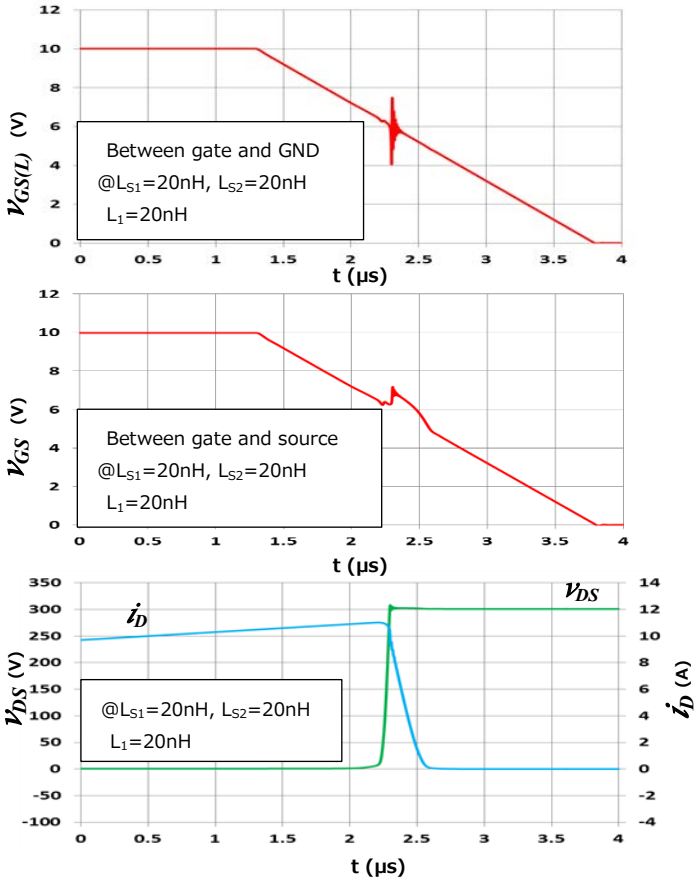

Figure 5.4 Waveforms with the increased L_1

5.2. Ringing caused by drain stray inductance

5.2.1. Ringing simulation

We analyzed the effect of the drain stray inductance on ringing.

As described in Section 3, "Voltage ringing induced by the drain inductance," a surge voltage induced by the stray inductance of the drain of a MOSFET is superimposed on the gate voltage via the gate-drain capacitance C_{gd}, and then it causes the ringing of the gate voltage.

The ringing of a circuit shown in Figure 5.5 was simulated using the following component values:

Drain stray inductance L_{S2}=200 nH

Gate stray inductance L_1=100 nH

Gate resistance R_1=1 Ω

Figure 5.6 shows the waveforms of the gate voltage, drain voltage and drain current of the MOSFET.

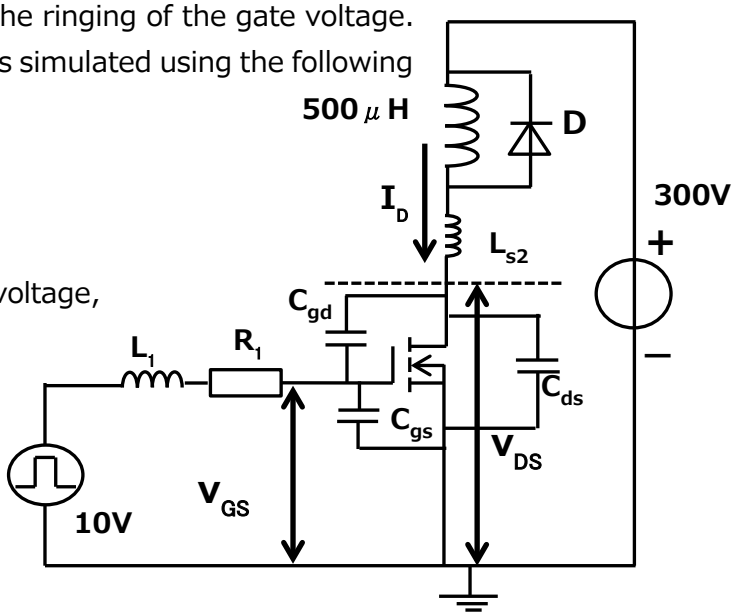

Figure 5.5 Test circuit for the gate voltage ringing caused by the drain inductance

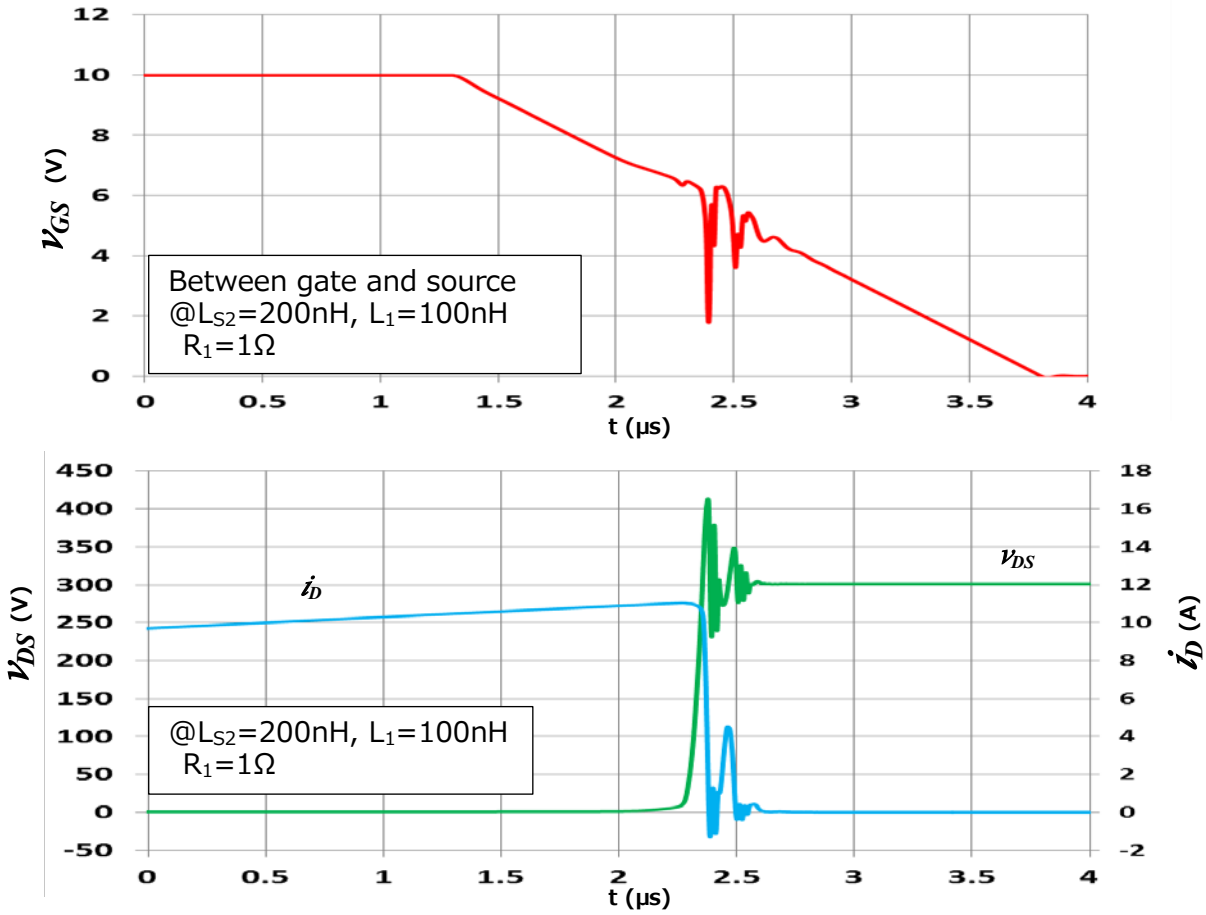

Figure 5.6 Ringing waveforms

5.2.2. Mitigating the ringing

As described in Section 3.2, "Mitigating the ringing," the most important thing is to reduce the drain stray inductance.

As another solution, our simulation showed that changing the gate resistance and gate inductance also helps mitigate the ringing caused by the drain stray inductance.

(1) Increasing the gate resistance

We changed the gate resistor value in Figure 5.5. Figure 5.7 shows the simulation results. Increasing the gate resistor value R_1 helped mitigate the ringing compared with the waveforms of Figure 5.6.

The gate resistance R_1 was increased from 1 Ω to 10 Ω.

L_{S2}=200 nH, L_1=100 nH

(2) Reducing the gate stray inductance

We reduced the gate stray inductance in Figure 5.5. Figure 5.8 shows the simulation results. Reducing the gate stray inductance L_1 helped mitigate the ringing compared with the waveforms of Figure 5.6.

The gate stray inductance L_1 was reduced from 100 nH to 10 nH.

L_{S2}=200 nH, R_1=1 Ω

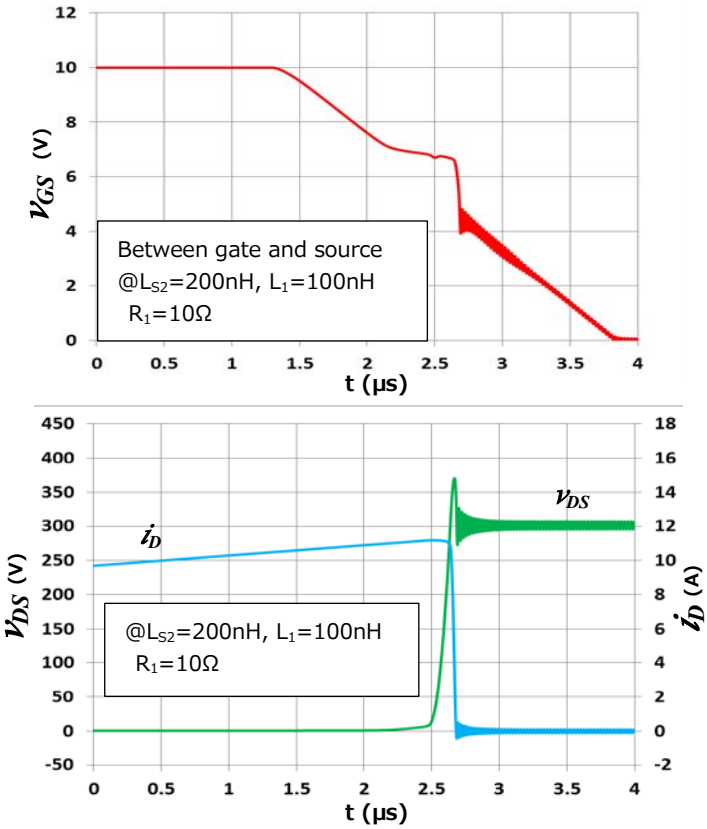

Figure 5.7 Waveforms with the increased R_1

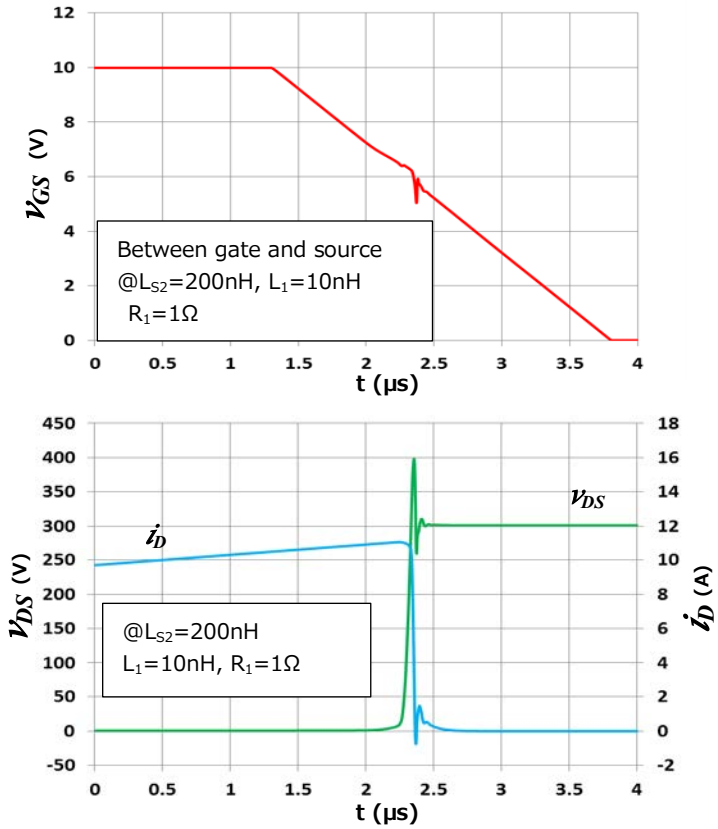

Figure 5.8 Waveforms with the reduced L_1

5.3. Ringing caused by the source lead and wire stray inductances

5.3.1. Ringing simulation

We analyzed the effect of the source and surrounding inductances on ringing.

As described in Section 4, "Voltage induced by the source lead and wire stray inductances," a voltage induced by the source stray inductance L_{s1} caused the ringing of the gate-source loop of a MOSFET due to the stray inductance of the gate wire L_1 and the gate-source capacitance C_{gs}.

The ringing was simulated with the following component values:

Source stray inductance: L_{S1}=20 nH
Gate stray inductance L_1=50 nH
Gate resistance R_1=1 Ω

Figure 5.10 shows the waveforms of the gate voltage, drain voltage and drain current of the MOSFET.

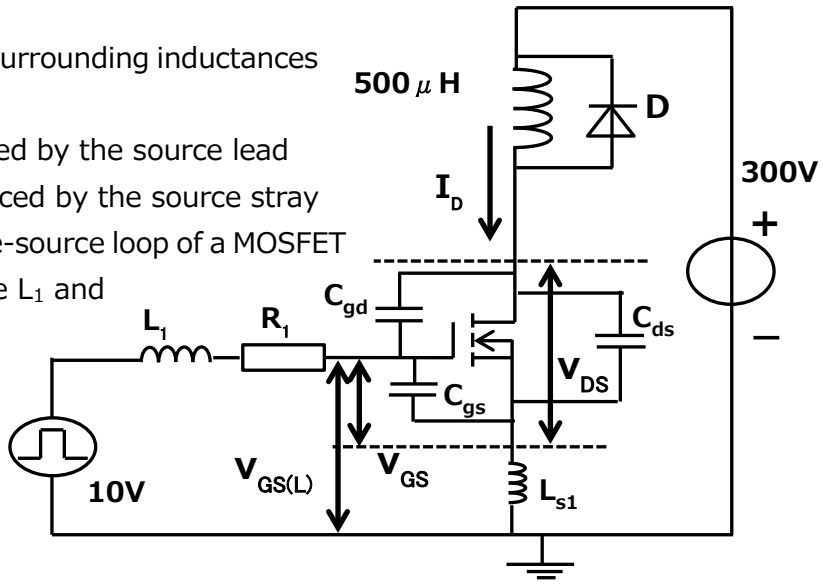

Figure 5.9 Test circuit for gate voltage ringing caused by the source inductance

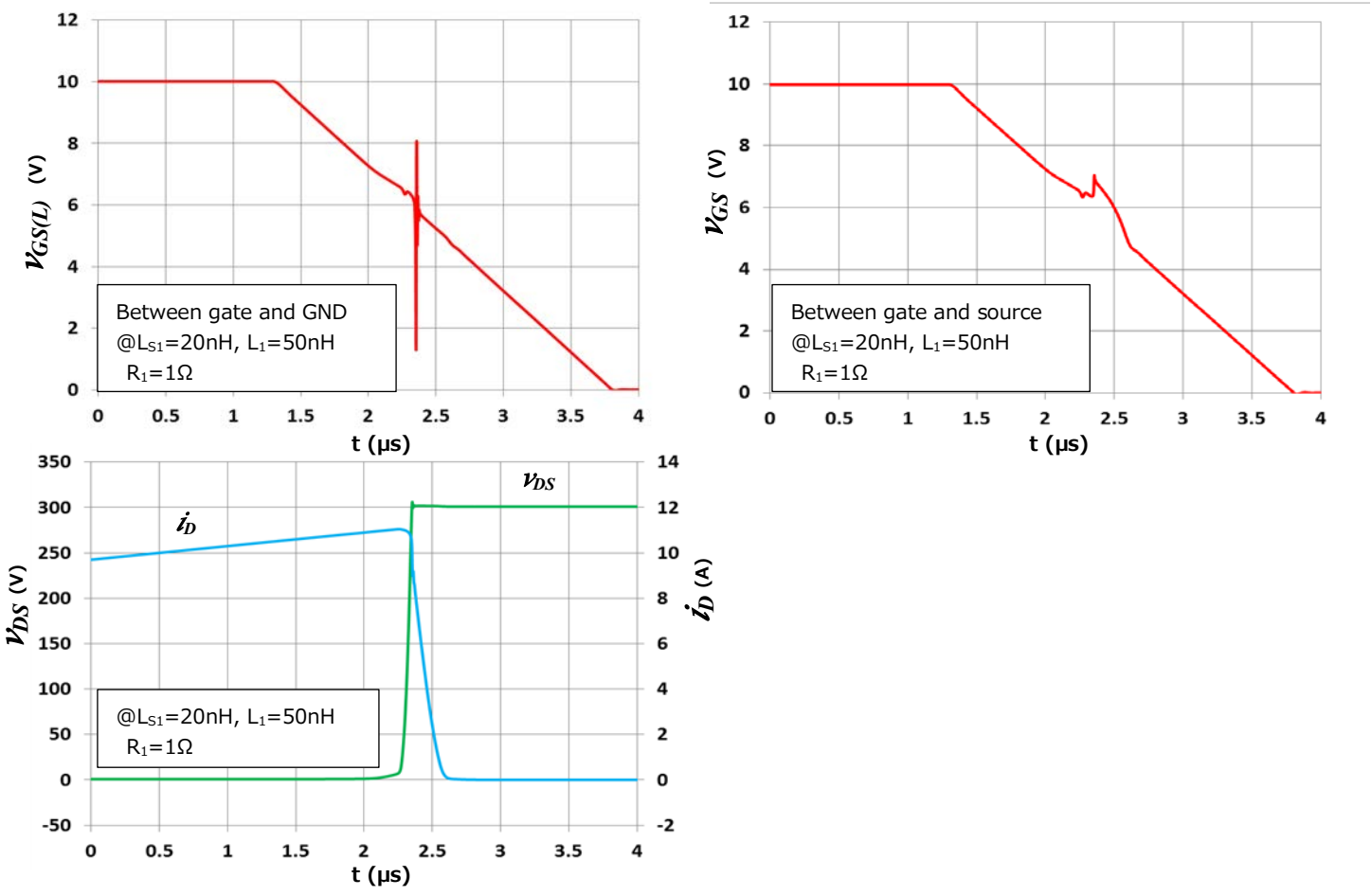

Figure 5.10 Ringing waveforms

5.3.2. Mitigating the ringing

As described in Section 4.1, "Mitigating the ringing," the most important thing is to reduce the source stray inductance.

Our simulation showed that changing the gate resistance and gate inductance also helps mitigate the ringing caused by the source stray inductance.

(1) Increasing the gate resistance

We changed the gate resistor value in Figure 5.9. Figure 5.11 shows the simulation results. Increasing the gate resistor value R_1 helped mitigate the ringing compared with the waveforms of Figure 5.10.

The gate resistance R_1 was changed from 1 Ω to 10 Ω.

L_{S1}=20 nH, L_1=50 nH

(2) Reducing the gate stray inductance

We reduced the gate stray inductance in Figure 5.9. Figure 5.12 shows the simulation results. Reducing the gate stray inductance L_1 helped mitigate the ringing compared with the waveforms of Figure 5.10.

The gate stray inductance L_1 was reduced from 50 nH to 10 nH.

L_{S1}=20 nH, R_1=1 Ω

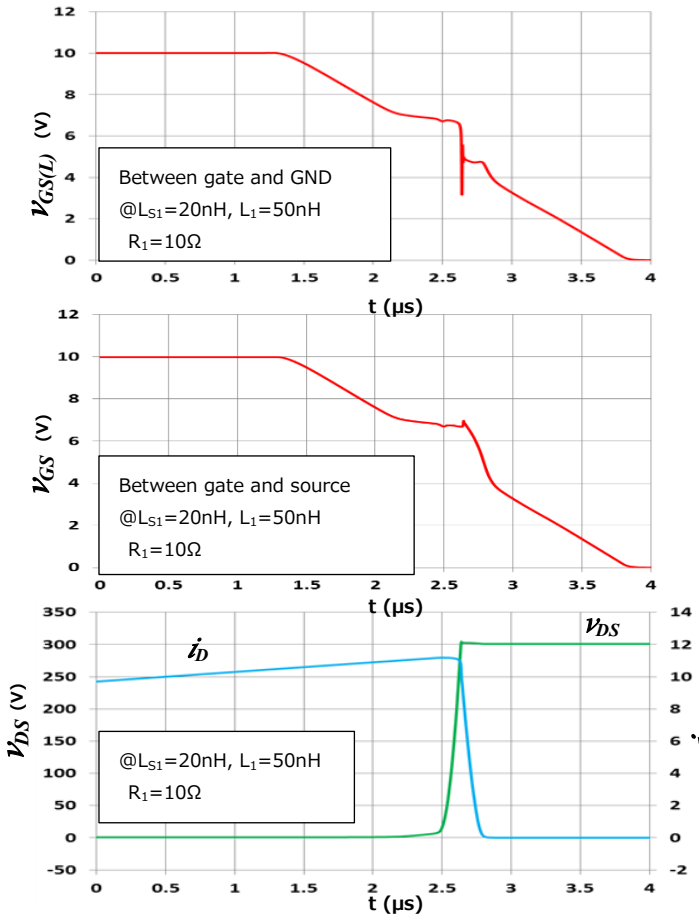

Figure 5.11 Waveforms with the increased gate resistance R_1

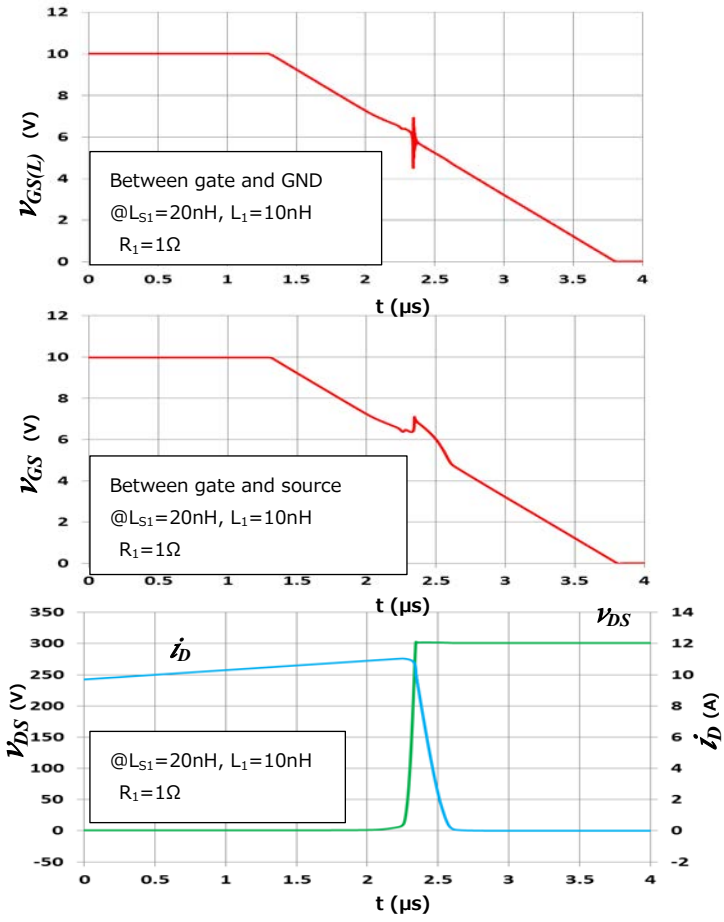

Figure 5.12 Waveforms with the reduced gate stray inductance L_1

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