32-Bit RISC Microcontroller

TMPM3H Group(1)

Reference Manual
Product Information
(PINFO-M3H(1))

Revision 2.2

2019-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related document

Document name	IP Symbol
Input / Output Ports (TMPM3H Group(1))	PORT-M3H(1)
Memory Map (TMPM3H Group(1))	MMAP-M3H(1)
Exception (TMPM3H Group(1))	EXCEPT-M3H(1)
Clock Control and Operation Mode (TMPM3H Group(1))	CG-M3H(1)-D
Power Supply and Reset Operation (TMPM3H Group(1))	RESET-M3H(1)
Clock Selective Watchdog Timer	SIWDT-A
Oscillation Frequency Detector	OFD-A
Debug Interface	DEBUG-A
Flash Memory	FLASH128_32-A
DMA Controller	DMAC-B
Programmable Motor Control Circuit plus	PMD+ -A
Advanced Encoder Input Circuit	A-ENC-A
12-bit Analog to Digital Converter	ADC-A
8-bit Digital to Analog Converter	DAC-A
Voltage Detection Circuit	LVD-A
32-bit Timer Event Counter	T32A-B
Real Time Clock	RTC-A
Asynchronous Serial Communication Circuit	UART-C
I^2C interface	I2C-B
Serial Peripheral Interface	TSPI-B
Remote Control Signal Preprocessor	RMC-A
Digital Noise Filter Circuit	DNF-A
Boundary scan	BSC-A
Trimming Circuit	TRM-A

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

The Flash memory uses the Super Flash® technology under license from Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviation

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
BSC	Poboundary-Scan
DAC	Digital to Analog Converter
DNF	Digital Noise Filter
DMAC	Direct Memory Access Controller
INT	Interrupt
I^2C	Inter-Integrated Circuit
I2CS	I^2C wake-up circuit from Stand-by mode
LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
PMD+	Programmable Motor Control Circuit Plus
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
T32A	32-bit Timer Event counter
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Toshiba Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

This chapter describes peripheral function-related channels or number of units, information of pins and product specific function information. Use this chapter in conjunction with Reference Manual for Peripheral Function.

2. Information of Peripheral Function

2.1. Register Base Address

The type of the register base address used by each peripheral function is shown in the following table.

Table 2.1 Register Base Address Type

Product	Base Address Type
TMPM3H(1) group	TYPE 1

Please develop each peripheral function with reference to the above mentioned base address type.
If TYPE 1/2 is not mentioned in the register base address of the reference manual, please use it as TYPE 1.

2.2. Trigger Selector (TRGSEL)

The trigger selector is the circuit which chooses the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger chosen from eight triggers by ***[TSEL0CRn]*** <INSELm> is outputted to the peripheral function of a connection destination.

"Figure 2.1 Example of trigger Selector Connection" is the example in which the trigger signal (port terminals (PB1, PA3) and DMAC (ch18, ch20, ch23, and ch25)) are connected to the DMAC (ch30) via the trigger selector.

The setup of input trigger selection (<INSEL14[2:0]>), edge detection condition selection (<UPDN14>), trigger output selection (<OUTSEL14>), and trigger output control (<EN14>) is performed by ***[TSEL0CR3]***.

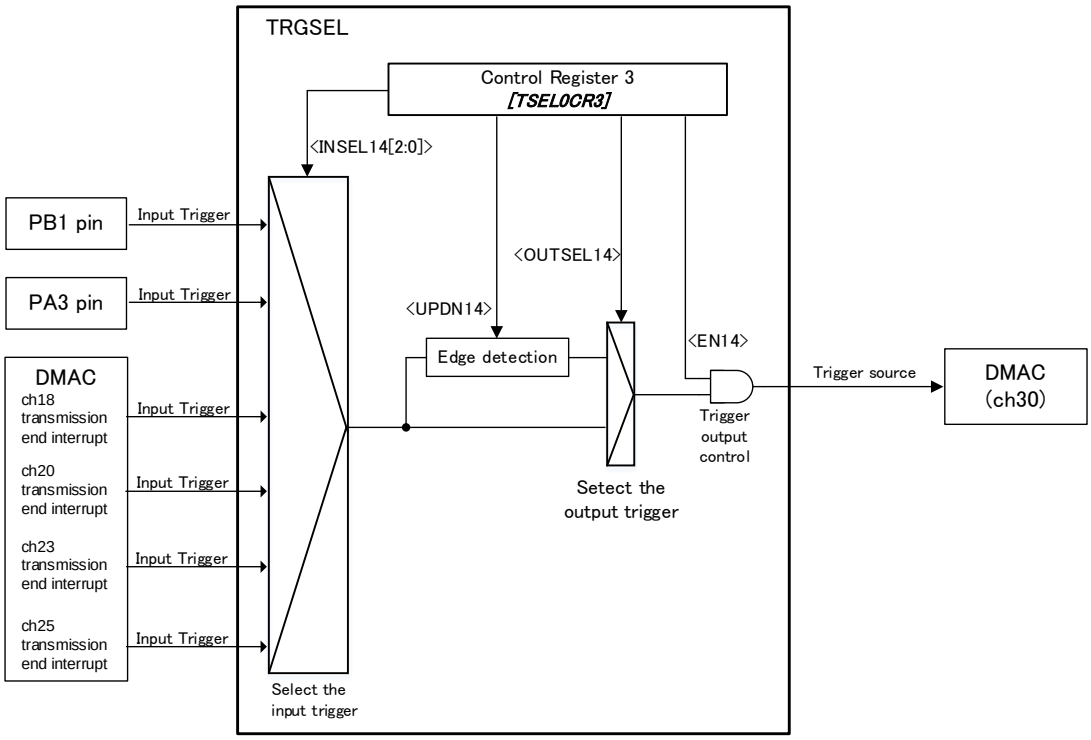

Figure 2.1 Example of trigger Selector Connection

2.2.1. Trigger selector and product table

TMPM3H group (1) trigger group selector consists of 11 control registers (***[TSEL0CR0-10]***), and can control 41 triggers.

The control register, the connection destination, and correspondence products are shown in the following table.

Table 2.2 Trigger selector and product table (1/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR0]	INSEL0[2:0]	DMACA ch16	- ADC unit A General-purpose trigger DMA request - ADC unit A Single conversion DMA request - ADC unit A Continuous conversion DMA request	✓	✓	✓	✓	✓	✓	✓
	INSEL1[2:0]	DMACA ch17	- T32A ch0 DMA request at match A1 register - T32A ch0 DMA request at match C1 register - T32A ch1 DMA request at match A1 register - T32A ch1 DMA request at match C1 register - PMD ch0 PWM interrupt	✓	✓	✓	✓	✓	✓	✓
	INSEL2[2:0]	DMACA ch18	- T32A ch2 DMA request at match A1 register - T32A ch2 DMA request at match C1 register - T32A ch3 DMA request at match A1 register - T32A ch3 DMA request at match C1 register	✓	✓	✓	✓	✓	✓	✓
	INSEL3[2:0]	DMACA ch19	- T32A ch4 DMA request at match A1 register - T32A ch4 DMA request at match C1 register - T32A ch5 DMA request at match A1 register - T32A ch5 DMA request at match C1 register	✓	✓	✓	✓	✓	✓	✓
[TSEL0CR1]	INSEL4[2:0]	DMACA ch20	- T32A ch0 DMA request at match B1 register - T32A ch1 DMA request at match B1 register - T32A ch2 DMA request at match B1 register	✓	✓	✓	✓	✓	✓	✓
	INSEL5[2:0]	DMACA ch21	- T32A ch3 DMA request at match B1 register - T32A ch4 DMA request at match B1 register - T32A ch5 DMA request at match B1 register	✓	✓	✓	✓	✓	✓	✓
	INSEL6[2:0]	DMACA ch22	- T32A ch0 DMA request at capture A0 register - T32A ch0 DMA request at capture A1 register - T32A ch1 DMA request at capture A0 register - T32A ch1 DMA request at capture A1 register - T32A ch0 DMA request at capture C0 register - T32A ch0 DMA request at capture C1 register - T32A ch1 DMA request at capture C0 register - T32A ch1 DMA request at capture C1 register	✓	✓	✓	✓	✓	✓	✓
	INSEL7[2:0]	DMACA ch23	- T32A ch2 DMA request at capture A0 register - T32A ch2 DMA request at capture A1 register - T32A ch3 DMA request at capture A0 register - T32A ch3 DMA request at capture A1 register - T32A ch2 DMA request at capture C0 register - T32A ch2 DMA request at capture C1 register - T32A ch3 DMA request at capture C0 register - T32A ch3 DMA request at capture C1 register	✓	✓	✓	✓	✓	✓	✓

Table 2.3 Trigger selector and product table (2/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR2]	INSEL8[2:0]	DMACA ch24	- T32A ch4 DMA request at capture A0 register - T32A ch4 DMA request at capture A1 register - T32A ch5 DMA request at capture A0 register - T32A ch5 DMA request at capture A1 register - T32A ch4 DMA request at capture C0 register - T32A ch4 DMA request at capture C1 register - T32A ch5 DMA request at capture C0 register - T32A ch5 DMA request at capture C1 register	✓	✓	✓	✓	✓	✓	✓
	INSEL9[2:0]	DMACA ch25	- T32A ch0 DMA request at capture B0 register - T32A ch0 DMA request at capture B1 register - T32A ch1 DMA request at capture B0 register - T32A ch1 DMA request at capture B1 register - T32A ch2 DMA request at capture B0 register - T32A ch2 DMA request at capture B1 register	✓	✓	✓	✓	✓	✓	✓
	INSEL10[2:0]	DMACA ch26	- T32A ch3 DMA request at capture B0 register - T32A ch3 DMA request at capture B1 register - T32A ch4 DMA request at capture B0 register - T32A ch4 DMA request at capture B1 register - T32A ch5 DMA request at capture B0 register - T32A ch5 DMA request at capture B1 register	✓	✓	✓	✓	✓	✓	✓
	INSEL11[2:0]	DMACA ch27	- DMAC ch0 transmission end interrupt - DMAC ch1 transmission end interrupt - DMAC ch4 transmission end interrupt - DMAC ch5 transmission end interrupt - DMAC ch10 transmission end interrupt - DMAC ch11 transmission end interrupt	✓	✓	✓	✓	✓	✓	✓
[TSEL0CR3]	INSEL12[2:0]	DMACA ch28	- DMAC ch2 transmission end interrupt - DMAC ch3 transmission end interrupt - DMAC ch6 transmission end interrupt - DMAC ch7 transmission end interrupt - DMAC ch12 transmission end interrupt - DMAC ch13 transmission end interrupt	✓	✓	✓	✓	✓	✓	✓
	INSEL13[2:0]	DMACA ch29	- DMAC ch8 transmission end interrupt - DMAC ch9 transmission end interrupt - DMAC ch14 transmission end interrupt - DMAC ch15 transmission end interrupt - DMAC ch16 transmission end interrupt - DMAC ch17 transmission end interrupt - DMAC ch22 transmission end interrupt	✓	✓	✓	✓	✓	✓	✓
	INSEL14[2:0]	DMACA ch30	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - DMAC ch18 transmission end interrupt - DMAC ch20 transmission end interrupt - DMAC ch23 transmission end interrupt - DMAC ch25 transmission end interrupt	✓	✓	✓	✓	✓	✓	✓ (Note1)
	INSEL15[2:0]	DMACA ch31	- PN3 pin (TRGIN2) - DMAC ch19 transmission end interrupt - DMAC ch21 transmission end interrupt - DMAC ch24 transmission end interrupt - DMAC ch26 transmission end interrupt	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note2)

Note1: The PA3(TRGIN1) pin cannot be selected.

Note2: The PN3(TRGIN2) pin cannot be selected.

Table 2.4 Trigger selector and product table (3/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR4]	INSEL16[2:0]	ADC unit A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch5 Timer register A1 match trigger - T32A ch5 Timer register B1 match trigger - T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL17[2:0]	ADC unit A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch5 Timer register A1 match trigger - T32A ch5 Timer register B1 match trigger - T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL18[2:0]	TSPI ch0	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch5 Timer register A1 match trigger - T32A ch5 Timer register B1 match trigger - T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL19[2:0]	TSPI ch1	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch5 Timer register A1 match trigger - T32A ch5 Timer register B1 match trigger - T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	-

Note1: The PA3(TRGIN1) pin cannot be selected.

Note2: The PN3(TRGIN2) pin cannot be selected.

Table 2.5 Trigger selector and product table (4/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR5]	INSEL20[2:0]	UART ch0	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch5 Timer register A1 match trigger - T32A ch5 Timer register B1 match trigger - T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL21[2:0]	UART ch1	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) -T32A ch5 Timer register A1 match trigger - T32A ch5 Timer register B1 match trigger - T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL22[2:0]	UART ch2	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) -T32A ch5 Timer register A1 match trigger - T32A ch5 Timer register B1 match trigger - T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	-
	INSEL23[2:0]	T32A ch0 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch0 Transmission completion trigger - UART ch0 Reception completion trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)

Note1: The PA3 (TRGIN1) pin cannot be selected.

Note2: The PN3 (TRGIN2) pin cannot be selected.

Table 2.6 Trigger selector and product table (5/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR6]	INSEL24[2:0]	T32A ch0 Timer B	- T32A ch0 Timer register A0 match trigger - T32A ch0 Timer register A1 match trigger - T32A ch0 Timer A overflow trigger - T32A ch0 timer A underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL25[2:0]	T32A ch0 Timer C	- T32A ch5 Timer register C0 match trigger - T32A ch5 Timer register C1 match trigger - T32A ch5 Timer C overflow trigger - T32A ch5 Timer C underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL26[2:0]	T32A ch1 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch1 Transmission completion trigger - UART ch1 Reception completion trigger	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL27[2:0]	T32A ch1 Timer B	- T32A ch1 Timer register A0 match trigger - T32A ch1 Timer register A1 match trigger - T32A ch1 Timer A overflow trigger - T32A ch1 Timer A underflow trigger	✓	✓	✓	✓	✓	✓	✓

Note1: The PA3 (TRGIN1) pin cannot be selected.

Note2: The PN3 (TRGIN2) pin cannot be selected.

Table 2.7 Trigger selector and product table (6/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR7]	INSEL28[2:0]	T32A ch1 Timer C	- T32A ch0 Timer register C0 match trigger - T32A ch0 Timer register C1 match trigger - T32A ch0 Timer C overflow trigger - T32A ch0 Timer C underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL29[2:0]	T32A ch2 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch2 Transmission completion trigger - UART ch2 Reception completion trigger - I^2C ch0 Interruption	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL30[2:0]	T32A ch2 Timer B	- T32A ch2 Timer register A0 match trigger - T32A ch2 Timer register A1 match trigger - T32A ch2 Timer A overflow trigger - T32A ch2 Timer A underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL31[2:0]	T32A ch2 Timer C	- T32A ch1 Timer register C0 match trigger - T32A ch1 Timer register C1 match trigger - T32A ch1 Timer C overflow trigger - T32A ch1 Timer C underflow trigger	✓	✓	✓	✓	✓	✓	✓

Note1: The PA3 (TRGIN1) pin cannot be selected.

Note2: The PN3 (TRGIN2) pin cannot be selected.

Table 2.8 Trigger selector and product table (7/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR8]	INSEL32[2:0]	T32A ch3 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - TSPI ch0 Transmit completion - TSPI ch0 Receive completion - I²C ch1 Interruption - A-ENC ch0 Dividing pulse signal	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL33[2:0]	T32A ch3 Timer B	- T32A ch3 Timer register A0 match trigger - T32A ch3 Timer register A1 match trigger - T32A ch3 Timer A overflow trigger - T32A ch3 Timer A underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL34[2:0]	T32A ch3 Timer C	- T32A ch2 Timer register C0 match trigger - T32A ch2 Timer register C1 match trigger - T32A ch2 Timer C overflow trigger - T32A ch2 Timer C underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL35[2:0]	T32A ch4 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - TSPI ch1 Transmit completion - TSPI ch1 Receive completion - I²C ch2 Interruption - ELOSC Low speed clock	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)

Note1: The PA3 (TRGIN1) pin cannot be selected.

Note2: The PN3 (TRGIN2) pin cannot be selected.

Table 2.9 Trigger selector and product table (8/8)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
[TSEL0CR9]	INSEL36[2:0]	T32A ch4 Timer B	- T32A ch4 Timer register A0 match trigger - T32A ch4 Timer register A1 match trigger - T32A ch4 Timer A overflow trigger - T32A ch4 Timer A underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL37[2:0]	T32A ch4 Timer C	- T32A ch3 Timer register C0 match trigger - T32A ch3 Timer register C1 match trigger - T32A ch3 Timer C overflow trigger - T32A ch3 Timer C underflow trigger	✓	✓	✓	✓	✓	✓	✓
	INSEL38[2:0]	T32A ch5 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - ADC unit A General-purpose trigger interrupt - ADC unit A Single conversion interrupt - ADC unit A Continuous conversion interrupt - ADC unit A Monitor function0 interrupt - ADC unit A Monitor function1 interrupt	✓	✓	✓	✓ (Note2)	✓ (Note2)	✓ (Note2)	✓ (Note1) (Note2)
	INSEL39[2:0]	T32A ch5 Timer B	- T32A ch5 Timer register A0 match trigger - T32A ch5 Timer register A1 match trigger - T32A ch5 Timer A overflow trigger - T32A ch5 Timer A underflow trigger	✓	✓	✓	✓	✓	✓	✓
[TSEL0CR10]	INSEL40[2:0]	T32A ch5 Timer C	- T32A ch4 Timer register C0 match trigger - T32A ch4 Timer register C1 match trigger - T32A ch4 Timer C overflow trigger - T32A ch4 Timer C underflow trigger	✓	✓	✓	✓	✓	✓	✓

Note1: The PA3 (TRGIN1) pin cannot be selected.

Note2: The PN3 (TRGIN2) pin cannot be selected.

2.2.2. Directions for use and setup

When you use TRGSEL, please set as "1"(clock supply) the clock enabling bit (***[CGFSYSENA]***, ***[CGFSYSENB]***) to which CG corresponds. Please refer to "Clock Control and Operational Mode" of the reference manual for details.

Please perform a setup of a trigger selector in following order.

(1) Selection of an input trigger (***[TSEL0CRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger subdevice bit (***[TSEL0CRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]*** <UPDNm>)

For the selected input trigger signal, select detection of rising edge or falling edge.

To select the edge detection condition, set with the edge detection condition bit (***[TSEL0CRn]*** <UPDNm>) of the control register.

The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)
- ELOSC Low speed clock (fs)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set as "1".

2.2.3. List of Registers

The table below shows control registers and their addresses.

Peripheral function		Channel/Unit	Base address
Trigger selector	TRGSEL	ch0	0x400BB800

Register name		Address(Base+)
Control Register0	***[TSELxCR0]***	0x0000
Control Register1	***[TSELxCR1]***	0x0004
Control Register2	***[TSELxCR2]***	0x0008
Control Register3	***[TSELxCR3]***	0x000C
Control Register4	***[TSELxCR4]***	0x0010
Control Register5	***[TSELxCR5]***	0x0014
Control Register6	***[TSELxCR6]***	0x0018
Control Register7	***[TSELxCR7]***	0x001C
Control Register8	***[TSELxCR8]***	0x0020
Control Register9	***[TSELxCR9]***	0x0024
Control Register10	***[TSELxCR10]***	0x0028

2.2.4. Detail of Registers

The following chapters show the details of a register.

The sign in the functional column parenthesis of each table expresses each function signal name.

2.2.4.1. *[TSEL0CR0]* (Control Register 0)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL3[2:0]	000	R/W	Selection of an input trigger (DMAC A ch19) 000: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 001: T32A ch4 DMA request at match C1 register (T32A04DMAREQCMPC1) 010: T32A ch5 DMA request at match A1 register (T32A05DMAREQCMPA1) 011: T32A ch5 DMA request at match C1 register (T32A05DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0".
26	-	0	R/W	Write as "0".
25	-	0	R/W	Write as "0".
24	EN3	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL2[2:0]	000	R/W	Selection of an input trigger (DMAC A ch18) 000: T32A ch2 DMA request at match A1 register (T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register (T32A02DMAREQCMPC1) 010: T32A ch3 DMA request at match A1 register (T32A03DMAREQCMPA1) 011: T32A ch3 DMA request at match C1 register (T32A03DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0".
18	-	0	R/W	Write as "0".
17	-	0	R/W	Write as "0".
16	EN2	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL1[2:0]	000	R/W	Selection of an input trigger (DMAC A ch17) 000: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 001: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 010: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 011: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 100: PMD+ ch0 PWM interrupt (INTPMD0) 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0".
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	EN1	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL0[2:0]	000	R/W	Selection of an input trigger (DMAC A ch16) 000: ADC unit A General-purpose trigger DMA request (ADATRG_DMAREQ) 001: ADC unit A Single conversion DMA request (ADASGL_DMAREQ) 010: ADC unit A Continuous conversion DMA request (ADACNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN0	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.2. *[TSEL0CR1]* (Control Register 1)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL7[2:0]	000	R/W	Selection of an input trigger (DMAC A ch23) 000: T32A ch2 DMA request at capture A0 register (T32A02DMAREQCAPA0) 001: T32A ch2 DMA request at capture A1 register (T32A02DMAREQCAPA1) 010: T32A ch3 DMA request at capture A0 register (T32A03DMAREQCAPA0) 011: T32A ch3 DMA request at capture A1 register (T32A03DMAREQCAPA1) 100: T32A ch2 DMA request at capture C0 register (T32A02DMAREQCAPC0) 101: T32A ch2 DMA request at capture C1 register (T32A02DMAREQCAPC1) 110: T32A ch3 DMA request at capture C0 register (T32A03DMAREQCAPC0) 111: T32A ch3 DMA request at capture C1 register (T32A03DMAREQCAPC1)
27	-	0	R	Read as "0".
26	-	0	R/W	Write as "0".
25	-	0	R/W	Write as "0".
24	EN7	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL6[2:0]	000	R/W	Selection of an input trigger (DMAC A ch22) 000: T32A ch0 DMA request at capture A0 register (T32A00DMAREQCAPA0) 001: T32A ch0 DMA request at capture A1 register (T32A00DMAREQCAPA1) 010: T32A ch1 DMA request at capture A0 register (T32A01DMAREQCAPA0) 011: T32A ch1 DMA request at capture A1 register (T32A01DMAREQCAPA1) 100: T32A ch0 DMA request at capture C0 register (T32A00DMAREQCAPC0) 101: T32A ch0 DMA request at capture C1 register (T32A00DMAREQCAPC1) 110: T32A ch1 DMA request at capture C0 register (T32A01DMAREQCAPC0) 111: T32A ch1 DMA request at capture C1 register (T32A01 DMAREQCAPC1)
19	-	0	R	Read as "0".
18	-	0	R/W	Write as "0".
17	-	0	R/W	Write as "0".
16	EN6	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL5[2:0]	000	R/W	Selection of an input trigger (DMAC A ch21) 000: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 001: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 010: T32A ch5 DMA request at match B1 register (T32A05DMAREQCMPB1) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0".
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	EN5	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL4[2:0]	000	R/W	Selection of an input trigger (DMAC A ch20) 000: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 001: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 010: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN4	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.3. *[TSEL0CR2]* (Control Register 2)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL11[2:0]	000	R/W	Selection of an input trigger (DMAC A ch27) 000: DMAC ch0 transmission end interrupt (INTDMAATC0) 001: DMAC ch1 transmission end interrupt (INTDMAATC1) 010: DMAC ch4 transmission end interrupt (INTDMAATC4) 011: DMAC ch5 transmission end interrupt (INTDMAATC5) 100: DMAC ch10 transmission end interrupt (INTDMAATC10) 101: DMAC ch11 transmission end interrupt (INTDMAATC11) 110: Reserved 111: Reserved
27	-	0	R	Read as "0".
26	-	0	R/W	Write as "0".
25	-	0	R/W	Write as "0".
24	EN11	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL10[2:0]	000	R/W	Selection of an input trigger (DMAC A ch26) 000: T32A ch3 DMA request at capture B0 register (T32A03DMAREQCAPB0) 001: T32A ch3 DMA request at capture B1 register (T32A03DMAREQCAPB1) 010: T32A ch4 DMA request at capture B0 register (T32A04DMAREQCAPB0) 011: T32A ch4 DMA request at capture B1 register (T32A04DMAREQCAPB1) 100: T32A ch5 DMA request at capture B0 register (T32A05DMAREQCAPB0) 101: T32A ch5 DMA request at capture B1 register (T32A05DMAREQCAPB1) 110: Reserved 111: Reserved
19	-	0	R	Read as "0".
18	-	0	R/W	Write as "0".
17	-	0	R/W	Write as "0".
16	EN10	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL9[2:0]	000	R/W	Selection of an input trigger (DMAC A ch25) 000: T32A ch0 DMA request at capture B0 register (T32A00DMAREQCAPB0) 001: T32A ch0 DMA request at capture B1 register (T32A00DMAREQCAPB1) 010: T32A ch1 DMA request at capture B0 register (T32A01DMAREQCAPB0) 011: T32A ch1 DMA request at capture B1 register (T32A01DMAREQCAPB1) 100: T32A ch2 DMA request at capture B0 register (T32A02DMAREQCAPB0) 101: T32A ch2 DMA request at capture B1 register (T32A02DMAREQCAPB1) 110: Reserved 111: Reserved
11	-	0	R	Read as "0".
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	EN9	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL8[2:0]	000	R/W	Selection of an input trigger (DMAC A ch24) 000: T32A ch4 DMA request at capture A0 register (T32A04DMAREQCAPA0) 001: T32A ch4 DMA request at capture A1 register (T32A04DMAREQCAPA1) 010: T32A ch5 DMA request at capture A0 register (T32A05DMAREQCAPA0) 011: T32A ch5 DMA request at capture A1 register (T32A05DMAREQCAPA1) 100: T32A ch4 DMA request at capture C0 register (T32A04DMAREQCAPC0) 101: T32A ch4 DMA request at capture C1 register (T32A04DMAREQCAPC1) 110: T32A ch5 DMA request at capture C0 register (T32A05DMAREQCAPC0) 111: T32A ch5 DMA request at capture C1 register (T32A05DMAREQCAPC1)
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN8	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.4. *[TSEL0CR3]* (Control Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL15[2:0]	000	R/W	Selection of an input trigger (DMAC A ch31) 000: PN3 pin (TRGIN2) 001: DMAC ch19 transmission end interrupt (INTDMAATC19) 010: DMAC ch21 transmission end interrupt (INTDMAATC21) 011: DMAC ch24 transmission end interrupt (INTDMAATC24) 100: DMAC ch26 transmission end interrupt (INTDMAATC26) 101: Reserved 110: Reserved 111: Reserved When <INSEL15[2:0]> is set to "000"(PN3 pin), set "1" to <OUTSEL15>
27	-	0	R	Read as "0".
26	UPDN15	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL15	0	R/W	Selection of a trigger output 0: The edge detection is disable 1: Edge detection is enable
24	EN15	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL14[2:0]	000	R/W	Selection of an input trigger (DMAC A ch30) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: DMAC ch18 transmission end interrupt (INTDMAATC18) 011: DMAC ch20 transmission end interrupt (INTDMAATC20) 100: DMAC ch23 transmission end interrupt (INTDMAATC23) 101: DMAC ch25 transmission end interrupt (INTDMAATC25) 110: Reserved 111: Reserved When <INSEL14[2:0]> is set to "000"(PB1 pin) or 001(PA3 pin), set "1" to <OUTSEL14>
19	-	0	R	Read as "0".
18	UPDN14	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL14	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN14	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL13[2:0]	000	R/W	Selection of an input trigger (DMAC A ch29) 000: DMAC ch8 transmission end interrupt (INTDMAATC8) 001: DMAC ch9 transmission end interrupt (INTDMAATC9) 010: DMAC ch14 transmission end interrupt (INTDMAATC14) 011: DMAC ch15 transmission end interrupt (INTDMAATC15) 100: DMAC ch16 transmission end interrupt (INTDMAATC16) 101: DMAC ch17 transmission end interrupt (INTDMAATC17) 110: DMAC ch22 transmission end interrupt (INTDMAATC22) 111: Reserved
11	-	0	R	Read as "0".
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	EN13	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL12[2:0]	000	R/W	Selection of an input trigger (DMAC A ch28) 000: DMAC ch2 transmission end interrupt (INTDMAATC2) 001: DMAC ch3 transmission end interrupt (INTDMAATC3) 010: DMAC ch6 transmission end interrupt (INTDMAATC6) 011: DMAC ch7 transmission end interrupt (INTDMAATC7) 100: DMAC ch12 transmission end interrupt (INTDMAATC12) 101: DMAC ch13 transmission end interrupt (INTDMAATC13) 110: Reserved 111: Reserved
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN12	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.5. *[TSEL0CR4]* (Control Register 4)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL19[2:0]	000	R/W	Selection of an input trigger (TSPI ch1) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL19[2:0]> is set to 000(PB1pin) , 001(PA3pin) or 010(PN3pin), set "1" to <OUTSEL19>.
27	-	0	R	Read as "0".
26	UPDN19	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL19	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN19	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL18[2:0]	000	R/W	Selection of an input trigger (TSPI ch0) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL18[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL18>.
19	-	0	R	Read as "0".
18	UPDN18	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL18	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN18	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL17[2:0]	000	R/W	Selection of an input trigger (ADC unit A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL17[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL17>.
11	-	0	R	Read as "0".
10	UPDN17	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL17	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN17	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL16[2:0]	000	R/W	Selection of an input trigger (ADC unit A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch5 T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL16[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL16>.
3	-	0	R	Read as "0".
2	UPDN16	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL16	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN16	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.6. *[TSEL0CR5]* (Control Register 5)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL23[2:0]	000	R/W	Selection of an input trigger (T32A ch0 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: UART ch0 Transmission completion trigger (UART0TXTRG) 100: UART ch0 Reception completion trigger (UART0RXTRG) 101: Reserved 110: Reserved 111: Reserved When <INSEL23[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL23>.
27	-	0	R	Read as "0".
26	UPDN23	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL23	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN23	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL22[2:0]	000	R/W	Selection of an input trigger (UART ch2) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL22[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL22>.
19	-	0	R	Read as "0".
18	UPDN22	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL22	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN22	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL21[2:0]	000	R/W	Selection of an input trigger (UART ch1) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL21[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL21>.
11	-	0	R	Read as "0".
10	UPDN21	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL21	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN21	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL20[2:0]	000	R/W	Selection of an input trigger (UART ch0) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL20[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL20>.
3	-	0	R	Read as "0".
2	UPDN20	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL20	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN20	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.7. *[TSEL0CR6]* (Control Register 6)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL27[2:0]	000	R/W	Selection of an input trigger (T32A ch1 Timer B) 000: T32A ch1 Timer register A0 match trigger (T32A01TRGOUTCMPA0) 001: T32A ch1 Timer register A1 match trigger (T32A01TRGOUTCMPA1) 010: T32A ch1 Timer A overflow trigger (T32A01TRGOUTOFA) 011: T32A ch1 Timer A underflow trigger (T32A01TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0".
26	-	0	R/W	Write as "0".
25	-	0	R/W	Write as "0".
24	EN27	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL26[2:0]	000	R/W	Selection of an input trigger (T32A ch1 Timer A) 000: PB1pin (TRGIN0) 001: PA3pin (TRGIN1) 010: PN3pin (TRGIN2) 011: UART ch1 Transmission completion trigger (UART1TXTRG) 100: UART ch1 Reception completion trigger (UART1RXTRG) 101: Reserved 110: Reserved 111: Reserved When <INSEL26[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL26>.
19	-	0	R	Read as "0".
18	UPDN26	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL26	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN26	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL25[2:0]	000	R/W	Selection of an input trigger (T32A ch0 Timer C) 000: T32A ch5 Timer register C0 match trigger (T32A05TRGOUTCMPC0) 001: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 010: T32A ch5 timer C overflow trigger (T32A05TRGOUTOFC) 011: T32A ch5 timer C underflow trigger (T32A05TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0".
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	EN25	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL24[2:0]	000	R/W	Selection of an input trigger (T32A ch0 Timer B) 000: T32A ch0 Timer register A0 match trigger (T32A00TRGOUTCMPA0) 001: T32A ch0 Timer register A1 match trigger (T32A00TRGOUTCMPA1) 010: T32A ch0 Timer A overflow trigger (T32A00TRGOUTOFA) 011: T32A ch0 Timer A underflow trigger (T32A00TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN24	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.8. *[TSEL0CR7]* (Control Register 7)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL31[2:0]	000	R/W	Selection of an input trigger (T32A ch2 Timer C) 000: T32A ch1 Timer register C0 match trigger (T32A01TRGOUTCMPC0) 001: T32A ch1 Timer register C1 match trigger (T32A01TRGOUTCMPC1) 010: T32A ch1 Timer C overflow trigger (T32A01TRGOUTOFC) 011: T32A ch1 Timer C underflow trigger (T32A01TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0".
26	-	0	R/W	Write as "0".
25	-	0	R/W	Write as "0".
24	EN31	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL30[2:0]	000	R/W	Selection of an input trigger (T32A ch2 Timer B) 000: T32A ch2 Timer register A0 match trigger (T32A02TRGOUTCMPA0) 001: T32A ch2 Timer register A1 match trigger (T32A02TRGOUTCMPA1) 010: T32A ch2 Timer A overflow trigger (T32A02TRGOUTOFA) 011: T32A ch2 Timer A underflow trigger (T32A02TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0".
18	-	0	R/W	Write as "0".
17	-	0	R/W	Write as "0".
16	EN30	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL29[2:0]	000	R/W	Selection of an input trigger (T32A ch2 Timer A) 000: PB1pin (TRGIN0) 001: PA3pin (TRGIN1) 010: PN3pin (TRGIN2) 011: UART ch2 Transmission completion trigger (UART2TXTRG) 100: UART ch2 Reception completion trigger (UART2RXTRG) 101: I^2C ch0 interrupt (INTI2C0) 110: Reserved 111: Reserved When <INSEL29[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL29>.
11	-	0	R	Read as "0".
10	UPDN29	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL29	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN29	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL28[2:0]	000	R/W	Selection of an input trigger (T32A ch1 Timer C) 000: T32A ch0 Timer register C0 match trigger (T32A00TRGOUTCMPC0) 001: T32A ch0 Timer register C1 match trigger (T32A00TRGOUTCMPC1) 010: T32A ch0 Timer C overflow trigger (T32A00TRGOUTOFC) 011: T32A ch0 Timer C underflow trigger (T32A00TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN28	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.9. *[TSEL0CR8]* (Control Register 8)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL35[2:0]	000	R/W	Selection of an input trigger (T32A ch4 Timer A) 000: PB1pin (TRGIN0) 001: PA3pin (TRGIN1) 010: PN3pin (TRGIN2) 011: TSPI ch1 transmission completion (TSPI1TXEND) 100: TSPI ch1 reception completion (TSPI1RXEND) 101: I^2C ch2 interrupt (INTI2C2) 110: ELOSC low speed clock (fs) 111: Reserved When <INSEL35[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL35>.
27	-	0	R	Read as "0".
26	UPDN35	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL35	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN35	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL34[2:0]	000	R/W	Selection of an input trigger (T32A ch3 Timer C) 000: T32A ch2 Timer register C0 match trigger (T32A02TRGOUTCMPC0) 001: T32A ch2 Timer register C1 match trigger (T32A02TRGOUTCMPC1) 010: T32A ch2 Timer C overflow trigger (T32A02TRGOUTOFC) 011: T32A ch2 Timer C underflow trigger (T32A02TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as "0".
18	-	0	R/W	Write as "0".
17	-	0	R/W	Write as "0".
16	EN34	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL33[2:0]	000	R/W	Selection of an input trigger (T32A ch3 Timer B) 000: T32A ch3 Timer register A0 match trigger (T32A03TRGOUTCMPA0) 001: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 010: T32A ch3 Timer A overflow trigger (T32A03TRGOUTOFA) 011: T32A ch3 Timer A underflow trigger (T32A03TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0".
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	EN33	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL32[2:0]	000	R/W	Selection of an input trigger (T32A ch3 Timer A) 000: PB1pin (TRGIN0) 001: PA3pin (TRGIN1) 010: PN3pin (TRGIN2) 011: TSPI ch0 Transmit complete (TSPI0TXEND) 100: TSPI ch0 Receive complete (TSPI0RXEND) 101: I^2C ch1 interruption (INTI2C1) 110: A-ENC ch0 Dividing pulse signal (ENC0TIMPLS) 111: Reserved When <INSEL32[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL32>.
3	-	0	R	Read as "0".
2	UPDN32	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL32	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN32	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.10. *[TSEL0CR9]* (Control Register 9)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as "0".
30:28	INSEL39[2:0]	000	R/W	Selection of an input trigger (T32A ch5 Timer B) 000: T32A ch5 Timer register A0 match trigger (T32A05TRGOUTCMPA0) 001: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 010: T32A ch5 Timer A overflow trigger (T32A05TRGOUTOFA) 011: T32A ch5 Timer A underflow trigger (T32A05TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as "0".
26	-	0	R/W	Write as "0".
25	-	0	R/W	Write as "0".
24	EN39	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as "0".
22:20	INSEL38[2:0]	000	R/W	Selection of an input trigger (T32A ch5 Timer A) 000: PB1pin (TRGIN0) 001: PA3pin (TRGIN1) 010: PN3pin (TRGIN2) 011: ADC unit A General-purpose trigger interrupt (INTADATRG) 100: ADC unit A Single conversion interrupt (INTADASG) 101: ADC unit A Continuous conversion interrupt (INTADACNT) 110: ADC unit A Monitor function0 interrupt (INTADACP0) 111: ADC unit A Monitor function1 interrupt (INTADACP1) When <INSEL38[2:0]> is set to "000"(PB1pin), "001"(PA3pin) or "010"(PN3pin), set "1" to <OUTSEL38>.
19	-	0	R	Read as "0".
18	UPDN38	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL38	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN38	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as "0".
14:12	INSEL37[2:0]	000	R/W	Selection of an input trigger (T32A ch4 Timer C) 000: T32A ch3 Timer register C0 match trigger (T32A03TRGOUTCMPC0) 001: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 010: T32A ch3 Timer C overflow trigger (T32A03TRGOUTOFC) 011: T32A ch3 Timer C underflow trigger (T32A03TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as "0".
10	-	0	R/W	Write as "0".
9	-	0	R/W	Write as "0".
8	EN37	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as "0".
6:4	INSEL36[2:0]	000	R/W	Selection of an input trigger (T32A ch4 Timer B) 000: T32A ch4 Timer register A0 match trigger (T32A04TRGOUTCMPA0) 001: T32A ch4 Timer register A1 match trigger (T32A04TRGOUTCMPA1) 010: T32A ch4 Timer A overflow trigger (T32A04TRGOUTOFA) 011: T32A ch4 Timer A underflow trigger (T32A04TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN36	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.11. *[TSEL0CR10]* (Control Register 10)

Bit	Bit Symbol	After Reset	Type	Function
31:7	-	0	R	Read as "0".
6:4	INSEL40[2:0]	000	R/W	Selection of an input trigger (T32A ch5 Timer C) 000: T32A ch4 Timer register C0 match trigger (T32A04TRGOUTCMPC0) 001: T32A ch4 Timer register C1 match trigger (T32A04TRGOUTCMPC1) 010: T32A ch4 Timer C overflow trigger (T32A04TRGOUTOFC) 011: T32A ch4 Timer C underflow trigger (T32A04TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "0".
0	EN40	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.3. Clock Selective Watchdog Timer (SIWDT)

2.3.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.10 SIWDT Built-in channel

Product	SIWDT Built-in channel (✓: Available, -: N/A)
	ch0
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.3.2. Count clock

The clock selection type watchdog timer can choose the clock to count. The clock which can be chosen as the following tables is shown.

Table 2.11 SIWDT Count clock

Clock	Signal name	Selection
System clock	fsys	***[SIWD0MOD]***<WDCLS> It chooses with a register.
Internal High Speed Oscillator 1 Clock	f_{IHOSC1}	
Internal High Speed Oscillator 2 Clock	f_{IHOSC2}	

2.3.3. Control Output

When the Internal High Speed Oscillator 2 (f_{IHOSC2}) is chosen, it is possible to forbid rewriting of the Internal High Speed Oscillator 2.

Table 2.12 SIWDT Control Output

Control Output	Signal name	Remarks
The protection signal of an Internal High Speed Oscillator 2 oscillation control bit (***[CGOSCCR]***<IHOSC2EN>).	OSCPRO	It sets up by the ***[SIWD0OSCCR]***<OSCPRO> register.

2.4. Oscillation Frequency Detector (OFD)

2.4.1. Built-in List

The following table shows the built-in list for each product.

Table 2.13 OFD Built-in List

Product	Built-in OFD (✓:Available, -: N/A)
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.4.2. Reference clock

In the oscillation frequency detection circuit, the clock of the following tables operates with the reference clock.

Table 2.14 OFD Reference clock

Reference clock	Signal name	Divide value
Internal High Speed Oscillators 2	f_{IHOSC2}	256

2.4.3. Detection object clock

A frequency sensing circuit chooses a clock to monitor from the detection object clock of the following tables.

Table 2.15 OFD Detection object clock

Detection object clock		Signal name
Input Signal	External high speed oscillator clock	f_{EHOSC}
	It is the clock selected by ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> of CG (Clock control part).	fc

2.5. Debug Interface

2.5.1. Debugging interface terminal list of each product.

Table 2.16 Debugging interface terminal list

Debugging pin (Signal name)	Port	Product table (✓: Available, -: N/A)						
		M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
SWDIO	PK2	✓	✓	✓	✓	✓	✓	✓
TMS								
SWCLK	PK3	✓	✓	✓	✓	✓	✓	✓
TCK								
SWV	PK4	✓	✓	✓	✓	✓	✓	-
TDO								
TDI	PK5	✓	✓	✓	✓	✓	✓	-
TRST_N	PK6	✓	✓	✓	-	-	-	-
TRACECLK	PM0	✓	✓	✓	-	-	-	-
TRACEDATA0	PM1	✓	✓	✓	-	-	-	-
TRACEDATA1	PM2	✓	✓	✓	-	-	-	-
TRACEDATA2	PM3	✓	-	-	-	-	-	-
TRACEDATA3	PM4	✓	-	-	-	-	-	-

2.6. Flash Memory

2.6.1. Clock for Write/Erase

As for flash memory, the clock of the following tables is used for writing/erasing of the code flash or the data flash.

Table 2.17 Clock for Write/Erase

Clock for Write/Erase
f_{IHOSC1}

2.6.2. The code flash block configuration of each product.

The code flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.18 The code flash of each product

Block name		M3H6FWFG M3H6FWDFG M3H5FWFG M3H5FWDFG M3H4FWUG M3H4FWFG M3H3FWUG M3H2FWQG M3H2FWDUG M3H1FWUG	M3H6FUFG M3H6FUDFG M3H5FUFG M3H5FUDFG M3H4FUUG M3H4FUFG M3H3FUUG M3H2FUQG M3H2FUDUG M3H1FUUG	M3H6FSFG M3H6FSDFG M3H5FSFG M3H5FSDFG M3H4FSUG M3H4FSFG M3H3FSUG M3H2FSQG M3H2FSDUG M3H1FSUG M3H0FSDUG	M3H1FPUG	M3H0FMDUG	Block Size (KB)
Block0	PG0	✓	✓	✓	✓	✓	4
	PG1	✓	✓	✓	✓	✓	4
	PG2	✓	✓	✓	✓	✓	4
	PG3	✓	✓	✓	✓	✓	4
	PG4	✓	✓	✓	✓	✓	4
	PG5	✓	✓	✓	✓	✓	4
	PG6	✓	✓	✓	✓	✓	4
	PG7	✓	✓	✓	✓	✓	4
Block1		✓	✓	✓	✓ (Note1)	-	32
Block2		✓	✓	-	-	-	32
Block3		✓	-	-	-	-	32

✓: Available, -: N/A

Note1: 16KB only.

2.6.3. The data flash block configuration of each product.

The data flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.19 The data flash of each product

Block name	M3H6FWFG M3H6FWDFG M3H6FUFG M3H6FUDFG M3H5FWFG M3H5FWDFG M3H5FUFG M3H5FUDFG M3H4FWUG M3H4FWFG M3H4FUUG M3H4FUFG M3H3FWUG M3H3FUUG M3H2FWQG M3H2FWDUG M3H2FUQG M3H2FUDUG M3H1FWUG M3H1FUUG	M3H6FSFG M3H6FSDFG M3H5FSFG M3H5FSDFG M3H4FSUG M3H4FSFG M3H3FSUG M3H2FSQG M3H2FSDUG M3H1FSUG M3H0FSDUG	M3H1FPUG M3H0FMDUG	Block Size (KB)
Block0	✓	✓	✓	4
Block1	✓	✓	✓	4
Block2	✓	✓	-	4
Block3	✓	✓	-	4
Block4	✓	-	-	4
Block5	✓	-	-	4
Block6	✓	-	-	4
Block7	✓	-	-	4

✓: Available, -: N/A

2.6.4. Single boot use resource

The peripheral function of the following table is used in single boot.

Table 2.20 Single boot use resource

Peripheral function	Channel	Pin name
BOOT	-	PB0 (BOOT_N)
UART	ch0	PA1/PA2 (UT0TXDA/UT0RXD) or, PM1/PM2 (UT0TXDA/UT0RXD) : (Note)
T32A	ch0	-

Note: At the time of single boot start, the selection of PA1/PA2 or PM1/PM2 is distinguished automatically by the state of the terminal. During the automatic distinction, internal pull-up of PA2/UT0RXD and PM2/UT0RXD becomes effective, and the "High" level is outputted. Please keep the "High" level (open or "High" level input) of UT0RXD which is not used at this time. As for UT0RXD which is not used after automatic distinction finishes, "Hi-z" is outputted.

The range of the RAM address transmitted by the RAM loader command should use the following table.

Table 2.21 The end address in which RAM transmission is possible

Product name	The end address in which RAM transmission is possible
TMPM3H6FWFG TMPM3H6FWDFG TMPM3H5FWFG TMPM3H5FWDFG TMPM3H4FWFG TMPM3H4FWUG TMPM3H3FWUG TMPM3H2FWDUG TMPM3H2FWQG TMPM3H1FWUG	0x20000400 to 0x20003FFF
TMPM3H6FUFG TMPM3H6FUDFG TMPM3H5FUFG TMPM3H5FUDFG TMPM3H4FUFG TMPM3H4FUUG TMPM3H3FUUG TMPM3H2FUDUG TMPM3H2FUQG TMPM3H1FUUG	0x20000400 to 0x20002FFF
TMPM3H6FSFG TMPM3H6FSDFG TMPM3H5FSFG TMPM3H5FSDFG TMPM3H4FSFG TMPM3H4FSUG TMPM3H3FSUG TMPM3H2FSDUG TMPM3H2FSQG TMPM3H1FSUG TMPM3H0FSDUG	0x20000400 to 0x20001FFF
TMPM3H1FPUG	0x20000400 to 0x200017FF
TMPM3H0FMDUG	

2.7. DMA Controller (DMAC)

2.7.1. Built-in unit

The built-in unit for each product is shown in the following table.

Table 2.22 DMAC Built-in unit

Product	DMAC Built-in unit (✓: Available, -: N/A)
	unit A
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.7.2. DMA request list

A DMA request list is shown in the following table.

The channel which has a register name in the trigger selector column of a table should choose the demand used by a trigger group selector. "-" in a table does not have an applicable function.

Table 2.23 DMA Request list (1/3)

Channel	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
0	TSPI ch0 Receive DMA request	TSPI0RX_DMA	-	TSPI ch0 Receive DMA request	TSPI0RX_DMA
1	TSPI ch0 Transmit DMA request	TSPI0TX_DMA	-	TSPI ch0 Transmit DMA request	TSPI0TX_DMA
2	TSPI ch1 Receive DMA request (Note2)	TSPI1RX_DMA	-	TSPI ch1 Receive DMA request (Note2)	TSPI1RX_DMA
3	TSPI ch1 Transmit DMA request (Note2)	TSPI1TX_DMA	-	TSPI ch1 Transmit DMA request (Note2)	TSPI1TX_DMA
4	-	-	-	I^2C ch0 Receiving DMA request	I2C0RXDMAREQ
5	-	-	-	I^2C ch0 Transmitting DMA request	I2C0TXDMAREQ
6	-	-	-	I^2C ch1 Receiving DMA request (Note3)	I2C1RXDMAREQ
7	-	-	-	I^2C ch1 Transmitting DMA request (Note3)	I2C1TXDMAREQ
8	-	-	-	I^2C ch2 Receiving DMA request (Note4)	I2C2RXDMAREQ
9	-	-	-	I^2C ch2 Transmitting DMA request (Note4)	I2C2TXDMAREQ
10	UART ch0 Reception DMA request	UART0RX_DMAREQ	-	UART ch0 Reception DMA request	UART0RX_DMAREQ
11	UART ch0 Transmission DMA request	UART0TX_DMAREQ	-	UART ch0 Transmission DMA request	UART0TX_DMAREQ
12	UART ch1 Reception DMA request	UART1RX_DMAREQ	-	UART ch1 Reception DMA request	UART1RX_DMAREQ
13	UART ch1 Transmission DMA request	UART1TX_DMAREQ	-	UART ch1 Transmission DMA request	UART1TX_DMAREQ
14	UART ch2 Reception DMA request (Note5)	UART2RX_DMAREQ	-	UART ch2 Reception DMA request (Note5)	UART2RX_DMAREQ
15	UART ch2 Transmission DMA request (Note5)	UART2TX_DMAREQ	-	UART ch2 Transmission DMA request (Note5)	UART2TX_DMAREQ
16	-	-	***[TSEL0CR0]*** <INSEL0[2:0]> (Note1)	ADC unit A General-purpose trigger DMA request	ADATRG_DMAREQ
				ADC unit A Single conversion DMA request	ADASGL_DMAREQ
				ADC unit A Continuous conversion DMA request	ADACNT_DMAREQ

Note1: ch16-ch31 choose the trigger source of a DMA request by a trigger group selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: There is not ch1 of TSPI in M3H0.

Note3: There is not ch1 of I^2C in M3H0.

Note4: There is not ch2 of I^2C in M3H2 / M3H1/ M3H0.

Note5: There is not ch2 of UART in M3H0.

Table 2.24 DMA Request list (2/3)

Channel	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
17	-	-	***[TSEL0CR0]*** <INSEL1[2:0]> (Note1)	T32A ch0 DMA request at match A1 register	T32A00DMAREQCMPA1
				T32A ch0 DMA request at match C1 register	T32A00DMAREQCMPC1
				T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1
				T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1
				PMD ch0 PWM interrupt	INTPMD0
18	-	-	***[TSEL0CR0]*** <INSEL2[2:0]> (Note1)	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1
				T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1
				T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1
				T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1
19	-	-	***[TSEL0CR0]*** <INSEL3[2:0]> (Note1)	T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1
				T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1
				T32A ch5 DMA request at match A1 register	T32A05DMAREQCMPA1
				T32A ch5 DMA request at match C1 register	T32A05DMAREQCMPC1
20	-	-	***[TSEL0CR1]*** <INSEL4[2:0]> (Note1)	T32A ch0 DMA request at match B1 register	T32A00DMAREQCMPB1
				T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1
				T32A ch2 DMA request at match B1 register	T32A02DMAREQCMPB1
21	-	-	***[TSEL0CR1]*** <INSEL5[2:0]> (Note1)	T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1
				T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1
				T32A ch5 DMA request at match B1 register	T32A05DMAREQCMPB1
22	-	-	***[TSEL0CR1]*** <INSEL6[2:0]> (Note1)	T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0
				T32A ch0 DMA request at capture A1 register	T32A00DMAREQCAPA1
				T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0
				T32A ch1 DMA request at capture A1 register	T32A01DMAREQCAPA1
				T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0
				T32A ch0 DMA request at capture C1 register	T32A00DMAREQCAPC1
				T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0
				T32A ch1 DMA request at capture C1 register	T32A01DMAREQCAPC1
23	-	-	***[TSEL0CR1]*** <INSEL7[2:0]> (Note1)	T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0
				T32A ch2 DMA request at capture A1 register	T32A02DMAREQCAPA1
				T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0
				T32A ch3 DMA request at capture A1 register	T32A03DMAREQCAPA1
				T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0
				T32A ch2 DMA request at capture C1 register	T32A02DMAREQCAPC1
				T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0
				T32A ch3 DMA request at capture C1 register	T32A03DMAREQCAPC1
24	-	-	***[TSEL0CR2]*** <INSEL8[2:0]> (Note1)	T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0
				T32A ch4 DMA request at capture A1 register	T32A04DMAREQCAPA1
				T32A ch5 DMA request at capture A0 register	T32A05DMAREQCAPA0
				T32A ch5 DMA request at capture A1 register	T32A05DMAREQCAPA1
				T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0
				T32A ch4 DMA request at capture C1 register	T32A04DMAREQCAPC1
				T32A ch5 DMA request at capture C0 register	T32A05DMAREQCAPC0
				T32A ch5 DMA request at capture C1 register	T32A05DMAREQCAPC1

Note1: ch16-ch31 choose the trigger source of a DMA request by a trigger group selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.25 DMA Request list (3/3)

Channel	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
25	-	-	***[TSEL0CR2]*** <INSEL9[2:0]> (Note1)	T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0
				T32A ch0 DMA request at capture B1 register	T32A00DMAREQCAPB1
				T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0
				T32A ch1 DMA request at capture B1 register	T32A01DMAREQCAPB1
				T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0
				T32A ch2 DMA request at capture B1 register	T32A02DMAREQCAPB1
26	-	-	***[TSEL0CR2]*** <INSEL10[2:0]> (Note1)	T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0
				T32A ch3 DMA request at capture B1 register	T32A03DMAREQCAPB1
				T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0
				T32A ch4 DMA request at capture B1 register	T32A04DMAREQCAPB1
				T32A ch5 DMA request at capture B0 register	T32A05DMAREQCAPB0
				T32A ch5 DMA request at capture B1 register	T32A05DMAREQCAPB1
27	-	-	***[TSEL0CR2]*** <INSEL11[2:0]> (Note1)	DMAC ch0 transmission end interrupt	INTDMAATC0
				DMAC ch1 transmission end interrupt	INTDMAATC1
				DMAC ch4 transmission end interrupt	INTDMAATC4
				DMAC ch5 transmission end interrupt	INTDMAATC5
				DMAC ch10 transmission end interrupt	INTDMAATC10
				DMAC ch11 transmission end interrupt	INTDMAATC11
28	-	-	***[TSEL0CR3]*** <INSEL12[2:0]> (Note1)	DMAC ch2 transmission end interrupt	INTDMAATC2
				DMAC ch3 transmission end interrupt	INTDMAATC3
				DMAC ch6 transmission end interrupt	INTDMAATC6
				DMAC ch7 transmission end interrupt	INTDMAATC7
				DMAC ch12 transmission end interrupt	INTDMAATC12
				DMAC ch13 transmission end interrupt	INTDMAATC13
29	-	-	***[TSEL0CR3]*** <INSEL13[2:0]> (Note1)	DMAC ch8 transmission end interrupt	INTDMAATC8
				DMAC ch9 transmission end interrupt	INTDMAATC9
				DMAC ch14 transmission end interrupt	INTDMAATC14
				DMAC ch15 transmission end interrupt	INTDMAATC15
				DMAC ch16 transmission end interrupt	INTDMAATC16
				DMAC ch17 transmission end interrupt	INTDMAATC17
				DMAC ch22 transmission end interrupt	INTDMAATC22
30	-	-	***[TSEL0CR3]*** <INSEL14[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin (Note2)	TRGIN1
				DMAC ch18 transmission end interrupt	INTDMAATC18
				DMAC ch20 transmission end interrupt	INTDMAATC20
				DMAC ch23 transmission end interrupt	INTDMAATC23
				DMAC ch25 transmission end interrupt	INTDMAATC25
31	-	-	***[TSEL0CR3]*** <INSEL15[2:0]> (Note1)	PN3 pin (Note3)	TRGIN2
				DMAC ch19 transmission end interrupt	INTDMAATC19
				DMAC ch21 transmission end interrupt	INTDMAATC21
				DMAC ch24 transmission end interrupt	INTDMAATC24
				DMAC ch26 transmission end interrupt	INTDMAATC26

Note1: ch16-ch31 choose the trigger source of a DMA request by a trigger group selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: There is no PA3 (TRGIN1) pin in M3H0.

Note3: There is no PN3 (TRGIN2) pin in M3H3 / M3H2 / M3H1 / M3H0.

2.8. Programmable Motor Control Circuit plus (PMD+)

2.8.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.26 PMD+ Built-in channel

Product	PMD+ Built-in channel (✓: Available, -: N/A)
	ch0
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.8.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.27 PMD+ Functional pin

Channel	Functional pin		Signal name	Port	Product table (✓: Available, -: N/A)						
					M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	XO0	Output	XO0	PJ1	✓	✓	✓	✓	✓	✓	✓
	YO0	Output	YO0	PJ3	✓	✓	✓	✓	✓	✓	✓
	ZO0	Output	ZO0	PJ5	✓	✓	✓	✓	✓	✓	✓
	UO0	Output	UO0	PJ0	✓	✓	✓	✓	✓	✓	✓
	VO0	Output	VO0	PJ2	✓	✓	✓	✓	✓	✓	✓
	WO0	Output	WO0	PJ4	✓	✓	✓	✓	✓	✓	✓
	EMG0_N	Input	EMG0_N	PK0	✓	✓	✓	✓	✓	✓	✓
	OVV0_N	Input	OVV0_N	PK1	✓	✓	✓	✓	✓	✓	✓

2.8.3. DMA request

A motor control circuit has the DMA request shown in the following tables.

Table 2.28 PMD+ DMA request

Channel	Demand	Signal name	Trigger selector	DMA request channel		
					Single Transmission	Burst Transmission
ch0	PWM interruption	INTPMD0	***[TSEL0CR0]*** <INSEL1[2:0]>	17	-	✓

Note: ✓: Available, -: N/A

2.8.4. Internal signal connection specification

The motor control circuit is connected to the peripheral function inside, as shown in the following table.

2.8.4.1. ADC/A-ENC/T32A connection

Table 2.29 PMD+ ch0 Internal signal connection specification: Input

Input/output	Functional input (PMD+)		Input Signal		
		Signal name	Peripheral function		Signal name
Input	OVV state signal (AD monitor function0)	ADACMP0L_N	ADC unit A	Monitor function0 output for PMD protect function	ADACP0L_N
	OVV state signal (AD monitor function1)	ADACMP1L_N		Monitor function1 output for PMD protect function	ADACP1L_N
	Commutation trigger (ENC position detection sync)	INTENC00	A-ENC ch0	Encoder input interruption 0	INTENC00
	Commutation trigger (ENC MCMP completion sync)	ENC0CTRGO		The commutation trigger for motor control circuit (PMD)	ENC0CTRGO
	Commutation trigger (General-purpose timer sync)	PMD0TMR	T32A ch3	Timer register A0 match trigger	T32A03TRGOUTCMPA0

Table 2.30 PMD+ ch0 Internal signal connection specification: Output

Input/output	Functional Output (PMD+)		Output place		
		Signal name	Peripheral function		Signal name
Output	ADC synchronous sampling Output 0	PMD0TRG0	ADC unit A	PMD trigger 0	PMDTRG0
	ADC synchronous sampling Output 1	PMD0TRG1		PMD trigger 1	PMDTRG1
	ADC synchronous sampling Output 2	PMD0TRG2		PMD trigger 2	PMDTRG2
	ADC synchronous sampling Output 3	PMD0TRG3		PMD trigger 3	PMDTRG3
	ADC synchronous sampling Output 4	PMD0TRG4		PMD trigger 4	PMDTRG4
	ADC synchronous sampling Output 5	PMD0TRG5		PMD trigger 5	PMDTRG5
	PWM signal for the encoder input	PMD0PWMON	A-ENC ch0	The PWM signal for a sampling	ENC0PWMON

2.9. Advanced Encoder Input Circuit (A-ENC)

2.9.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.31 A-ENC Built-in channel

Product	A-ENC Built-in channel (✓: Available, -: N/A)
	ch0
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.9.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.32 A-ENC Functional pin and port

Channel	Functional pin		Signal name	Port	Product table (✓: Available, -: N/A)						
					M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	ENC0A	Input	ENC0A	PA0	✓	✓	✓	✓	✓	✓	✓
	ENC0B	Input	ENC0B	PA1	✓	✓	✓	✓	✓	✓	✓
	ENC0Z	Input	ENC0Z	PA2	✓	✓	✓	✓	✓	✓	✓

2.9.3. Internal signal connection specification

2.9.3.1. T32A / PMD+ connection

The advanced encoder input circuit is connected to the peripheral function inside, as shown in the following table.
"-" in a table does not have an applicable function.

Table 2.33 A-ENC Internal signal connection specification: Input

Input/output	Functional input (A-ENC)		Input Signal		
		Signal name	Peripheral function		Signal name
Input	Timer output signal in general	ENC0PSGI	T32A ch3	Timer A output	T32A03OUTA
	The PWM signal for a sampling	ENC0PWMON	PMD+ ch0	PWM signal for the encoder input	PMD0PWMON

Table 2.34 A-ENC Internal signal connection specification: Output

Input /output	Functional Output (A-ENC)	Signal name	Trigger selector	Output place		
				Peripheral function		Signal name
Output	Divided pulse signal	ENC0TIMPLS	***[TSEL0CR8]*** <INSEL32>	T32A ch3	Timer A internal trigger input	T32A03TRGINAPCK
	The commutation trigger for motor control circuit (PMD)	ENC0CTRGO	-	PMD+ ch0	Commutation trigger (A-ENC MCMP completion sync)	ENC0CTRGO
	Encoder input interruption 0	INTENC00	-		Commutation trigger (A-ENC position detection sync)	INTENC00

2.10. 12-bit Analog to Digital Converter (ADC)

2.10.1. Built-in unit

The built-in unit for each product is shown in the following table.

Table 2.35 ADC Built-in unit

Product	ADC Built-in unit (✓: Available, -: N/A)
	unit A
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.10.2. Functional pin and port

The functional pin is assigned to the port of the following tables.
There is also a channel which does not have a functional pin by a product.

Table 2.36 ADC Functional pin and a port

Input channel	Functional pin (Signal name)	Port	Product table (✓: Available, -: N/A)						
			M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	AINA00	PD0	✓	✓	✓	✓	✓	✓	✓
ch1	AINA01	PD1	✓	✓	✓	✓	✓	✓	✓
ch2	AINA02	PD2	✓	✓	✓	✓	✓	✓	-
ch3	AINA03	PD3	✓	-	-	-	-	-	-
ch4	AINA04	PE0	✓	✓	✓	✓	✓	✓	✓
ch5	AINA05	PE1	✓	✓	✓	✓	✓	✓	✓
ch6	AINA06	PE2	✓	✓	✓	✓	✓	✓	-
ch7	AINA07	PE3	✓	✓	✓	✓	✓	✓	-
ch8	AINA08	PE4	✓	✓	✓	✓	✓	✓	-
ch9	AINA09	PE5	✓	✓	-	-	-	-	-
ch10	AINA10	PE6	✓	✓	-	-	-	-	-
ch11	AINA11	PF0	✓	-	-	-	-	-	-
ch12	AINA12	PF1	✓	-	-	-	-	-	-
ch13	AINA13	PF2	✓	-	-	-	-	-	-
ch14	AINA14	PF3	✓	-	-	-	-	-	-
ch15	AINA15	PF4	✓	-	-	-	-	-	-
ch16	VREFHA	-	✓	✓	✓	✓	✓	✓	✓
ch17	VREFLA	-	✓	✓	✓	✓	✓	✓	✓
ch18	Reference power supply	-	✓	✓	✓	✓	✓	✓	✓

Note1: Internal connection of ch16-ch18 is carried out for self-diagnostic function support.

Note2: VREFH is connected to AVDD5 and VREFL is connected to AVSS.

2.10.3. Clock for the ADC conversion

The clock which shows the 12-bit Analog to Digital Converter in the following tables at the conversion clock is used.

Table 2.37 ADC Clock for the conversion

Clock for the conversion
ADCLK

2.10.4. Set of mode setting register 2

Please be sure to set up the value of the following tables about the set point of the mode setting register 2 (***[ADxMOD2]***).

Table 2.38 ADC Set of mode setting register 2

Register name	Value
[ADxMOD2]<MOD2[31:0]>	0x00000300

2.10.5. DMA request

A 12-bit Analog to Digital Converter has the DMA request shown in the following tables.

Table 2.39 ADC DMA request

Unit	Demand	Signal name	Trigger selector		DMA request channel	
					Single Transmission	Burst Transmission
Unit A	General-purpose trigger DMA request	ADATRG_DMAREQ	***[TSEL0CR0]*** <INSEL0[2:0]>	16	-	✓
	Single conversion DMA request	ADASGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADACNT_DMAREQ			-	✓

Note: ✓: Available, -: N/A

2.10.6. Internal signal connection specification

2.10.6.1. Start-trigger connection specification

The 12-bit Analog to Digital Converter has the AD translation function by the trigger signal.

The input trigger signal which has a register name in the trigger group selector column of the following table should choose the input trigger used by a trigger group selector. "-" in a table does not have an applicable function.

Table 2.40 ADC Start-trigger connection specification

Connection destination (Signal name)	Starting trigger		
	Trigger selector	Input trigger signal	Signal name
PMDTRG0	-	PMD trigger 0	PMD0TRG0
PMDTRG1	-	PMD trigger 1	PMD0TRG1
PMDTRG2	-	PMD trigger 2	PMD0TRG2
PMDTRG3	-	PMD trigger 3	PMD0TRG3
PMDTRG4	-	PMD trigger 4	PMD0TRG4
PMDTRG5	-	PMD trigger 5	PMD0TRG5
PMDTRG6	***[TSEL0CR4]*** <INSEL16[2:0]> (Note1)	PB1 pin	TRGIN0
		PA3 pin (Note2)	TRGIN1
		PN3 pin (Note3)	TRGIN2
		T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
		T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPB1
		T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1
PMDTRG7	-	-	-
PMDTRG8	-	-	-
PMDTRG9	-	-	-
PMDTRG10	-	-	-
PMDTRG11	-	-	-
ADATRGIN	***[TSEL0CR4]*** <INSEL17[2:0]> (Note1)	PB1 pin	TRGIN0
		PA3 pin (Note2)	TRGIN1
		PN3 pin (Note3)	TRGIN2
		T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
		T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPB1
		T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1

Note1: ***[TSEL0CR4]***<INSELx[2:0]> chooses the trigger source of internal triggering by a trigger group selector.a detailed connection destination "2.2. Trigger Selector (TRGSEL)" please refer to it.

Note2: There is no PA3 (TRGIN1) pin in M3H0.

Note3: There is no PN3 (TRGIN2) pin in M3H3 / M3H2 / M3H1 / M3H0.

2.10.6.2. T32A / PMD+ connection

In addition to this, the 12-bit Analog to Digital Converter is connected with the peripheral function inside, as shown in the following table. "-" in a table does not have an applicable function.

Table 2.41 ADC Internal signal connection specification: Output

Input /output	Functional Output (ADC)			Output place		
		Signal name	Trigger selector	Peripheral function		Signal name
Output	General-purpose trigger interrupt	INTADATRG	***[TSEL0CR9]*** <INSEL38[2:0]>	T32A ch5	Timer A internal trigger input	T32A05TRGINAPCK
	Single conversion interrupt	INTADASGL				
	Continuous conversion interrupt	INTADACNT				
	Monitor function0 interrupt	INTADACP0				
	Monitor function1 interrupt	INTADACP1				
	Monitor function0 output for PMD protect function	ADACP0L_N	-	PMD+ ch0	OVV state signal (AD monitor function0)	ADACMP0L_N
	Monitor function1 output for PMD protect function	ADACP1L_N	-		OVV state signal (AD monitor function1)	ADACMP1L_N

2.11. 8-bit Digital to Analog Converter (DAC)

2.11.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.42 DAC Built-in channel

Product	DAC Built-in channel (✓: Available, -: N/A)	
	ch0	ch1
M3H6	✓	✓
M3H5	✓	✓
M3H4	✓	-
M3H3	✓	-
M3H2	✓	-
M3H1	-	-
M3H0	-	-

2.11.2. Functional pin and a port

The functional terminal is assigned to the following ports.
There is also a channel which does not have a functional pin by a product.

Table 2.43 DAC Functional pin and a port

Channel	Functional pin (Signal name)	Port	Product table (✓: Available, -: N/A)						
			M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	DAC0	PG0	✓	✓	✓	✓	✓	-	-
ch1	DAC1	PG1	✓	✓	-	-	-	-	-

2.12. Voltage Detection Circuit (LVD)

2.12.1. Built-in List

The following table shows the built-in list for each product.

Table 2.44 LVD Built-in List

Product	Built-in LVD (✓:Available, -: N/A)
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.12.2. LVD Detection power supply

A voltage detecting circuit monitors the power supply of the following tables.

Table 2.45 LVD Detection power supply

LVD Detection power supply	Power supply name
Digital power source terminal	DVDD5A, DVDD5B, DVDD5C

2.13. 32-bit Timer Event Counter (T32A)

2.13.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.46 T32A Built-in channel

Product	T32A Built-in channel (✓: Available, -: N/A)					
	ch0	ch1	ch2	ch3	ch4	ch5
M3H6	✓	✓	✓	✓	✓	✓
M3H5	✓	✓	✓	✓	✓	✓
M3H4	✓	✓	✓	✓	✓	✓
M3H3	✓	✓	✓	✓	✓	✓
M3H2	✓	✓	✓	✓	✓	✓
M3H1	✓	✓	✓	✓	✓	✓
M3H0	✓	✓	✓	✓	✓	✓

2.13.2. Functional pin and port

The functional pin is assigned to the port of the following tables.
Please use exclusively the same functional pin currently assigned to plurality.
There is also a channel which does not have a functional pin by a product.

Table 2.47 T32A Functional pin and a port (1/2)

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	T32A00INA0	Input	PA1 / PM1	✓ / ✓	✓ / ✓	✓ /✓	✓ / -	✓ / -	✓ / -	✓ / -
	T32A00INA1	Input	PA2 / PM2	✓ / ✓	✓ / ✓	✓ /✓	✓ / -	✓ / -	✓ / -	✓ / -
	T32A00OUTA	Output	PA0 / PM0	✓ / ✓	✓ / ✓	✓ /✓	✓ / -	✓ / -	✓ / -	✓ / -
	T32A00INB0	Input	PA4 / PM4	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	T32A00INB1	Input	PA5 / PM5	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	T32A00OUTB	Output	PA3 / PM3	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	T32A00INC0	Input	PA1 / PM1	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -
	T32A00INC1	Input	PA2 / PM2	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -
	T32A00OUTC	Output	PA0 / PM0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -
ch1	T32A01INA0	Input	PB1 / PP1	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A01INA1	Input	PB2 / PP2	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	T32A01OUTA	Output	PB0 / PP0	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A01INB0	Input	PB4	✓	✓	✓	✓	✓	✓	-
	T32A01INB1	Input	PB5	✓	-	-	-	-	-	-
	T32A01OUTB	Output	PB3	✓	✓	✓	✓	✓	✓	-
	T32A01INC0	Input	PB1 / PP1	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A01INC1	Input	PB2 / PP2	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	T32A01OUTC	Output	PB0 / PP0	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -

Table 2.48 T32A Functional signal and a port (2/2)

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch2	T32A02INA0	Input	PC1 / PR1	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A02INA1	Input	PC2 / PR2	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A02OUTA	Output	PC0 / PR0	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A02INB0	Input	PC4	✓	✓	-	-	-	-	-
	T32A02INB1	Input	PC5	✓	✓	-	-	-	-	-
	T32A02OUTB	Output	PC3	✓	✓	✓	✓	✓	-	-
	T32A02INC0	Input	PC1 / PR1	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A02INC1	Input	PC2 / PR2	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
	T32A02OUTC	Output	PC0 / PR0	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -
ch3	T32A03INA0	Input	PJ1	✓	✓	✓	✓	✓	✓	✓
	T32A03INA1	Input	PJ2	✓	✓	✓	✓	✓	✓	✓
	T32A03OUTA	Output	PJ0	✓	✓	✓	✓	✓	✓	✓
	T32A03INB0	Input	PJ4	✓	✓	✓	✓	✓	✓	✓
	T32A03INB1	Input	PJ5	✓	✓	✓	✓	✓	✓	✓
	T32A03OUTB	Output	PJ3	✓	✓	✓	✓	✓	✓	✓
	T32A03INC0	Input	PJ1	✓	✓	✓	✓	✓	✓	✓
	T32A03INC1	Input	PJ2	✓	✓	✓	✓	✓	✓	✓
	T32A03OUTC	Output	PJ0	✓	✓	✓	✓	✓	✓	✓
ch4	T32A04INA0	Input	PK3	✓	✓	✓	✓	✓	✓	✓
	T32A04INA1	Input	PK4	✓	✓	✓	✓	✓	✓	-
	T32A04OUTA	Output	PK2	✓	✓	✓	✓	✓	✓	✓
	T32A04INB0	Input	PK6	✓	✓	✓	-	-	-	-
	T32A04INB1	Input	PK7	✓	✓	-	-	-	-	-
	T32A04OUTB	Output	PK5	✓	✓	✓	✓	✓	✓	-
	T32A04INC0	Input	PK3	✓	✓	✓	✓	✓	✓	✓
	T32A04INC1	Input	PK4	✓	✓	✓	✓	✓	✓	-
	T32A04OUTC	Output	PK2	✓	✓	✓	✓	✓	✓	✓
ch5	T32A05INA0	Input	PN1	✓	✓	✓	-	-	-	-
	T32A05INA1	Input	PN2	✓	✓	✓	-	-	-	-
	T32A05OUTA	Output	PN0	✓	✓	✓	-	-	-	-
	T32A05INB0	Input	PN4	✓	✓	-	-	-	-	-
	T32A05INB1	Input	PN5	✓	-	-	-	-	-	-
	T32A05OUTB	Output	PN3	✓	✓	✓	-	-	-	-
	T32A05INC0	Input	PN1	✓	✓	✓	-	-	-	-
	T32A05INC1	Input	PN2	✓	✓	✓	-	-	-	-
	T32A05OUTC	Output	PN0	✓	✓	✓	-	-	-	-

2.13.3. Clock for prescaler

The clock which a 32-bit Timer Event Counter shows in the following tables for prescaler is used.

Table 2.49 T32A Clock for prescaler

Clock for prescaler
ΦT0

2.13.4. Internal signal connection specification

The capture trigger signal which shows 32-bit Timer Event Counter in the following tables is connected.

The input trigger signal which has a register name in the trigger selector column of the following table should choose the input trigger used by a trigger selector.

2.13.4.1. TRGIN / UART / I²C / TSPI / A-ENC / ADC / ELOSC connection

Table 2.50 T32A Internal signal connection specification (1/3)

Channel			Trigger source		
	Timer	Capture trigger input Signal name	Trigger selector	Input trigger signal	Signal name
ch0	A	T32A00TRGINAPHCK (Other timer outputs)	-	-	-
		T32A00TRGINAPCK (Internal trigger input)	***[TSEL0CR5]*** <INSEL23[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin (Note2)	TRGIN1
				PN3 pin (Note3)	TRGIN2
				UART ch0 Transmission completion trigger	UART0TXTRG
				UART ch0 Reception completion trigger	UART0RXTRG
	B	T32A00TRGINBPHCK (Other timer outputs)	T32A ch0 Timer A Output		T32A00OUTA
		T32A00TRGINBPCK (Other timer inputs)	***[TSEL0CR6]*** <INSEL24[2:0]> (Note1)	T32A ch0 Timer register A0 match trigger	T32A00TRGOUTCMPA0
				T32A ch0 Timer register A1 match trigger	T32A00TRGOUTCMPA1
				T32A ch0 Timer A overflow trigger	T32A00TRGOUTOFA
				T32A ch0 Timer A underflow trigger	T32A00TRGOUTUFA
	C	T32A00TRGINCPHCK (Other timer outputs)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL25[2:0]> (Note1)	T32A ch5 Timer register C0 match trigger	T32A05TRGOUTCMPC0
				T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1
				T32A ch5 Timer C overflow trigger	T32A05TRGOUTOFC
				T32A ch5 Timer C underflow trigger	T32A05TRGOUTUFC
ch1	A	T32A01TRGINAPHCK (Other timer outputs)	-	-	-
		T32A01TRGINAPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL26[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin (Note2)	TRGIN1
				PN3 pin (Note3)	TRGIN2
				UART ch1 Transmission completion trigger	UART1TXTRG
				UART ch1 Reception completion trigger	UART1RXTRG
	B	T32A01TRGINBPHCK (Other timer outputs)	T32A ch1 Timer A Output		T32A01OUTA
		T32A01TRGINBPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL27[2:0]> (Note1)	T32A ch1 Timer register A0 match trigger	T32A01TRGOUTCMPA0
				T32A ch1 Timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 Timer A overflow trigger	T32A01TRGOUTOFA
				T32A ch1 Timer A underflow trigger	T32A01TRGOUTUFA
	C	T32A01TRGINCPHCK (Other timer outputs)	T32A ch0 Timer C Output		T32A00OUTC
		T32A01TRGINCPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL28[2:0]> (Note1)	T32A ch0 Timer register C0 match trigger	T32A00TRGOUTCMPC0
				T32A ch0 Timer register C1 match trigger	T32A00TRGOUTCMPC1
				T32A ch0 Timer C overflow trigger	T32A00TRGOUTOFC
				T32A ch0 Timer C underflow trigger	T32A00TRGOUTUFC

Note1: ***[TSEL0CRx]***<INSELx[2:0]> chooses the trigger source of internal triggering by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: There is no PA3 (TRGIN1) pin in M3H0.

Note3: There is no PN3 (TRGIN2) pin in M3H3 / M3H2 / M3H1 / M3H0.

Table 2.51 T32A Internal signal connection specification (2/3)

Channel			Trigger source		
	Timer	capture trigger input Signal name	Trigger selector	Input trigger signal	Signal name
ch2	A	T32A02TRGINAPHCK (Other timer outputs)	-	-	-
		T32A02TRGINAPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL29[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin (Note2)	TRGIN1
				PN3 pin (Note3)	TRGIN2
				UART ch2 Transmission completion trigger (Note4)	UART2TXTRG
				UART ch2 Reception completion trigger (Note4)	UART2RXTRG
				I^2C ch0 Interruption	INTI2C0
	B	T32A02TRGINBPHCK (Other timer outputs)	T32A ch2 Timer A Output		T32A02OUTA
		T32A02TRGINBPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL30[2:0]> (Note1)	T32A ch2 Timer register A0 match trigger	T32A02TRGOUTCMPA0
				T32A ch2 Timer register A1 match trigger	T32A02TRGOUTCMPA1
				T32A ch2 Timer A overflow trigger	T32A02TRGOUTOFA
				T32A ch2 Timer A underflow trigger	T32A02TRGOUTUFA
	C	T32A02TRGINCPHCK (Other timer outputs)	-	-	-
		T32A02TRGINCPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL31[2:0]> (Note1)	T32A ch1 Timer register C0 match trigger	T32A01TRGOUTCMPC0
				T32A ch1 Timer register C1 match trigger	T32A01TRGOUTCMPC1
				T32A ch1 Timer C overflow trigger	T32A01TRGOUTOFC
				T32A ch1 Timer C underflow trigger	T32A01TRGOUTUFC
ch3	A	T32A03TRGINAPHCK (Other timer outputs)	-	-	-
		T32A03TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL32[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin (Note2)	TRGIN1
				PN3 pin (Note3)	TRGIN2
				TSPI ch0 Transmit completion	TSPI0TXEND
				TSPI ch0 Receive completion	TSPI0RXEND
				I^2C ch1 Interruption	INTI2C1
				A-ENC ch0 Dividing pulse signal	ENC0TIMPLS
	B	T32A03TRGINBPHCK (Other timer outputs)	T32A ch3 Timer A Output		T32A03OUTA
		T32A03TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL33[2:0]> (Note1)	T32A ch3 Timer register A0 match trigger	T32A03TRGOUTCMPA0
				T32A ch3 Timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 Timer A overflow trigger	T32A03TRGOUTOFA
				T32A ch3 Timer A underflow trigger	T32A03TRGOUTUFA
	C	T32A03TRGINCPHCK (Other timer outputs)	T32A ch2 Timer C Output		T32A02OUTC
		T32A03TRGINCPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL34[2:0]> (Note1)	T32A ch2 Timer register C0 match trigger	T32A02TRGOUTCMPC0
				T32A ch2 Timer register C1 match trigger	T32A02TRGOUTCMPC1
				T32A ch2 Timer C overflow trigger	T32A02TRGOUTOFC
				T32A ch2 Timer C underflow trigger	T32A02TRGOUTUFC

Note1: ***[TSEL0CRx]***<INSELx[2:0]> chooses the trigger source of internal triggering by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: There is no PA3 (TRGIN1) pin in M3H0.

Note3: There is no PN3 (TRGIN2) pin in M3H3 / M3H2 / M3H1 / M3H0.

Note4: There is not ch2 of UART in M3H0

Table 2.52 T32A Internal signal connection specification (3/3)

Channel			Trigger source		
	Timer	capture trigger input Signal name	Trigger selector	Input trigger signal	Signal name
ch4	A	T32A04TRGINAPHCK (Other timer outputs)	-	-	-
		T32A04TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL35[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin (Note2)	TRGIN1
				PN3 pin (Note3)	TRGIN2
				TSPI ch1 Transmit completion (Note4)	TSPI1TXEND
				TSPI ch1 Receive completion (Note4)	TSPI1RXEND
				I^2C ch2 Interruption	INTI2C2
				ELOSC Low speed clock (Note5)	fs
	B	T32A04TRGINBPHCK (Other timer outputs)	T32A ch4 Timer A Output		T32A04OUTA
		T32A04TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL36[2:0]> (Note1)	T32A ch4 Timer register A0 match trigger	T32A04TRGOUTCMPA0
				T32A ch4 Timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 Timer A overflow trigger	T32A04TRGOUTOFA
				T32A ch4 Timer A underflow trigger	T32A04TRGOUTUFA
	C	T32A04TRGINCPHCK (Other timer outputs)	-	-	-
		T32A04TRGINCPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL37[2:0]> (Note1)	T32A ch3 Timer register C0 match trigger	T32A03TRGOUTCMPC0
				T32A ch3 Timer register C1 match trigger	T32A03TRGOUTCMPC1
				T32A ch3 Timer C overflow trigger	T32A03TRGOUTOFC
				T32A ch3 Timer C underflow trigger	T32A03TRGOUTUFC
ch5	A	T32A05TRGINAPHCK (Other timer outputs)	-	-	-
		T32A05TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL38[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin (Note2)	TRGIN1
				PN3 pin (Note3)	TRGIN2
				ADC unit A General-purpose trigger interrupt	INTADATRG
				ADC unit A Single conversion interrupt	INTADASGL
				ADC unit A Continuous conversion interrupt	INTADACNT
				ADC unit A Monitor function0 interrupt	INTADACP0
				ADC unit A Monitor function1 interrupt	INTADACP1
	B	T32A05TRGINBPHCK (Other timer outputs)	T32A ch5 Timer A Output		T32A05OUTA
		T32A05TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL39[2:0]> (Note1)	T32A ch5 Timer register A0 match trigger	T32A05TRGOUTCMPA0
				T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer A overflow trigger	T32A05TRGOUTOFA
				T32A ch5 timer A underflow trigger	T32A05TRGOUTUFA
	C	T32A05TRGINCPHCK (Other timer outputs)	T32A ch4 Timer C Output		T32A04OUTC
		T32A05TRGINCPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL40[2:0]> (Note1)	T32A ch4 Timer register C0 match trigger	T32A04TRGOUTCMPC0
				T32A ch4 Timer register C1 match trigger	T32A04TRGOUTCMPC1
				T32A ch4 Timer C overflow trigger	T32A04TRGOUTOFC
				T32A ch4 Timer C underflow trigger	T32A04TRGOUTUFC

Note1: ***[TSEL0CRx]***<INSELx[2:0]> chooses the trigger source of internal triggering by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: There is no PA3 (TRGIN1) pin in M3H0.

Note3: There is no PN3 (TRGIN2) pin in M3H3 / M3H2 / M3H1 / M3H0.

Note4: There is not ch1 of TSPI in M3H0.

Note5: There is not LOSC in M3H1 / M3H0.

2.13.4.2. Synchronous control connection specification

The timer synchronous connection specification of a 32-bit Timer Event Counter is shown in the following tables.

Table 2.53 T32A Synchronous control connection specification

Channel	Timer	Master		Timer	Slave	
		Function (Output)	Signal name		Function (input)	Signal name
0	A	Trigger output for synchronous start	T32A00SYNCSTARTOUTA	B	Synchronous start at trigger input	T32A00SYNCSTARTB
		Trigger output for synchronous stop	T32A00SYNCSTOPOUTA		Synchronous stop at trigger input	T32A00SYNCSTOPB
		Trigger output for synchronous reload	T32A00SYNCRELOADOUTA		Synchronous reload at trigger input	T32A00SYNCRELOADB
1	A	Trigger output for synchronous start	T32A01SYNCSTARTOUTA	B	Synchronous start at trigger input	T32A01SYNCSTARTB
		Trigger output for synchronous stop	T32A01SYNCSTOPOUTA		Synchronous stop at trigger input	T32A01SYNCSTOPB
		Trigger output for synchronous reload	T32A01SYNCRELOADOUTA		Synchronous reload at trigger input	T32A01SYNCRELOADB
2	A	Trigger output for synchronous start	T32A02SYNCSTARTOUTA	B	Synchronous start at trigger input	T32A02SYNCSTARTB
		Trigger output for synchronous stop	T32A02SYNCSTOPOUTA		Synchronous stop at trigger input	T32A02SYNCSTOPB
		Trigger output for synchronous reload	T32A02SYNCRELOADOUTA		Synchronous reload at trigger input	T32A02SYNCRELOADB
3	A	Trigger output for synchronous start	T32A03SYNCSTARTOUTA	B	Synchronous start at trigger input	T32A03SYNCSTARTB
		Trigger output for synchronous stop	T32A03SYNCSTOPOUTA		Synchronous stop at trigger input	T32A03SYNCSTOPB
		Trigger output for synchronous reload	T32A03SYNCRELOADOUTA		Synchronous reload at trigger input	T32A03SYNCRELOADB
4	A	Trigger output for synchronous start	T32A04SYNCSTARTOUTA	B	Synchronous start at trigger input	T32A04SYNCSTARTB
		Trigger output for synchronous stop	T32A04SYNCSTOPOUTA		Synchronous stop at trigger input	T32A04SYNCSTOPB
		Trigger output for synchronous reload	T32A04SYNCRELOADOUTA		Synchronous reload at trigger input	T32A04SYNCRELOADB
5	A	Trigger output for synchronous start	T32A05SYNCSTARTOUTA	B	Synchronous start at trigger input	T32A05SYNCSTARTB
		Trigger output for synchronous stop	T32A05SYNCSTOPOUTA		Synchronous stop at trigger input	T32A05SYNCSTOPB
		Trigger output for synchronous reload	T32A05SYNCRELOADOUTA		Synchronous reload at trigger input	T32A05SYNCRELOADB

2.13.5. Pulse count correspondence classified by product List

As the pulse count specification of a 32-bit Timer Event Counter is shown in the following tables, correspondence changes with products.

Table 2.54 T32A Pulse count support list

Channel	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	2-Phase pulse count 1 phase pulse count						
ch1	2-Phase pulse count 1 phase pulse count						1 phase pulse count (T32A01INC0 only)
ch2	2-Phase pulse count 1 phase pulse count						
ch3	2-Phase pulse count 1 phase pulse count						
ch4	2-Phase pulse count 1 phase pulse count						1 phase pulse count (T32A04INC0 only)
ch5	2-Phase pulse count 1 phase pulse count			-			

2.13.6. DMA request

The 32-bit Timer Event Counter has the DMA request shown in the following tables.

When there is mention of the register name in the trigger selector column of the table, please choose a demand to use with a trigger selector.

Table 2.55 T32A DMA request (1/2)

Channel	Demand	Signal name	Trigger selector	DMA demand channel		
					Single Transmission	Burst Transmission
ch0	DMA request at match A1 register	T32A00DMAREQCMPA1	***[TSEL0CR0]*** <INSEL1[2:0]>	17	-	✓
	DMA request at match C1 register	T32A00DMAREQCMPC1				
	DMA request at match B1 register	T32A00DMAREQCMPB1	***[TSEL0CR1]*** <INSEL4[2:0]>	20	-	✓
	DMA request at capture A0 register	T32A00DMAREQCAPA0	***[TSEL0CR1]*** <INSEL6[2:0]>	22	-	✓
	DMA request at capture A1 register	T32A00DMAREQCAPA1				
	DMA request at capture C0 register	T32A00DMAREQCAPC0				
	DMA request at capture C1 register	T32A00DMAREQCAPC1				
	DMA request at capture B0 register	T32A00DMAREQCAPB0	***[TSEL0CR2]*** <INSEL9[2:0]>	25	-	✓
	DMA request at capture B1 register	T32A00DMAREQCAPB1				
ch1	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR0]*** <INSEL1[2:0]>	17	-	✓
	DMA request at match C1 register	T32A01DMAREQCMPC1				
	DMA request at match B1 register	T32A01DMAREQCMPB1	***[TSEL0CR1]*** <INSEL4[2:0]>	20	-	✓
	DMA request at capture A0 register	T32A01DMAREQCAPA0	***[TSEL0CR1]*** <INSEL6[2:0]>	22	-	✓
	DMA request at capture A1 register	T32A01DMAREQCAPA1				
	DMA request at capture C0 register	T32A01DMAREQCAPC0				
	DMA request at capture C1 register	T32A01DMAREQCAPC1				
	DMA request at capture B0 register	T32A01DMAREQCAPB0	***[TSEL0CR2]*** <INSEL9[2:0]>	25	-	✓
	DMA request at capture B1 register	T32A01DMAREQCAPB1				

Note: ✓: Available, -: N/A

Table 2.56 T32A DMA demand (2/2)

Channel	Demand	Signal name	Trigger group selector	DMA demand channel		
					Single Transmission	Burst Transmission
ch2	DMA request at match A1 register	T32A02DMAREQCMPA1	***[TSEL0CR0]*** <INSEL2[2:0]>	18	-	✓
	DMA request at match C1 register	T32A02DMAREQCMPC1				
	DMA request at match B1 register	T32A02DMAREQCMPB1	***[TSEL0CR1]*** <INSEL4[2:0]>	20	-	✓
	DMA request at capture A0 register	T32A02DMAREQCAPA0	***[TSEL0CR1]*** <INSEL7[2:0]>	23	-	✓
	DMA request at capture A1 register	T32A02DMAREQCAPA1				
	DMA request at capture C0 register	T32A02DMAREQCAPC0				
	DMA request at capture C1 register	T32A02DMAREQCAPC1				
	DMA request at capture B0 register	T32A02DMAREQCAPB0	***[TSEL0CR2]*** <INSEL9[2:0]>	25	-	✓
	DMA request at capture B1 register	T32A02DMAREQCAPB1				
ch3	DMA request at match A1 register	T32A03DMAREQCMPA1	***[TSEL0CR0]*** <INSEL2[2:0]>	18	-	✓
	DMA request at match C1 register	T32A03DMAREQCMPC1				
	DMA request at match B1 register	T32A03DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5[2:0]>	21	-	✓
	DMA request at capture A0 register	T32A03DMAREQCAPA0	***[TSEL0CR1]*** <INSEL7[2:0]>	23	-	✓
	DMA request at capture A1 register	T32A03DMAREQCAPA1				
	DMA request at capture C0 register	T32A03DMAREQCAPC0				
	DMA request at capture C1 register	T32A03DMAREQCAPC1				
	DMA request at capture B0 register	T32A03DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10[2:0]>	26	-	✓
	DMA request at capture B1 register	T32A03DMAREQCAPB1				
ch4	DMA request at match A1 register	T32A04DMAREQCMPA1	***[TSEL0CR0]*** <INSEL3[2:0]>	19	-	✓
	DMA request at match C1 register	T32A04DMAREQCMPC1				
	DMA request at match B1 register	T32A04DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5[2:0]>	21	-	✓
	DMA request at capture A0 register	T32A04DMAREQCAPA0	***[TSEL0CR2]*** <INSEL8[2:0]>	24	-	✓
	DMA request at capture A1 register	T32A04DMAREQCAPA1				
	DMA request at capture C0 register	T32A04DMAREQCAPC0				
	DMA request at capture C1 register	T32A04DMAREQCAPC1				
	DMA request at capture B0 register	T32A04DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10[2:0]>	26	-	✓
	DMA request at capture B1 register	T32A04DMAREQCAPB1				
ch5	DMA request at match A1 register	T32A05DMAREQCMPA1	***[TSEL0CR0]*** <INSEL3[2:0]>	19	-	✓
	DMA request at match C1 register	T32A05DMAREQCMPC1				
	DMA request at match B1 register	T32A05DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5[2:0]>	21	-	✓
	DMA request at capture A0 register	T32A05DMAREQCAPA0	***[TSEL0CR2]*** <INSEL8[2:0]>	24	-	✓
	DMA request at capture A1 register	T32A05DMAREQCAPA1				
	DMA request at capture C0 register	T32A05DMAREQCAPC0				
	DMA request at capture C1 register	T32A05DMAREQCAPC1				
	DMA request at capture B0 register	T32A05DMAREQCAPB0	***[TSEL0CR2]*** <INSEL10[2:0]>	26	-	✓
	DMA request at capture B1 register	T32A05DMAREQCAPB1				

Note: ✓: Available, -: N/A

2.13.7. Non corresponding interruption

Every count interrupt (INTT32AxEVRYC) does not correspond in the TMPM3H group (1).

2.14. Real Time Clock (RTC)

2.14.1. Built-in List

The following table shows the built-in list for each product.

Table 2.57 RTC Built-in List

Product	Built-in RTC (✓:Abailable, -: N/A)
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	-
M3H0	-

2.14.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.58 RTC Functional pin and a port

Functional pin (Signal name)		Port	Product table (✓: Available, -: N/A)						
			M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
RTCOUT	Output	PC2	✓	✓	✓	✓	✓	-	-

Note: TMPM3H group (1) does not have an ALARM_N pin.

2.14.3. RTC count clock

The clock which shows the clock count clock of a real-time clock in the following tables is used.

Table 2.59 RTC Count clock

Count clock
fs

2.15. Asynchronous Serial Communication Circuit (UART)

2.15.1. Built-in channel

The built-in channel for every product is shown in the following table.
In M3H Group (1), Maximum Communication speed of UART is 2.5 Mbps.

Table 2.60 UART Built-in channel

Product	UART Built-in channel (✓: Available, -: N/A)		
	ch0	ch1	ch2
M3H6	✓	✓	✓
M3H5	✓	✓	✓
M3H4	✓	✓	✓
M3H3	✓	✓	✓
M3H2	✓	✓	✓
M3H1	✓	✓	✓
M3H0	✓	✓	-

2.15.2. Functional pin and port

The functional pin is assigned to the port of the following tables.
Please use exclusively the same functional pin currently assigned to plurality.
There is also a channel which does not have a functional pin by a product.

Table 2.61 UART Functional pin signal and a port

Channel	Functional pin (Signal name)		Port	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	UT0TXDA	Output	PA1 / PA2 / PM1 / PM2	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / - / -	✓ / ✓ / - / -	✓ / ✓ / - / -	✓ / ✓ / - / -
	UT0TXDB	Output	PA0 / PM0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -
	UT0RXD	Input	PA2 / PA1 / PM2 / PM1	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / - / -	✓ / ✓ / - / -	✓ / ✓ / - / -	✓ / ✓ / - / -
	UT0CTS_N	Input	PM3 / PM4	✓ / ✓	- / -	- / -	- / -	- / -	- / -	- / -
	UT0RTS_N	Output	PM4 / PM3	✓ / ✓	- / -	- / -	- / -	- / -	- / -	- / -
ch1	UT1TXDA	Output	PJ1 / PJ2 / PK1 / PK2	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓
	UT1TXDB	Output	PJ0 / PK0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	UT1RXD	Input	PJ2 / PJ1 / PK2 / PK1	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓
	UT1CTS_N	Input	PJ3 / PJ4 / PK3 / PK4	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / -
	UT1RTS_N	Output	PJ4 / PJ3 / PK4 / PK3	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / - / ✓
ch2	UT2TXDA	Output	PB2 / PB3 / PL0 / PL1	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / - / -	✓ / ✓ / - / -	- / - / - / -
	UT2TXDB	Output	-	-	-	-	-	-	-	-
	UT2RXD	Input	PB3 / PB2 / PL1 / PL0	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / ✓ / ✓	✓ / ✓ / - / -	✓ / ✓ / - / -	- / - / - / -
	UT2CTS_N	Input	PB4 / PB5 / PL2 / PL3	✓ / ✓ / ✓ / ✓	- / - / ✓ / ✓	- / - / ✓ / ✓	- / - / - / -	- / - / - / -	- / - / - / -	- / - / - / -
	UT2RTS_N	Output	PB5 / PB4 / PL3 / PL2	✓ / ✓ / ✓ / ✓	- / - / ✓ / ✓	- / - / ✓ / ✓	- / - / - / -	- / - / - / -	- / - / - / -	- / - / - / -

2.15.3. Half clock mode list for the each product

An asynchronous serial communication circuit does not have a half clock mode with a product, as shown in the following tables.

Table 2.62 UART Half clock mode adaptive list

Channel	Product table (✓: Available, -: N/A)						
	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	✓	✓	✓	✓	✓	✓	✓
ch1	✓	✓	✓	✓	✓	✓	✓
ch2	✓ (Note)	✓ (Note)	✓ (Note)	✓ (Note)	✓ (Note)	✓ (Note)	-

Note: Supports 1-pin mode only

2.15.4. Clock for prescaler

The clock which an asynchronous serial communication circuit shows in the following tables for prescaler is used.

Table 2.63 UART Clock for prescaler

Clock for prescaler
ΦT0

2.15.5. DMA request

An asynchronous serial communication circuit has the DMA request shown in the following tables.
"-" in a table does not have an applicable function.

Table 2.64 UART DMA request

Channel	Demand	Signal name	Trigger selector	DMA request channel		
					Single Transmission	Burst Transmission
ch0	Reception DMA request	UART0RX_DMAREQ	-	10	✓	✓
	Transmission DMA request	UART0TX_DMAREQ		11	✓	✓
ch1	Reception DMA request	UART1RX_DMAREQ	-	12	✓	✓
	Transmission DMA request	UART1TX_DMAREQ		13	✓	✓
ch2	Reception DMA request	UART2RX_DMAREQ	-	14	✓	✓
	Transmission DMA request	UART2TX_DMAREQ		15	✓	✓

Note: ✓: Available, -: N/A

2.15.6. Internal signal connection specification

2.15.6.1. Trigger transmission signal connection specification

An asynchronous serial communication circuit has a transmitting function by a trigger signal.
A trigger signal chooses and uses the trigger source shown in the following tables by a trigger selector.

Table 2.65 UART Trigger transmission signal connection specification

Channel	Signal name	Trigger source		
		Trigger selector	Input trigger signal	Signal name
ch0	UART0TRGIN (Input)	***[TSEL0CR5]*** <INSEL20[2:0]> (Note1)	PB1 pin	TRGIN0
			PA3 Pin (Note2)	TRGIN1
			PN3 pin (Note3)	TRGIN2
			T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1
ch1	UART1TRGIN (Input)	***[TSEL0CR5]*** <INSEL21[2:0]> (Note1)	PB1 pin	TRGIN0
			PA3 pin (Note2)	TRGIN1
			PN3 pin (Note3)	TRGIN2
			T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1
ch2	UART2TRGIN (Input)	***[TSEL0CR5]*** <INSEL22[2:0]> (Note1)	PB1 pin	TRGIN0
			PA3 pin (Note2)	TRGIN1
			PN3 pin (Note3)	TRGIN2
			T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 Timer register C1 match trigger r	T32A05TRGOUTCMPC1

Note1: ***[TSEL0CR5]***<INSELx[2:0]> chooses the trigger source of internal triggering by a trigger group selector.a detailed connection destination "2.2. Trigger Selector (TRGSEL)" please refer to it.

Note2: There is no PA3 (TRGIN1) pin in M3H0.

Note3: There is no PN3 (TRGIN2) pin in M3H3 / M3H2 / M3H1 / M3H0.

2.15.6.2. T32A connection

In addition to this, the asynchronous serial communication circuit is connected with the peripheral function inside, as shown in the following table.

Table 2.66 UART Internal connection specification: Output

Input /output	Functional Output		Trigger selector	Output place		
		Signal name		Peripheral function		Output place
Output	UART ch0 Transmission completion trigger	UART0TXTRG	***[TSEL0CR5]*** <INSEL23[2:0]>	T32A ch0	Timer A internal trigger input	T32A00TRGINAPCK
	UART ch0 Reception completion trigger	UART0RXTRG				
	UART ch1 Transmission completion trigger	UART1TXTRG	***[TSEL0CR6]*** <INSEL26[2:0]>	T32A ch1	Timer A internal trigger input	T32A01TRGINAPCK
	UART ch1 Reception completion trigger	UART1RXTRG				
	UART ch2 Transmission completion trigger	UART2TXTRG	***[TSEL0CR7]*** <INSEL29[2:0]>	T32A ch2	Timer A internal trigger input	T32A02TRGINAPCK
	UART ch2 Reception completion trigger	UART2RXTRG				

2.16. I²C interface (I²C)

2.16.1. Built-in channel

The built-in channel for each product is shown in the following table.

In the M3H group (1), the I²C interface supports Standard mode, Fast-mode and Fast-mode Plus.

Table 2.67 I²C interface Built-in channel

Product	I²C Built-in channel (✓: Available, -: N/A)		
	ch0	ch1	ch2
M3H6	✓	✓	✓
M3H5	✓	✓	✓
M3H4	✓	✓	✓
M3H3	✓	✓	✓
M3H2	✓	✓	-
M3H1	✓	✓	-
M3H0	✓	-	-

2.16.2. Functional pin and port

The functional pin is assigned to the port of the following tables.

Table 2.68 I²C Functional pin and port

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	I2C0SCL	Input/output	PC0	✓	✓	✓	✓	✓	✓	✓
	I2C0SDA	Input/output	PC1	✓	✓	✓	✓	✓	✓	✓
ch1	I2C1SCL	Input/output	PA4	✓	✓	✓	✓	✓	✓	-
	I2C1SDA	Input/output	PA5	✓	✓	✓	✓	✓	✓	-
ch2	I2C2SCL	Input/output	PL0	✓	✓	✓	✓	-	-	-
	I2C2SDA	Input/output	PL1	✓	✓	✓	✓	-	-	-

2.16.3. Clock for prescaler

The clock which an I²C interface shows in the following tables for prescaler is used.

Table 2.69 I²C Clock for prescaler

Clock for prescaler
fsys

2.16.4. Address match wakeup function support

As the address match wakeup function is shown in the following tables, correspondence changes with products.

Table 2.70 I^2C Address match wakeup function adaptive list

Channel	Product table (✓: Available, -: N/A)						
	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	✓	✓	✓	✓	✓	✓	✓
ch1	-	-	-	-	-	-	-
ch2	-	-	-	-	-	-	-

2.16.5. Filter selection

Filter support is shown in the table below. An analog filter is connected to channel 0 address match wakeup function (I2CS).

Table 2.71 I^2C interface filter

Channel		Filter type
ch0		Digital
	I2CS	Analog
ch1		Digital
ch2		Digital

2.16.6. DMA request

An I²C interface has the DMA request shown in the following tables.
"-" in a table does not have an applicable function.

Table 2.72 I²C DMA request

Channel	Demand	Signal name	Trigger selector	DMA request channel		
					Single Transmission	Burst Transmission
ch0	Receiving DMA request	I2C0RXDMAREQ	-	4	-	✓
	Transmitting DMA request	I2C0TXDMAREQ		5	-	✓
ch1	Receiving DMA request	I2C1RXDMAREQ	-	6	-	✓
	Transmitting DMA request	I2C1TXDMAREQ		7	-	✓
ch2	Receiving DMA request	I2C2RXDMAREQ	-	8	-	✓
	Transmitting DMA request	I2C2TXDMAREQ		9	-	✓

Note: ✓: Available, -: N/A

2.17. Serial Peripheral Interface (TSPI)

2.17.1. Built-in channel

The built-in channel for each product is shown in the following table.
In M3H Group (1), Maximum Communication speed of TSPI is 20 Mbps.

Table 2.73 TSPI Built-in channel

Product	TSPI Built-in channel (✓: Available, -: N/A)	
	ch0	ch1
M3H6	✓	✓
M3H5	✓	✓
M3H4	✓	✓
M3H3	✓	✓
M3H2	✓	✓
M3H1	✓	✓
M3H0	✓	-

2.17.2. Functional pin and port

The functional pin is assigned to the port below.
Please use exclusively the same functional pin currently assigned to plurality.
There is also a channel which does not have a functional pin by a product.

Table 2.74 TSPI Functional pin and a port

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	TSPI0SCK	Input/output	PA0 / PM0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -
	TSPI0TXD	Output	PA1 / PM1	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -
	TSPI0RXD	Input	PA2 / PM2	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -
	TSPI0CSIN	Input	PA3 / PM3	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	TSPI0CS0	Output	PA3 / PM3	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	TSPI0CS1	Output	PA4 / PM4	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	✓ / -	-/-
ch1	TSPI1SCK	Input/output	PB2 / PP0	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	TSPI1TXD	Output	PB3 / PP1	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	TSPI1RXD	Input	PB4 / PP2	✓ / ✓	✓ / ✓	✓ / -	✓ / -	✓ / -	✓ / -	-/-
	TSPI1CSIN	Input	PB5 / PL6	✓ / ✓	-/-	-/-	-/-	-/-	-/-	-/-
	TSPI1CS0	Output	PB5 / PL6	✓ / ✓	-/-	-/-	-/-	-/-	-/-	-/-
	TSPI1CS1	Output	PB6 / PL5	✓ / ✓	-/-	-/-	-/-	-/-	-/-	-/-

Note: M3H group (1) does not have TSPIxCS2 pin / TSPIxCS3 pin.

2.17.3. Transfer mode list for the each product

The transfer modes which can be used with a product as a serial peripheral interface is shown in the following tables differ.

Table 2.75 TSPI Mode support list

Channel	Mode support						
	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
ch0	SPI mode SIO mode						SIO mode
ch1	SPI mode SIO mode	SIO mode					-

2.17.4. *[TSPIxCR2]*<RXDLY> set value

For the setting value of TSPI control register 2 (***[TSPIxCR2]*** <RXDLY>), set the values in the following table.

Table 2.76 TSPI *[TSPIxCR2]*<RXDLY> set value

Register name	Value
[TSPIxCR2]<RXDLY>	0

2.17.5. Clock

The clock which a serial peripheral interface shows in the following tables for clock is used.

Table 2.77 TSPI Clock

Operation clock	Clock for prescaler
fsys	ΦT0

2.17.6. DMA request

A serial peripheral interface has the DMA request shown in the following tables.

"-" in a table does not have an applicable function.

Table 2.78 TSPI DMA request

Channel	Demand	Signal name	Trigger selector	DMA demand channel		
					Single Transmission	Burst Transmission
ch0	Receive DMA request	TSPI0RX_DMA	-	0	✓	✓
	Transmit DMA request	TSPI0TX_DMA		1	✓	✓
ch1	Receive DMA request	TSPI1RX_DMA	-	2	✓	✓
	Transmit DMA request	TSPI1TX_DMA		3	✓	✓

Note: ✓: Available, -: N/A

2.17.7. Internal signal connection specification

A serial peripheral interface has a transmitting function by a trigger signal.

A trigger signal chooses and uses the trigger source shown in the following tables by a trigger selector.

2.17.7.1. Trigger transmitting signal connection specification

Table 2.79 TSPI Trigger transmission specification

Channel	Signal name	Trigger source		
		Trigger selector	Input trigger signal	Signal name
ch0	TSPI0TRG (Input)	***[TSEL0CR4]*** <INSEL18[2:0]> (Note1)	PB1 pin	TRGIN0
			PA3 pin (Note2)	TRGIN1
			PN3 pin (Note3)	TRGIN2
			T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPC1
ch1	TSPI1TRG (Input)	***[TSEL0CR4]*** <INSEL19[2:0]> (Note1)	PB1 pin	TRGIN0
			PA3 pin (Note2)	TRGIN1
			PN3 pin (Note3)	TRGIN2
			T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 Timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1

Note1: ***[TSEL0CR4]***<INSELx[2:0]> chooses the trigger source of internal triggering by a trigger group selector.a detailed connection destination "2.2. Trigger Selector (TRGSEL)" please refer to it.

Note2: There is no PA3 (TRGIN1) pin in M3H0.

Note3: There is no PN3 (TRGIN2) pin in M3H3 / M3H2 / M3H1 / M3H0.

2.17.7.2. T32A connection

In addition to this, the serial peripheral interface is connected with the peripheral function inside, as shown in the following table.

Table 2.80 TSPI Internal connection specification (Output)

Input/output	Functional Output		Trigger selector			
		Signal name		Peripheral function	Input Signal	Signal name
Output	TSPI ch0 Transmit Completion	TSPI0TXEND	***[TSEL0CR8]*** <INSEL32[2:0]>	T32A ch3	Timer A internal trigger input	T32A03TRGINAPCK
	TSPI ch0 receiving Completion signal	TSPI0RXEND				
	TSPI ch1 Transmit Completion	TSPI1TXEND	***[TSEL0CR8]*** <INSEL35[2:0]>	T32A ch4	Timer A internal trigger input	T32A04TRGINAPCK
	TSPI ch1 Receive Completion	TSPI1RXEND				

2.18. Remote Control Signal Preprocessor (RMC)

2.18.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.81 RMC Built-in channel

Product	RMC Built-in channel (✓: Available, -: N/A)
	ch0
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.18.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.82 RMC Functional pin and a port

Functional pin (Signal name)		Port	Product table (✓: Available, -: N/A)						
			M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
RXIN0	Input	PB1	✓	✓	✓	✓	✓	✓	✓

2.18.3. Sampling clock

The remote control receiving circuit can choose the sampling clock shown in the following tables.

Table 2.83 RMC Sampling clock

Clock		Clock source	
	Signal name		Signal name
Low speed clock	fs	External low speed oscillator	fs
Timer trigger for clock source	TB0OUT	T32A ch5 timer output A	T32A05OUTA

Note: Please choose the sampling clock by ***[RMC0FSSEL]*** <RMCCLK>.

2.19. Digital Noise Filter Circuit (DNF)

2.19.1. Built-in unit

The built-in unit for each product is shown in the following table.

Table 2.84 DNF Built-in unit

Product	DNF Built-in unit (✓: Available, -: N/A)
	unit A
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.19.2. External interrupt pin and DNF

Digital noise filter circuits correspond to the following external interruption pins.

Table 2.85 External interruption pin and DNF correspondence

External interruption Pin (signal name)	Port	Unit	Setup Register name	Product table (✓: Available, -: N/A)						
				M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
INT00	PC0	A	***[DNFAENCR]***<NFEN0>	✓	✓	✓	✓	✓	✓	✓
INT01	PC1		***[DNFAENCR]***<NFEN1>	✓	✓	✓	✓	✓	✓	✓
INT02	PC2		***[DNFAENCR]***<NFEN2>	✓	✓	✓	✓	✓	✓	✓
INT03	PB1		***[DNFAENCR]***<NFEN3>	✓	✓	✓	✓	✓	✓	✓
INT04	PJ4		***[DNFAENCR]***<NFEN4>	✓	✓	✓	✓	✓	✓	✓
INT05	PK1		***[DNFAENCR]***<NFEN5>	✓	✓	✓	✓	✓	✓	✓
INT06	PH3		***[DNFAENCR]***<NFEN6>	✓	✓	✓	✓	✓	-	-
INT07	PA6		***[DNFAENCR]***<NFEN7>	✓	✓	✓	✓	-	-	-
INT08	PL3		***[DNFAENCR]***<NFEN8>	✓	✓	✓	-	-	-	-
INT09	PM2		***[DNFAENCR]***<NFEN9>	✓	✓	✓	-	-	-	-
INT10	PN3		***[DNFAENCR]***<NFEN10>	✓	✓	✓	-	-	-	-
INT11	PA7		***[DNFAENCR]***<NFEN11>	✓	✓	-	-	-	-	-
INT12	PL4		***[DNFAENCR]***<NFEN12>	✓	✓	-	-	-	-	-
INT13	PK7		***[DNFAENCR]***<NFEN13>	✓	✓	-	-	-	-	-
INT14	PP3		***[DNFAENCR]***<NFEN14>	✓	✓	-	-	-	-	-
INT15	PM6		***[DNFAENCR]***<NFEN15>	✓	-	-	-	-	-	-

2.19.3. Sampling source clock

The clock in which the digital noise filter circuit is shown as a sauce clock of the sampling at following table is used.

Table 2.86 DNF Sampling source clock

Sampling source clock
fc

2.20. Boundary scan (BSC)

2.20.1. Functional support

The functional support for each product is shown in the following table.

Table 2.87 Boundary scan functional support

Product	Boundary scan functional support (✓: Available, -: N/A)
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	-
M3H1	-
M3H0	-

2.20.2. JTAG interface according to the product

Table 2.88 JTAG interface Loading list

Debugging pin (Signal name)	Port	Product table (✓: Available, -: N/A)						
		M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
TMS	PK2	✓	✓	✓	✓	-	-	-
TCK	PK3	✓	✓	✓	✓	-	-	-
TDO	PK4	✓	✓	✓	✓	-	-	-
TDI	PK5	✓	✓	✓	✓	-	-	-
TRST_N	PK6	✓	✓	✓	-	-	-	-
BSC	-	✓	✓	✓	✓	-	-	-

2.20.3. Boundary scan order

An order of a boundary scan over the signal processor of this product is as follows.

Table 2.89 Boundary scan order (1/3)

Order	Function name or a port name	Product table (✓: Available, -: N/A)			
		M3H6	M3H5	M3H4	M3H3
-	TDI	✓	✓	✓	✓
1	PK1	✓	✓	✓	✓
2	PK0	✓	✓	✓	✓
3	PJ5	✓	✓	✓	✓
4	PJ4	✓	✓	✓	✓
5	PJ3	✓	✓	✓	✓
6	PJ2	✓	✓	✓	✓

Table 2.90 Boundary scan order (2/3)

Order	Function name or a port name	Product table (✓: Available, -: N/A)			
		M3H6	M3H5	M3H4	M3H3
7	PJ1	✓	✓	✓	✓
8	PJ0	✓	✓	✓	✓
9	PN0	✓	✓	✓	-
10	PN1	✓	✓	✓	-
11	PN2	✓	✓	✓	-
12	PN3	✓	✓	✓	-
13	PN4	✓	✓	-	-
14	PN5	✓	-	-	-
15	PR3	✓	-	-	-
16	PR2	✓	-	-	-
17	PR1	✓	-	-	-
18	PR0	✓	-	-	-
19	PC6	✓	✓	-	-
20	PC5	✓	✓	-	-
21	PC4	✓	✓	-	-
22	PC3	✓	✓	✓	✓
23	PC2	✓	✓	✓	✓
24	PC1	✓	✓	✓	✓
25	PC0	✓	✓	✓	✓
26	PH3	✓	✓	✓	✓
27	PH2	✓	✓	✓	✓
28	PH1	✓	✓	✓	✓
29	PH0	✓	✓	✓	✓
30	PP2	✓	✓	-	-
31	PP1	✓	✓	-	-
32	PP0	✓	✓	-	-
33	PL6	✓	-	-	-
34	PL5	✓	-	-	-
35	PL4	✓	✓	-	-
36	PL3	✓	✓	✓	-
37	PL2	✓	✓	✓	-
38	PL1	✓	✓	✓	✓
39	PL0	✓	✓	✓	✓
40	PB7	✓	-	-	-
41	PB6	✓	-	-	-
42	PB5	✓	-	-	-
43	PB4	✓	✓	✓	✓
44	PB3	✓	✓	✓	✓
45	PB2	✓	✓	✓	✓
46	PB1	✓	✓	✓	✓
47	PB0	✓	✓	✓	✓
48	PM0	✓	✓	✓	-
49	PM1	✓	✓	✓	-

Table 2.91 Boundary scan order (3/3)

Order	Function name or port name	Product table (✓: Available, -: N/A)			
		M3H6	M3H5	M3H4	M3H3
50	PM2	✓	✓	✓	-
51	PM3	✓	-	-	-
52	PM4	✓	-	-	-
53	PM5	✓	-	-	-
54	PM6	✓	-	-	-
55	PA0	✓	✓	✓	✓
56	PA1	✓	✓	✓	✓
57	PA2	✓	✓	✓	✓
58	PA3	✓	✓	✓	✓
59	PA4	✓	✓	✓	✓
60	PA5	✓	✓	✓	✓
61	PA6	✓	✓	✓	✓
62	PA7	✓	✓	-	-
63	PG1	✓	✓	-	-
64	PG0	✓	✓	✓	✓
65	PD0	✓	✓	✓	✓
66	PD1	✓	✓	✓	✓
67	PD2	✓	✓	✓	✓
68	PD3	✓	-	-	-
69	PE0	✓	✓	✓	✓
70	PE1	✓	✓	✓	✓
71	PE2	✓	✓	✓	✓
72	PE3	✓	✓	✓	✓
73	PE4	✓	✓	✓	✓
74	PE5	✓	✓	-	-
75	PE6	✓	✓	-	-
76	PF0	✓	-	-	-
77	PF1	✓	-	-	-
78	PF2	✓	-	-	-
79	PF3	✓	-	-	-
80	PF4	✓	-	-	-
81	PP3	✓	✓	-	-
82	PK7	✓	✓	-	-
-	TDO	✓	✓	✓	✓

2.21. Trimming Circuit (TRM)

2.21.1. Built-in List

The following table shows the built-in list for each product.

Table 2.92 TRM Built-in List

Product	Built-in TRM (✓:Available, -: N/A)
M3H6	✓
M3H5	✓
M3H4	✓
M3H3	✓
M3H2	✓
M3H1	✓
M3H0	✓

2.21.2. Object oscillator

The object oscillator of a trimming circuit is an oscillator shown in the following tables.

Table 2.93 TRM Trimming oscillator

Object oscillator	Oscillator name
Internal High Speed Oscillator 1	IHOSC1

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2017-09-08	First release
2.0	2018-03-15	Corrected: Item column of the table "ch"->"channel" Related document: Corrected (IP symbol addition, others.) Terms and Abbreviation: Revised 2.1. Register Base Address Corrected: "If TYPE 1/2 is not mentioned in the register base address of the reference manual, please use it as TYPE 1." 2.2. Trigger Selector (TRGSEL) Corrected: "Figure 2.1 the example of trigger selector connection is the example in which the trigger signal (port terminals (PB1, PA3) and DMAC (ch18, ch20, ch23, and ch25)) are connected to the DMAC (ch30) via the trigger selector." 2.2.1. Trigger selector and product table Added: Table 2.2,2.3 (Add the DMAC unit number in the trigger source column.) 2.2.2. Directions for use and setup Corrected: "For the selected input trigger signal, select detection of rising edge or falling edge." Corrected: "To select the edge detection condition, set with the edge detection condition bit (***[TSEL0CRn]*** <UPDNm>) of the control register." 2.2.4.1. ***[TSEL0CR0]*** (Control Register 0) to 2.2.4.11. ***[TSEL0CR10]*** (Control Register 10) Added: Add trigger source name to the function column of Bit Symbol INSELx (41 places). 2.3.2. Count clock Corrected: Table 2.11 Selection column "***[SIWDMOD]***"->"***[SIWD0MOD]***" 2.4.1. Support products Added: section "2.4.1. Support products" 2.4.2. Reference clock Added: Table 2,14 (Divide value) 2.5.1. Debugging interface terminal list of each product. Corrected: Table 2.16 2.8.2. Functional pin and port Deleted: Table 2.27 Channel column "PMD+" 2.8.3. DMA request Deleted: Table 2.28 Channel column "PMD+" 2.9.2. Functional pin and port Deleted: Table 2.32 Channel column "A-ENC" 2.9.3.1. T32A / PMD+ connection Corrected: "T32A / PMD connection"->"T32A / PMD+ connection" 2.10.5. DMA request Corrected: Table 2.39 Unit column "ADC"->"Unit A" 2.10.6.1. Start-trigger connection specification Corrected: Table 2.40 Note1: "***[TSEL0CRx]***"->"***[TSEL0CR4]***" 2.11.2. Functional pin and a port Deleted: Table 2.43 Channel column "DAC" 2.12.1. Support products Added: section "2.12.1. Support products" 2.13. 32-bit Timer Event Counter (T32A) Deleted: Channel column of table. "T32A" 2.13.2. Functional pin and port Corrected: Table 2.48 ch2 Line of Functional pin

		2.13.4.1. TRGIN / UART / I²C / TSPI / A-ENC / ADC / ELOSC connection Deleted: Timer column of table. "Timer" 2.14.1. Support products Corrected: "2.14.1. Built-in channel"->"2.14.1. Support products" Corrected: Table title "Table 2.57 RTC Built-in channel" ->"Table 2.57 RTC support product" Corrected: Table 2.57 2.15. Asynchronous Serial Communication Circuit (UART) Deleted: Channel column of table. "UART" 2.15.1. Built-in channel Added: "In M3H Group (1), Maximum Communication speed of UART is 2.5 Mbps." 2.15.5. DMA request Deleted: Table 2.64 Demand column "UART ch0","UART ch1","UART ch2" 2.15.6.1. Trigger transmission signal connection specification Corrected: Table 2.65 Note1: "***[TSEL0CRx]***"->"***[TSEL0CR5]***" 2.16. I²C interface (I²C) Deleted: Channel column of table. "I²C" 2.16.1. Built-in channel Added: "In the M3H group (1), the I²C interface supports Standard mode, Fast-mode and Fast-mode Plus." 2.16.5. Filter selection Corrected: "Filter support is shown in the table below. An analog filter is connected to channel 0 wakeup function (I2CS)." Corrected: Table 2.71 2.16.6. DMA request Deleted: Table 2.72 Demand column "I²C ch0","I²C ch1","I²C ch2" 2.17. Serial Peripheral Interface (TSPI) Deleted: Channel column of table. "TSPI" 2.17.1. Built-in channel Added: "In M3H Group (1), Maximum Communication speed of TSPI is 20 Mbps." 2.17.2. Functional pin and port Corrected: Table74 Function terminal column TSPI0CS0, TSPI0CS1, TSPI1CS0, TSPI1CS1 "Input"->"Output" 2.17.4. ***[TSPIxCR2]***<RXDLY> set value Added: section "2.17.4. ***[TSPIxCR2]***<RXDLY> set value" 2.17.6. DMA request Deleted: Table 2.78 Demand column "TSPI ch0","TSPI ch1","TSPI ch2" Corrected: Table 2.79 Note1: "***[TSEL0CRx]***"->"***[TSEL0CR4]***" 2.21.1. Support products Added: section "2.21.1. Support products"
2.1	2019-02-28	2.2.2 Directions for use and setup Deleted description of ***[CGFCEN]*** register 2.4.1 Built-in List Modified chapter title, explanation and table title 2.12.1 Built-in List Modified chapter title, explanation and table title 2.13.6 Pulse count correspondence classified by product List Corrected pin name of M3H0(ch1,ch4) in Table2.54 2.14.1 Built-in List Modified chapter title, explanation and table title 2.16.4 Address match wakeup function support Modified chapter title 2.16.5 Filter Selection Modified Wakeup function to Address match wakeup function 2.17.5 Clock Modified chapter title. Added operation clock in Table2.77. 2.20 Boundary scan(BSC)

		Modified chapter title. 2.21.1 Built-in List Modified chapter title, explanation and table title
2.2	2019-07-23	- Overall: Modified "Monitor function interrupt0" to "Monitor function0 interrupt" Modified "Monitor function interrupt1" to "Monitor function1 interrupt" Modified "Monitor function output0" to "Monitor function0 output" Modified "Monitor function output1" to "Monitor function1 output" - Conventions Updated trademark - Terms and Abbreviation Added BSC - 2.2.1. Trigger selector and product table Table 2.4 Trigger Source: Modified "PMDTRG6" to "ADC unit A" Modified "PMD+ general-purpose trigger" to "ADC unit A" Table 2.7, Table 2.8 Input Trigger: Modified "I^2C interruption" to "Interruption" - 2.2.4.5. ***[TSEL0CR4]*** (Control Register 4) Function: Modified "PMD+ General Purpose Trigger" to "ADC unit A" Modified "PMDTRG6" to "ADC unit A" - 2.6.2. The code flash block configuration of each product. Table 2.18 1st row: Modified "M3H0FSUG" to " M3H0FSDUG" Table 2.19 1st row: Modified "M3H3FxFG" to " M3H6FxFG" Modified "M3H0FxUG" to " M3H0FxDUG" - 2.8.4.1. ADC/A-ENC/T32A connection Table 2.29 Function input: Modified "monitoring function" to "monitor function" - 2.9.3.1. T32A / PMD+ connection Table 2.34 Output place: Modified "ENC" to "A-ENC" - 2.13.4.1. TRGIN / UART / I^2C / TSPI / A-ENC / ADC / ELOSC connection Table 2.51 Input trigger signal: Modified "I^2C interruption" to "Interruption" - 2.15.3. Half clock mode list for the each product Table 2.62 ch2 row: Modified "-" to "✓ (Note)" in M3H6,M3H5,M3H4,M3H3,M3H2,M3H1 Added "Note: Supports 1-pin mode only" - 2.17.3. Transfer mode list for the each product Table 2.75 ch0 row: Modified to "SIO mode" in M3H0 - 2.20.2. JTAG interface according to the product Table 2.88 TMS,TCK,TDO,TDI rows: Modified "✓" to "-" in M3H2 and M3H1

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**