32-bit RISC Microcontroller

TMPM3H Group(1)

Reference Manual
Input/Output Ports
(PORT-M3H(1))

Revision 2.2

2019-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

JTAG	Joint Test Action Group
SW	Serial Wire

1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

Table 1.1 Features

Function Classification	Function	Description
Port	-	Programmable pull-up/Programmable pull-down/Open-drain output are possible.
Peripheral Function pins	Clock Output	SCOUT pin
	External Interrupt	External Interrupt pin has a noise filter(Filter width 30ns Typ.).
	32bit Timer Event Counter	External trigger Input pin. Timer output pin.
	Real Time Clock	1Hz clock pin
	Serial Peripheral Interface	Chip select input for slave operation 1 pin, Chip select 2 pins, Serial data of transmission pin, Serial data reception pin, Serial clock input/output pin
	Asynchronous Serial Communication Circuit	Data input pin, Data output 2 pins, Request to send signal pin, Clear to send signal pin.
	I^2C Interface	SCL signal pin, SDA signal pin
	Remote Control Signal	Remote control data entry pin
	Analog Digital Convertor	Analog input pin
	Digital Analog Convertor	DAC output pin
	Motor Control Circuit	X/Y/Z phase output pins, U/V/W phase output pins, EMG detection input pin, Overvoltage detection input pin.
	Encoder Input Circuit	Encoder input pins
	Trigger Input	External trigger input pins
Debug pins	JTAG	JTAG Test select input pin, JTAG Serial clock input pin, JTAG Serial data output pin, JTAG Serial data input pin, JTAG Test reset input pin
	SW	Serial wire data input/output pin, Serial wire clock input pin, Serial wire viewer output pin
	Trace	Trace clock pin, Trace data 4pins.
Control pins	High speed clock	High speed oscillator connection pin, External clock input
	Low speed clock	Low speed oscillator connection pin
	BOOT mode control	BOOT mode control pin

2. Function

2.1. Clock supply

When PORT is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]***), fsys supply stop register B (***[CGFSYSENB]***). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in Reference manual.

3. Signal connection list

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal connection list (1/7)

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
Asynchronous Serial Communication Circuit	UT0RXD	PA2	16	18	15	11	11	10	9	5
		PA1	17	19	16	12	12	11	10	6
		PM2	23	25	18	14	-	-	-	-
		PM1	24	26	19	15	-	-	-	-
	UT0TXDB	PA0	18	20	17	13	13	12	11	7
		PM0	25	27	20	16	-	-	-	-
	UT0TXDA	PA1	17	19	16	12	12	11	10	6
		PA2	16	18	15	11	11	10	9	5
		PM1	24	26	19	15	-	-	-	-
		PM2	23	25	18	14	-	-	-	-
	UT0CTS_N	PM3	22	24	-	-	-	-	-	-
		PM4	21	23	-	-	-	-	-	-
	UT0RTS_N	PM4	21	23	-	-	-	-	-	-
		PM3	22	24	-	-	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Asynchronous Serial Communication Circuit	UT1RXD	PJ2	73	75	58	46	37	34	30	23
		PJ1	72	74	57	45	36	33	29	22
		PK2	79	81	64	52	43	40	36	29
		PK1	78	80	63	51	42	39	35	28
	UT1TXDB	PJ0	71	73	56	44	35	32	28	21
		PK0	77	79	62	50	41	38	34	27
	UT1TXDA	PJ1	72	74	57	45	36	33	29	22
		PJ2	73	75	58	46	37	34	30	23
		PK1	78	80	63	51	42	39	35	28
		PK2	79	81	64	52	43	40	36	29
	UT1CTS_N	PJ3	74	76	59	47	38	35	31	24
		PJ4	75	77	60	48	39	36	32	25
		PK3	80	82	65	53	44	41	37	-
		PK4	81	83	66	54	45	42	38	-
	UT1RTS_N	PJ4	75	77	60	48	39	36	32	25
		PJ3	74	76	59	47	38	35	31	24
		PK4	81	83	66	54	45	42	38	-
		PK3	80	82	65	53	44	41	37	-

Table 3.2 Signal connection list (2/7)

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
Asynchronous Serial Communication Circuit	UT2RXD	PB3	29	31	24	20	17	16	15	-
		PB2	28	30	23	19	16	15	14	-
		PL1	35	37	27	23	20	-	-	-
		PL0	34	36	26	22	19	-	-	-
	UT2TXDA	PB2	28	30	23	19	16	15	14	-
		PB3	29	31	24	20	17	16	15	-
		PL0	34	36	26	22	19	-	-	-
		PL1	35	37	27	23	20	-	-	-
	UT2CTS_N	PB4	30	32	-	-	-	-	-	-
		PB5	31	33	-	-	-	-	-	-
		PL2	36	38	28	24	-	-	-	-
		PL3	37	39	29	25	-	-	-	-
	UT2RTS_N	PB5	31	33	-	-	-	-	-	-
		PB4	30	32	-	-	-	-	-	-
		PL3	37	39	29	25	-	-	-	-
		PL2	36	38	28	24	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
I^2C Interface	I2C0SDA	PC1	55	57	45	37	32	29	26	19
	I2C0SCL	PC0	54	56	44	36	31	28	25	18
	I2C1SDA	PA5	13	15	12	8	8	7	6	-
	I2C1SCL	PA4	14	16	13	9	9	8	7	-
	I2C2SDA	PL1	35	37	27	23	20	-	-	-
	I2C2SCL	PL0	34	36	26	22	19	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Serial Peripheral Interface	TSPI0CSIN	PM3	22	24	-	-	-	-	-	-
		PA3	15	17	14	10	10	9	8	-
	TSPI0CS0	PM3	22	24	-	-	-	-	-	-
		PA3	15	17	14	10	10	9	8	-
	TSPI0CS1	PM4	21	23	-	-	-	-	-	-
		PA4	14	16	13	9	9	8	7	-
	TSPI0RXD	PM2	23	25	18	14	-	-	-	-
		PA2	16	18	15	11	11	10	9	5
	TSPI0TXD	PM1	24	26	19	15	-	-	-	-
		PA1	17	19	16	12	12	11	10	6
	TSPI0SCK	PM0	25	27	20	16	-	-	-	-
		PA0	18	20	17	13	13	12	11	7

Table 3.3 Signal connection list (3/7)

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
Serial Peripheral Interface	TSPI1CSIN	PL6	40	42	-	-	-	-	-	-
		PB5	31	33	-	-	-	-	-	-
	TSPI1CS0	PL6	40	42	-	-	-	-	-	-
		PB5	31	33	-	-	-	-	-	-
	TSPI1CS1	PL5	39	41	-	-	-	-	-	-
		PB6	32	34	-	-	-	-	-	-
	TSPI1RXD	PP2	43	45	33	-	-	-	-	-
		PB4	30	32	25	21	18	17	16	-
	TSPI1TXD	PP1	42	44	32	-	-	-	-	-
		PB3	29	31	24	20	17	16	15	-
	TSPI1SCK	PP0	41	43	31	-	-	-	-	-
		PB2	28	30	23	19	16	15	14	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
32-bit Timer Event Counter	T32A00INA0	PA1	17	19	16	12	12	11	10	6
		PM1	24	26	19	15	-	-	-	-
	T32A00INA1	PA2	16	18	15	11	11	10	9	5
		PM2	23	25	18	14	-	-	-	-
	T32A00OUTA	PA0	18	20	17	13	13	12	11	7
		PM0	25	27	20	16	-	-	-	-
	T32A00INB0	PA4	14	16	13	9	9	8	7	-
		PM4	21	23	-	-	-	-	-	-
	T32A00INB1	PA5	13	15	12	8	8	7	6	-
		PM5	20	22	-	-	-	-	-	-
	T32A00OUTB	PA3	15	17	14	10	10	9	8	-
		PM3	22	24	-	-	-	-	-	-
	T32A00INC0	PA1	17	19	16	12	12	11	10	6
		PM1	24	26	19	15	-	-	-	-
	T32A00INC1	PA2	16	18	15	11	11	10	9	5
		PM2	23	25	18	14	-	-	-	-
	T32A00OUTC	PA0	18	20	17	13	13	12	11	7
		PM0	25	27	20	16	-	-	-	-

Table 3.4 Signal connection list (4/7)

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
32-bit Timer Event Counter	T32A01INA0	PB1	27	29	22	18	15	14	13	9
		PP1	42	44	32	-	-	-	-	-
	T32A01INA1	PB2	28	30	23	19	16	15	14	-
		PP2	43	45	33	-	-	-	-	-
	T32A01OUTA	PB0	26	28	21	17	14	13	12	8
		PP0	41	43	31	-	-	-	-	-
	T32A01INB0	PB4	30	32	25	21	18	17	16	-
	T32A01INB1	PB5	31	33	-	-	-	-	-	-
	T32A01OUTB	PB3	29	31	24	20	17	16	15	-
	T32A01INC0	PB1	27	29	22	18	15	14	13	9
		PP1	42	44	32	-	-	-	-	-
	T32A01INC1	PB2	28	30	23	19	16	15	14	-
		PP2	43	45	33	-	-	-	-	-
	T32A01OUTC	PB0	26	28	21	17	14	13	12	8
		PP0	41	43	31	-	-	-	-	-

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
32-bit Timer Event Counter	T32A02INA0	PC1	55	57	45	37	32	29	26	19
		PR1	62	64	-	-	-	-	-	-
	T32A02INA1	PC2	56	58	46	38	33	30	27	20
		PR2	63	65	-	-	-	-	-	-
	T32A02OUTA	PC0	54	56	44	36	31	28	25	18
		PR0	61	63	-	-	-	-	-	-
	T32A02INB0	PC4	58	60	48	-	-	-	-	-
	T32A02INB1	PC5	59	61	49	-	-	-	-	-
	T32A02OUTB	PC3	57	59	47	39	34	31	-	-
	T32A02INC0	PC1	55	57	45	37	32	29	26	19
		PR1	62	64	-	-	-	-	-	-
	T32A02INC1	PC2	56	58	46	38	33	30	27	20
		PR2	63	65	-	-	-	-	-	-
	T32A02OUTC	PC0	54	56	44	36	31	28	25	18
		PR0	61	63	-	-	-	-	-	-

Table 3.5 Signal connection list (5/7)

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
32-bit Timer Event Counter	T32A03INA0	PJ1	72	74	57	45	36	33	29	22
	T32A03INA1	PJ2	73	75	58	46	37	34	30	23
	T32A03OUTA	PJ0	71	73	56	44	35	32	28	21
	T32A03INB0	PJ4	75	77	60	48	39	36	32	25
	T32A03INB1	PJ5	76	78	61	49	40	37	33	26
	T32A03OUTB	PJ3	74	76	59	47	38	35	31	24
	T32A03INC0	PJ1	72	74	57	45	36	33	29	22
	T32A03INC1	PJ2	73	75	58	46	37	34	30	23
	T32A03OUTC	PJ0	71	73	56	44	35	32	28	21
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
32-bit Timer Event Counter	T32A04INA0	PK3	80	82	65	53	44	41	37	30
	T32A04INA1	PK4	81	83	66	54	45	42	38	-
	T32A04OUTA	PK2	79	81	64	52	43	40	36	29
	T32A04INB0	PK6	83	85	68	56	-	-	-	-
	T32A04INB1	PK7	84	86	69	-	-	-	-	-
	T32A04OUTB	PK5	82	84	67	55	46	43	39	-
	T32A04INC0	PK3	80	82	65	53	44	41	37	30
	T32A04INC1	PK4	81	83	66	54	45	42	38	-
	T32A04OUTC	PK2	79	81	64	52	43	40	36	29
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
32-bit Timer Event Counter	T32A05INA0	PN1	69	71	54	42	-	-	-	-
	T32A05INA1	PN2	68	70	53	41	-	-	-	-
	T32A05OUTA	PN0	70	72	55	43	-	-	-	-
	T32A05INB0	PN4	66	68	51	-	-	-	-	-
	T32A05INB1	PN5	65	67	-	-	-	-	-	-
	T32A05OUTB	PN3	67	69	52	40	-	-	-	-
	T32A05INC0	PN1	69	71	54	42	-	-	-	-
	T32A05INC1	PN2	68	70	53	41	-	-	-	-
	T32A05OUTC	PN0	70	72	55	43	-	-	-	-

Table 3.6 Signal connection list (6/7)

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
12-bit Analog to Digital Convertor	AINA00	PD0	4	6	3	3	3	3	3	2
	AINA01	PD1	3	5	2	2	2	2	2	1
	AINA02	PD2	2	4	1	1	1	1	1	-
	AINA03	PD3	1	3	-	-	-	-	-	-
	AINA04	PE0	100	2	80	64	52	48	44	32
	AINA05	PE1	99	1	79	63	51	47	43	31
	AINA06	PE2	98	100	78	62	50	46	42	-
	AINA07	PE3	97	99	77	61	49	45	41	-
	AINA08	PE4	96	98	76	60	48	44	40	-
	AINA09	PE5	95	97	75	-	-	-	-	-
	AINA10	PE6	94	96	74	-	-	-	-	-
	AINA11	PF0	93	95	-	-	-	-	-	-
	AINA12	PF1	92	94	-	-	-	-	-	-
	AINA13	PF2	91	93	-	-	-	-	-	-
	AINA14	PF3	90	92	-	-	-	-	-	-
	AINA15	PF4	89	91	-	-	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
8-bit Digital to Analog Convertor	DAC0	PG0	7	9	6	6	6	6	-	-
	DAC1	PG1	8	10	7	-	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Exception	INT00	PC0	54	56	44	36	31	28	25	18
	INT01	PC1	55	57	45	37	32	29	26	19
	INT02	PC2	56	58	46	38	33	30	27	20
	INT03	PB1	27	29	22	18	15	14	13	9
	INT04	PJ4	75	77	60	48	39	36	32	25
	INT05	PK1	78	80	63	51	42	39	35	28
	INT06	PH3	52	54	42	34	29	26	-	-
	INT07	PA6	12	14	11	7	7	-	-	-
	INT08	PL3	37	39	29	25	-	-	-	-
	INT09	PM2	23	25	18	14	-	-	-	-
	INT10	PN3	67	69	52	40	-	-	-	-
	INT11	PA7	11	13	10	-	-	-	-	-
	INT12	PL4	38	40	30	-	-	-	-	-
	INT13	PK7	84	86	69	-	-	-	-	-
	INT14	PP3	85	87	70	-	-	-	-	-
	INT15	PM6	19	21	-	-	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Programmable Motor Control Circuit Plus	EMG0_N	PK0	77	79	62	50	41	38	34	27
	OVV0_N	PK1	78	80	63	51	42	39	35	28
	UO0	PJ0	71	73	56	44	35	32	28	21
	VO0	PJ2	73	75	58	46	37	34	30	23
	WO0	PJ4	75	77	60	48	39	36	32	25
	XO0	PJ1	72	74	57	45	36	33	29	22
	YO0	PJ3	74	76	59	47	38	35	31	24
	ZO0	PJ5	76	78	61	49	40	37	33	26

Table 3.7 Signal connection list (7/7)

Related Reference Manual	Function pin name	Port name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
Advanced Encoder Input Circuit	ENC0A	PA0	18	20	17	13	13	12	11	7
	ENC0B	PA1	17	19	16	12	12	11	10	6
	ENC0Z	PA2	16	18	15	11	11	10	9	5
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Product Information (Trigger Selector)	TRGIN0	PB1	27	29	22	18	15	14	13	9
	TRGIN1	PA3	15	17	14	10	10	9	8	-
	TRGIN2	PN3	67	69	52	40	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Remote Control Signal Preprocessor	RXIN0	PB1	27	29	22	18	15	14	13	9
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Real Time Clock	RTCOUT	PC2	56	58	46	38	33	30	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Boundary Scan(Note)	TMS	PK2	79	81	64	52	43	-	-	-
	TCK	PK3	80	82	65	53	44	-	-	-
	TDO	PK4	81	83	66	54	45	-	-	-
	TDI	PK5	82	84	67	55	46	-	-	-
	TRST_N	PK6	83	85	68	56	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Debug Interface	TMS	PK2	79	81	64	52	43	40	36	-
	TCK	PK3	80	82	65	53	44	41	37	-
	TDO	PK4	81	83	66	54	45	42	38	-
	TDI	PK5	82	84	67	55	46	43	39	-
	TRST_N	PK6	83	85	68	56	-	-	-	-
	SWDIO	PK2	79	81	64	52	43	40	36	29
	SWCLK	PK3	80	82	65	53	44	41	37	30
	SWV	PK4	81	83	66	54	45	42	38	-
	TRACECLK	PM0	25	27	20	16	-	-	-	-
	TRACEDATA0	PM1	24	26	19	15	-	-	-	-
	TRACEDATA1	PM2	23	25	18	14	-	-	-	-
	TRACEDATA2	PM3	22	24	-	-	-	-	-	-
	TRACEDATA3	PM4	21	23	-	-	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
Clock Generator and Operation Mode	SCOUT	PB0	26	28	21	17	14	13	12	8
	X1	PH0	48	50	38	30	25	22	21	14
	X2	PH1	49	51	39	31	26	23	22	15
	XT1	PH2	51	53	41	33	28	25	-	-
	XT2	PH3	52	54	42	34	29	26	-	-
	EHCLKIN	PH0	48	50	38	30	25	22	21	14
Related Reference Manual	**Function pin name**	**Port name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
FLASH Memory	BOOT_N	PB0	26	28	21	17	14	13	12	8

Note: When use boundary Scan, BSC pin should be done to “High” and start a power supply again.

4. Registers

The following registers should be set appropriately to use the ports.

Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

"x" and "n" in the following table show a port name and a function number, respectively.

Register Name		Type	Setting Value	Description
[PxDATA]	Data Register	R/W	0 or 1	Read from and write to a port.
[PxCR]	Output Control Register	R/W	0: Output disabled 1: Output enabled	Output control.
[PxFRn]	Function Register n	R/W	0: PORT 1: Function	Function setting. When 1 is set, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled.
[PxOD]	Open-Drain Control Register	R/W	0: CMOS 1: Open-drain	Programmable open-drain control. The programmable open-drain is a pseudo open-drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** = 1.
[PxPUP]	Pull-up Control Register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up control.
[PxPDN]	Pull-down Control Register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down control.
[PxIE]	Input Control Register	R/W	0: Input disabled 1: Input enabled	It takes 100ns(Max) that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled.

4.1. List of Register

When the bit which is assigned to no functions is read, 0 is returned. The write to the bit is ignored.

Table 4.1 Ports base address

Peripheral function		Channel/Unit	Base address
Input/output ports	PA	-	0x400C0000
	PB	-	0x400C0100
	PC	-	0x400C0200
	PD	-	0x400C0300
	PE	-	0x400C0400
	PF	-	0x400C0500
	PG	-	0x400C0600
	PH	-	0x400C0700
	PJ	-	0x400C0800
	PK	-	0x400C0900
	PL	-	0x400C0A00
	PM	-	0x400C0B00
	PN	-	0x400C0C00
	PP	-	0x400C0D00
	PR	-	0x400C0E00

Table 4.2 Register List

Register Name	Address (Base+)	Port A	Port B	Port C	Port D	Port E
Data Register	0x0000	*[PADATA]*	*[PBDATA]*	*[PCDATA]*	*[PDDATA]*	*[PEDATA]*
Output Control Register	0x0004	*[PACR]*	*[PBCR]*	*[PCCR]*	*[PDCR]*	*[PECR]*
Function Register 1	0x0008	*[PAFR1]*	*[PBFR1]*	*[PCFR1]*	-	-
Function Register 2	0x000C	*[PAFR2]*	*[PBFR2]*	-	-	-
Function Register 3	0x0010	*[PAFR3]*	*[PBFR3]*	*[PCFR3]*	-	-
Function Register 4	0x0014	*[PAFR4]*	*[PBFR4]*	*[PCFR4]*	-	-
Function Register 5	0x0018	*[PAFR5]*	*[PBFR5]*	*[PCFR5]*	-	-
Function Register 6	0x001C	*[PAFR6]*	*[PBFR6]*	-	-	-
Open-Drain Control Register	0x0028	*[PAOD]*	*[PBOD]*	*[PCOD]*	*[PDOD]*	*[PEOD]*
Pull-up Control Register	0x002C	*[PAPUP]*	*[PBPUP]*	*[PCPUP]*	*[PDPUP]*	*[PEPUP]*
Pull-down Control Register	0x0030	*[PAPDN]*	*[PBPDN]*	*[PCPDN]*	*[PDPDN]*	*[PEPDN]*
Input Control Register	0x0038	*[PAIE]*	*[PBIE]*	*[PCIE]*	*[PDIE]*	*[PEIE]*

Note: Do not access the addresses described as "-"

Register Name	Address (Base+)	Port F	Port G	Port H	Port J	Port K
Data Register	0x0000	*[PFDATA]*	*[PGDATA]*	*[PHDATA]*	*[PJDATA]*	*[PKDATA]*
Output Control Register	0x0004	*[PFCR]*	*[PGCR]*	-	*[PJCR]*	*[PKCR]*
Function Register 1	0x0008	-	-	-	*[PJFR1]*	*[PKFR1]*
Function Register 2	0x000C	-	-	-	*[PJFR2]*	*[PKFR2]*
Function Register 3	0x0010	-	-	-	*[PJFR3]*	*[PKFR3]*
Function Register 4	0x0014	-	-	-	*[PJFR4]*	*[PKFR4]*
Function Register 5	0x0018	-	-	-	*[PJFR5]*	*[PKFR5]*
Open-Drain Control Register	0x0028	*[PFOD]*	*[PGOD]*	-	*[PJOD]*	*[PKOD]*
Pull-up Control Register	0x002C	*[PFPUP]*	*[PGPUP]*	-	*[PJPUP]*	*[PKPUP]*
Pull-down Control Register	0x0030	*[PFPDN]*	*[PGPDN]*	*[PHPDN]*	*[PJPDN]*	*[PKPDN]*
Input Control Register	0x0038	*[PFIE]*	*[PGIE]*	*[PHIE]*	*[PJIE]*	*[PKIE]*

Note: Do not access the addresses described as "-"

Register Name	Address (Base+)	Port L	Port M	Port N	Port P	Port R
Data Register	0x0000	*[PLDATA]*	*[PMDATA]*	*[PNDATA]*	*[PPDATA]*	*[PRDATA]*
Output Control Register	0x0004	*[PLCR]*	*[PMCR]*	*[PNCR]*	*[PPCR]*	*[PRCR]*
Function Register 1	0x0008	*[PLFR1]*	*[PMFR1]*	-	*[PPFR1]*	-
Function Register 2	0x000C	*[PLFR2]*	*[PMFR2]*	-	-	-
Function Register 3	0x0010	*[PLFR3]*	*[PMFR3]*	*[PNFR3]*	*[PPFR3]*	*[PRFR3]*
Function Register 4	0x0014	-	*[PMFR4]*	*[PNFR4]*	*[PPFR4]*	*[PRFR4]*
Function Register 5	0x0018	-	*[PMFR5]*	*[PNFR5]*	-	-
Function Register 6	0x001C	-	*[PMFR6]*	-	-	-
Open-Drain Control Register	0x0028	*[PLOD]*	*[PMOD]*	*[PNOD]*	*[PPOD]*	*[PROD]*
Pull-up Control Register	0x002C	*[PLPUP]*	*[PMPUP]*	*[PNPUP]*	*[PPPUP]*	*[PRPUP]*
Pull-down Control Register	0x0030	*[PLPDN]*	*[PMPDN]*	*[PNPDN]*	*[PPPDN]*	*[PRPDN]*
Input Control Register	0x0038	*[PLIE]*	*[PMIE]*	*[PNIE]*	*[PPIE]*	*[PRIE]*

Note: Do not access the addresses described as "-"

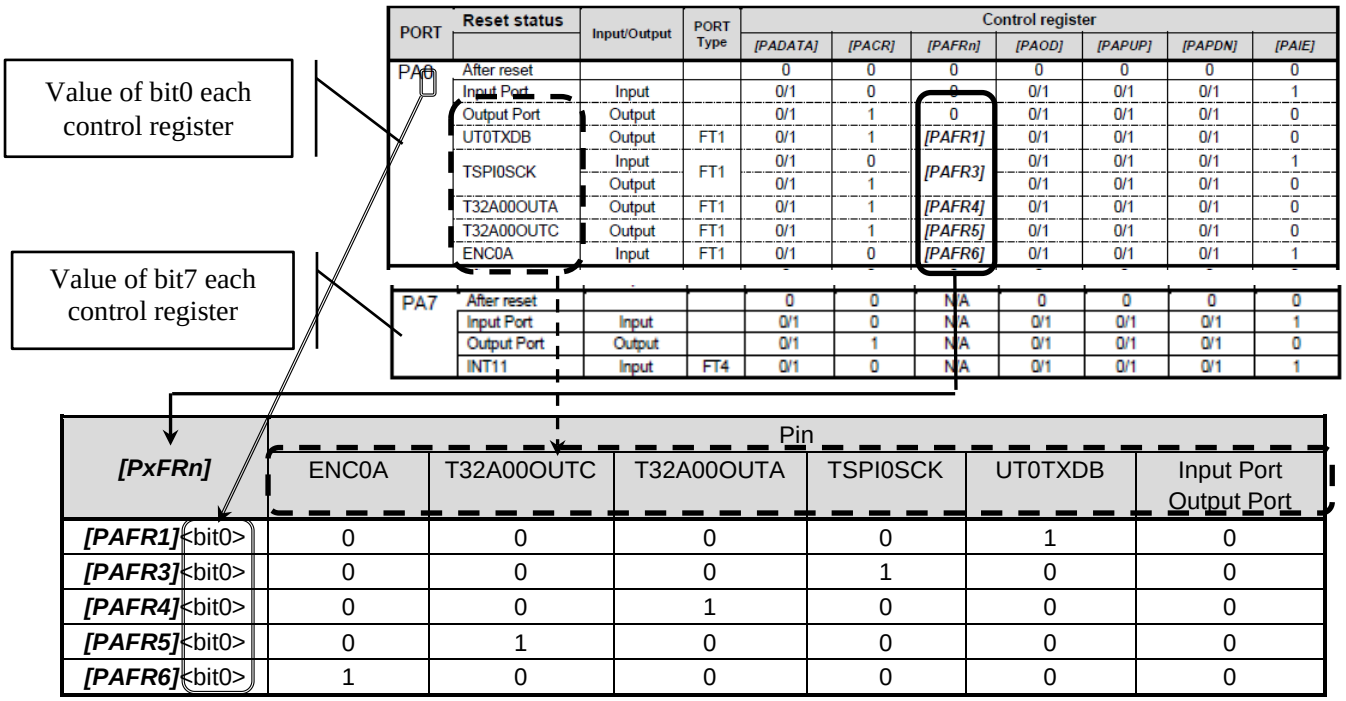
4.2. List of Port Functions and Settings

It is explained about viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the N/A in the tables returns 0 when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.



PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	[PACR]	[PAFRn]	[PAOD]	[PAPUP]	[PAPDN]	[PAIE]
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDB	Output	FT1	0/1	1	[PAFR1]	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1	0/1	0	[PAFR3]	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	[PAFR4]	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	[PAFR5]	0/1	0/1	0/1	0
	ENC0A	Input	FT1	0/1	0	[PAFR6]	0/1	0/1	0/1	1
PA7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT11	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1

[PxFRn]	Pin					
	ENC0A	T32A00OUTC	T32A00OUTA	TSPI0SCK	UT0TXDB	Input Port Output Port
[PAFR1]<bit0>	0	0	0	0	1	0
[PAFR3]<bit0>	0	0	0	1	0	0
[PAFR4]<bit0>	0	0	1	0	0	0
[PAFR5]<bit0>	0	1	0	0	0	0
[PAFR6]<bit0>	1	0	0	0	0	0

4.2.1. Setting of using the function pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and enable output control register (***[PxCR]***<bit m>=1), then set the peripheral functions. If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), then set the peripheral functions.

To use peripheral functions such as I^2C, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), then set the peripheral function.

- When multiple functions are assigned same pin, please choose only one function for usage.
- When same function are assigned multiple pins, please the function use exclusively.

4.2.2. PORT A

Table 4.3 Port A registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDB	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
	ENC0A	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FT2	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A00INA0	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	ENC0B	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A00INA1	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A00INC1	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	ENC0Z	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI0CS0	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A00OUTB	Output	FT1	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	TRGIN1	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C1SCL	I/O	FT1	0/1	1	***[PAFR1]***	1	0/1	0/1	1
	TSPI0CS1	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A00INB0	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C1SDA	I/O	FT1	0/1	1	***[PAFR1]***	1	0/1	0/1	1
	T32A00INB1	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT07	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1
PA7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT11	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1

4.2.3. PORT B

Table 4.4 Port B registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBPUP]*	*[PBPDN]*	*[PBIE]*
PB0	During reset (BOOT_N)	Input	FT6	0	0	0	0	1 (Note)	0	N/A
	After reset			0	0	0	0	0	0	N/A
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	N/A
	T32A01OUTA	Output	FT1	0/1	1	***[PBFR4]***	0/1	0/1	0/1	N/A
	T32A01OUTC	Output	FT1	0/1	1	***[PBFR5]***	0/1	0/1	0/1	N/A
	SCOUT	Output	FT1	0/1	1	***[PBFR6]***	0/1	0/1	0/1	N/A
PB1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	RXIN0	Input	FT1	0/1	0	***[PBFR1]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
	TRGIN0	Input	FT1	0/1	0	***[PBFR6]***	0/1	0/1	0/1	1
PB2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	TSPI1SCK	Input	FT1	0/1	0	***[PBFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A01INA1	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
PB3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PBFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1	0/1	1	***[PBFR2]***	0/1	0/1	0/1	0
	TSPI1TXD	Output	FT2	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	T32A01OUTB	Output	FT1	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PBFR1]***	0/1	0/1	0/1	1
	UT2RTS_N	Output	FT1	0/1	1	***[PBFR2]***	0/1	0/1	0/1	0
	TSPI1RXD	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	T32A01INB0	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
PB5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2RTS_N	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	TSPI1CS0	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	T32A01INB1	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	TSPI1CSIN	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1

PB6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS1	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
PB7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0

Note: ***[PBPUP]*** is enable during reset by the reset pin(RESET_N). ***[PBIE]*** is assigned as "N/A", but BOOT_N signal can be input.

4.2.4. PORT C

Table 4.5 Port C registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PCDATA]	***[PCCR]***	***[PCFRn]***	***[PCOD]***	***[PCPUP]***	***[PCPDN]***	***[PCIE]***
PC0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	I2C0SCL	I/O	FT12	0/1	1	***[PCFR1]***	1	0/1	0/1	1
	T32A02OUTA	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1	0/1	1	***[PCFR4]***	0/1	0/1	0/1	0
PC1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	I2C0SDA	I/O	FT12	0/1	1	***[PCFR1]***	1	0/1	0/1	1
	T32A02INA0	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FT1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
PC2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A02INA1	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FT1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
	RTCOUT	Output	FT1	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
PC3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02OUTB	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
PC4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02INB0	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
PC5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02INB1	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
PC6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0

4.2.5. PORT D

Table 4.6 Port D registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA00	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA01	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA02	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA03	Input	FT5	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINAx), ***[PDCR]*** should be output disable "0", ***[PDIE]*** should be input disable"0" , ***[PDPUP]*** should be pull-up disable "0" and ***[PDPDN]*** should be pull-down disable "0".

4.2.6. PORT E

Table 4.7 Port E registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA04	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA05	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA06	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA07	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA08	Input	FT5	0/1	0	N/A	0/1	0	0	0

PE5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA09	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA10	Input	FT5	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINAx), ***[PECR]*** should be output disable "0", ***[PEIE]*** should be input disable "0" , ***[PEPUP]*** should be pull-up disable "0" and ***[PEPDN]*** should be pull-down disable "0".

4.2.7. PORT F

Table 4.8 Port F registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA11	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA12	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA13	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA14	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA15	Input	FT5	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINAx), ***[PFCR]*** should be output disable "0", ***[PFIE]*** should be input disable "0" , ***[PFPUP]*** should be pull-up disable "0" and ***[PFPDN]*** should be pull-down disable "0".

4.2.8. PORT G

Table 4.9 Port G registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	DAC0	Output	FT13	0/1	0	N/A	0/1	0	0	0
PG1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	DAC1	Output	FT13	0/1	0	N/A	0/1	0	0	0

Note: When using analog output(DACx), ***[PGCR]*** should be output disable "0", ***[PGIE]*** should be input disable "0" , ***[PGPUP]*** should be pull-up disable "0" and ***[PGPDN]*** should be pull-down disable "0".

4.2.9. PORT H

Table 4.10 Port H registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PHDATA]	*[PHCR]*	*[PHFRn]*	*[PHOD]*	*[PHPUP]*	*[PHPDN]*	*[PHIE]*
PH0	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X1	Input	FT11	0/1	N/A	N/A	N/A	N/A	0	0
	EHCLKIN	Input	FT11	0/1	N/A	N/A	N/A	N/A	0	1
PH1	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X2	Output	FT11	0/1	N/A	N/A	N/A	N/A	0	0
PH2	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	XT1	Input	FT11	0/1	N/A	N/A	N/A	N/A	0	0
PH3	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	XT2	Output	FT11	0/1	N/A	N/A	N/A	N/A	0	0
	INT06	Input	FT11	0/1	N/A	N/A	N/A	N/A	0/1	1

4.2.10. PORT J

Table 4.11 Port J registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PJDATA]	*[PJCR]*	*[PJFRn]*	*[PJOD]*	*[PJPUP]*	*[PJPDN]*	*[PJIE]*
PJ0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1TXDB	Output	FT1	0/1	1	***[PJFR1]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FT1	0/1	1	***[PJFR3]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FT1	0/1	1	***[PJFR4]***	0/1	0/1	0/1	0
	UO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1TXDA	Output	FT1	0/1	1	***[PJFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PJFR2]***	0/1	0/1	0/1	1
	T32A03INA0	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FT1	0/1	0	***[PJFR4]***	0/1	0/1	0/1	1
	XO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PJFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PJFR2]***	0/1	0/1	0/1	0
	T32A03INA1	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FT1	0/1	0	***[PJFR4]***	0/1	0/1	0/1	1
	VO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PJFR1]***	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PJFR2]***	0/1	0/1	0/1	0
	T32A03OUTB	Output	FT1	0/1	1	***[PJFR3]***	0/1	0/1	0/1	0
	YO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT04	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PJFR1]***	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PJFR2]***	0/1	0/1	0/1	1
	T32A03INB0	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	WO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ5	After reset	Input		0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03INB1	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	ZO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0

4.2.11. PORT K

Table 4.12 Port K registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PKDATA]	*[PKCR]*	*[PKFRn]*	*[PKOD]*	*[PKPUP]*	*[PKPDN]*	*[PKIE]*
PK0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1TXDB	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	EMG0_N	Input	FT1	0/1	0	***[PKFR5]***	0/1	0/1	0/1	1
PK1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	OVV0_N	Input	FT1	0/1	0	***[PKFR5]***	0/1	0/1	0/1	1
PK2	After reset (TMS/SWDIO)	I/O	FT2	0	1(Note)	***[PKFR5]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	T32A04OUTA	Output	FT1	0/1	1	***[PKFR3]***	0/1	0/1	0/1	0
	T32A04OUTC	Output	FT1	0/1	1	***[PKFR4]***	0/1	0/1	0/1	0
PK3	After reset (TCK/SWCLK)	Input	FT1	0	0	***[PKFR5]***	0	0	1	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	T32A04INA0	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	T32A04INC0	Input	FT1	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
PK4	After reset (TDO/SWV)	Output	FT2	0	1(Note)	***[PKFR5]***	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1RTS_N	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A04INA1	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	T32A04INC1	Input	FT1	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
PK5	After reset (TDI)	Input	FT1	0	0	***[PKFR5]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04OUTB	Output	FT1	0/1	1	***[PKFR3]***	0/1	0/1	0/1	0
PK6	After reset (TRST_N)	Input	FT3	0	0	***[PKFR5]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04INB0	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
PK7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT13	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A04INB1	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1

Note: When receive the command from TOOL, it becomes output.

4.2.12. PORT L

Table 4.13 Port L registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PLDATA]	*[PLCR]*	*[PLFRn]*	*[PLOD]*	*[PLPUP]*	*[PLPDN]*	*[PLIE]*
PL0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FT1	0/1	1	***[PLFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PLFR2]***	0/1	0/1	0/1	1
	I2C2SCL	I/O	FT1	0/1	1	***[PLFR3]***	1	0/1	0/1	1
PL1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PLFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0
	I2C2SDA	I/O	FT1	0/1	1	***[PLFR3]***	1	0/1	0/1	1
PL2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PLFR1]***	0/1	0/1	0/1	1
	UT2RTS_N	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0
PL3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT08	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT2RTS_N	Output	FT1	0/1	1	***[PLFR1]***	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PLFR2]***	0/1	0/1	0/1	1
PL4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT12	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1
PL5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS1	Output	FT1	0/1	1	***[PLFR1]***	0/1	0/1	0/1	0
PL6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS0	Output	FT1	0/1	1	***[PLFR1]***	0/1	0/1	0/1	0
	TSPI1CSIN	Input	FT1	0/1	0	***[PLFR2]***	0/1	0/1	0/1	1

4.2.13. PORT M

Table 4.14 Port M registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PMDATA]	*[PMCR]*	*[PMFRn]*	*[PMOD]*	*[PMPUP]*	*[PMPDN]*	*[PMIE]*
PM0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDB	Output	FT1	0/1	1	***[PMFR1]***	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1	0/1	0	***[PMFR3]***	0/1	0/1	0/1	1
		Output	FT1	0/1	1		0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	***[PMFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	***[PMFR5]***	0/1	0/1	0/1	0
	TRACECLK	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FT1	0/1	1	***[PMFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PMFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FT2	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	T32A00INA0	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TRACEDATA0	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT09	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FT1	0/1	0	***[PMFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FT1	0/1	0	***[PMFR3]***	0/1	0/1	0/1	1
	T32A00INA1	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	T32A00INC1	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TRACEDATA1	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1	0/1	0	***[PMFR1]***	0/1	0/1	0/1	1
	UT0RTS_N	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	TSPI0CS0	Output	FT1	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	T32A00OUTB	Output	FT1	0/1	1	***[PMFR4]***	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TRACEDATA2	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RTS_N	Output	FT1	0/1	1	***[PMFR1]***	0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1	0/1	0	***[PMFR2]***	0/1	0/1	0/1	1
	TSPI0CS1	Output	FT1	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	T32A00INB0	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	TRACEDATA3	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A00INB1	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
PM6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT15	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1

4.2.14. PORT N

Table 4.15 Port N registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PNDATA]	*[PNCR]*	*[PNFRn]*	*[PNOD]*	*[PNPUP]*	*[PNPDN]*	*[PNIE]*
PN0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05OUTA	Output	FT1	0/1	1	***[PNFR3]***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FT1	0/1	1	***[PNFR4]***	0/1	0/1	0/1	0
PN1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05INA0	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1
	T32A05INC0	Input	FT1	0/1	0	***[PNFR4]***	0/1	0/1	0/1	1
PN2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05INA1	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1
	T32A05INC1	Input	FT1	0/1	0	***[PNFR4]***	0/1	0/1	0/1	1
PN3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT10	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A05OUTB	Output	FT1	0/1	1	***[PNFR3]***	0/1	0/1	0/1	0
	TRGIN2	Input	FT1	0/1	0	***[PNFR5]***	0/1	0/1	0/1	1
PN4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05INB0	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1
PN5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05INB1	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1

4.2.15. PORT P

Table 4.16 Port P registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PPDATA]	*[PPCR]*	*[PPFRn]*	*[PPOD]*	*[PPPUP]*	*[PPPDN]*	*[PPIE]*
PP0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1SCK	Input	FT1	0/1	0	***[PPFR1]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A01OUTA	Output	FT1	0/1	1	***[PPFR3]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FT1	0/1	1	***[PPFR4]***	0/1	0/1	0/1	0
PP1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1TXD	Output	FT2	0/1	1	***[PPFR1]***	0/1	0/1	0/1	0
	T32A01INA0	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FT1	0/1	0	***[PPFR4]***	0/1	0/1	0/1	1
PP2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1RXD	Input	FT1	0/1	0	***[PPFR1]***	0/1	0/1	0/1	1
	T32A01INA1	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1	0/1	0	***[PPFR4]***	0/1	0/1	0/1	1
PP3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT14	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1

4.2.16. PORT R

Table 4.17 Port R registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PRDATA]	*[PRCR]*	*[PRFRn]*	*[PROD]*	*[PRPUP]*	*[PRPDN]*	*[PRIE]*
PR0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02OUTA	Output	FT1	0/1	1	***[PRFR3]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1	0/1	1	***[PRFR4]***	0/1	0/1	0/1	0
PR1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02INA0	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FT1	0/1	0	***[PRFR4]***	0/1	0/1	0/1	1
PR2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02INA1	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FT1	0/1	0	***[PRFR4]***	0/1	0/1	0/1	1
PR3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0

5. Block Diagrams of Ports

The port has nine types of circuits, FT1 to FT6,FT11 to FT13. Each circuit diagram is shown in the following page and after. The dot line block shows an equivalent circuit which is described in "Datasheet".

The "IO Reset" shown in the circuit diagram is described the power on reset(POR) or the reset pin(RESET_N). Although, “I/O Reset” of debug pins(TMS/SWDIO.TDI,TDO/SWV,TCK/SWCLK,TRST_N) is the power on reset(POR) only.

5.1. Type FT1

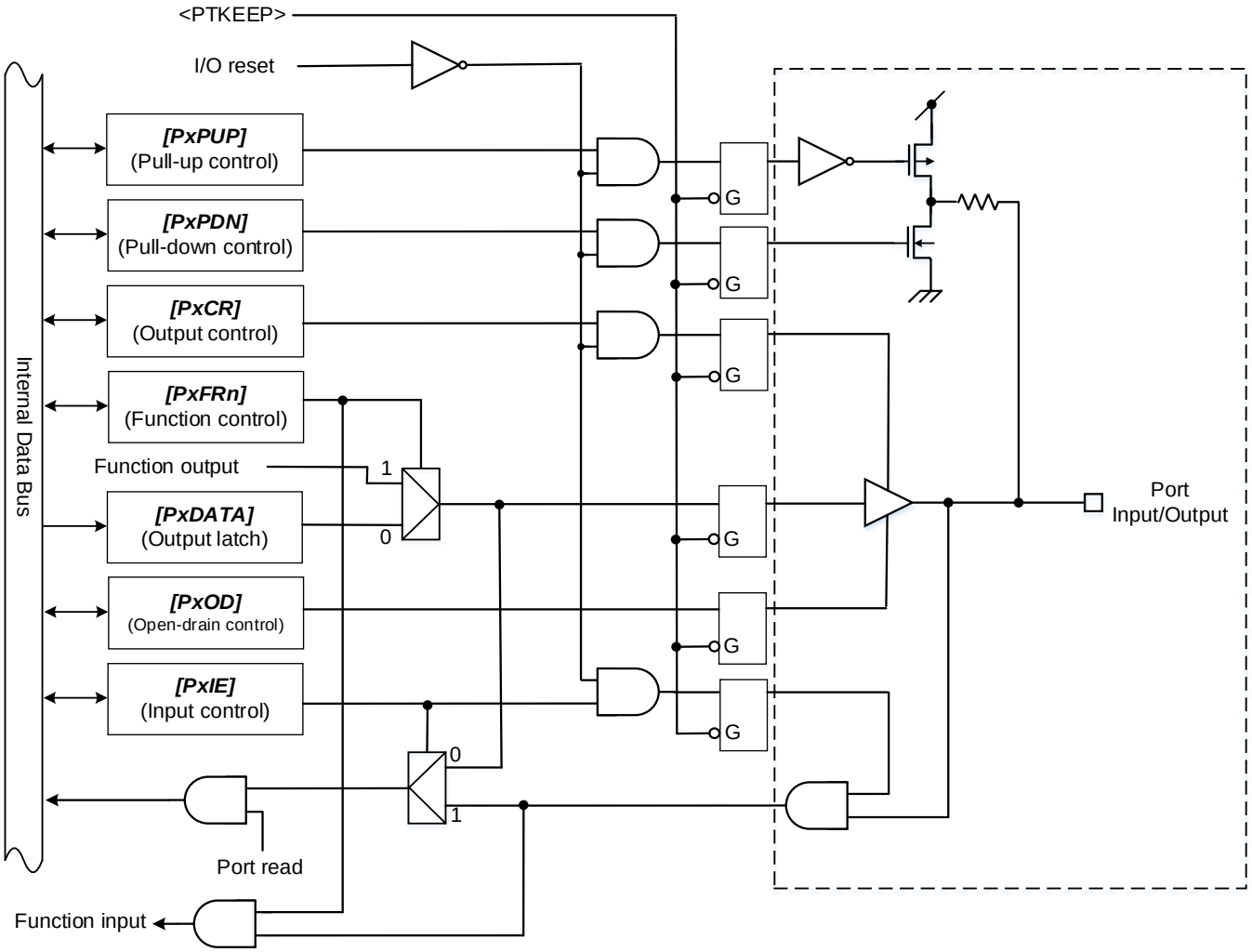


Figure 5.1 Port Type FT1

Note: ***[PxIE]*** is not available PB0 pin.

5.2. Type FT2

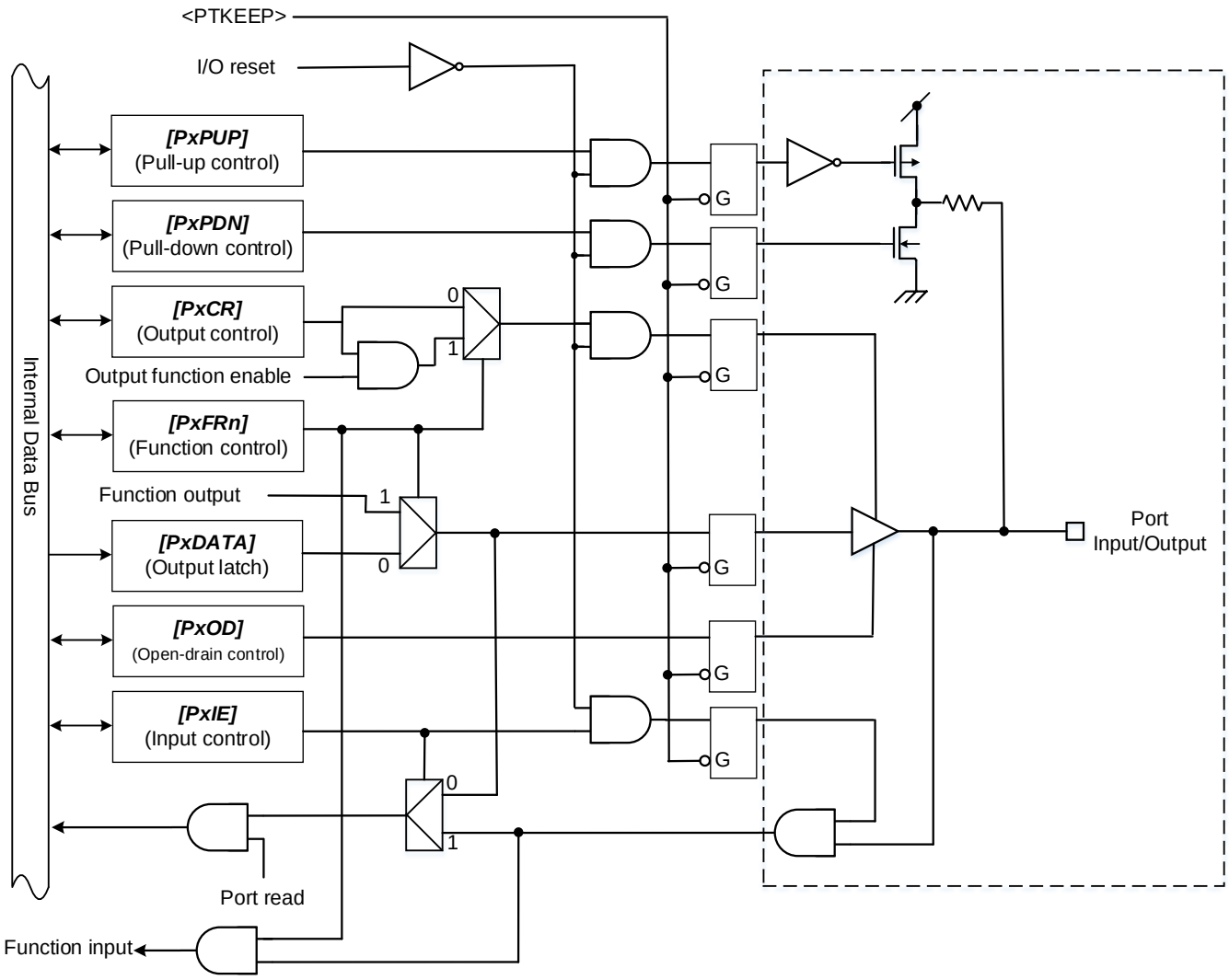


Figure 5.2 Port Type FT2

5.3. Type FT3

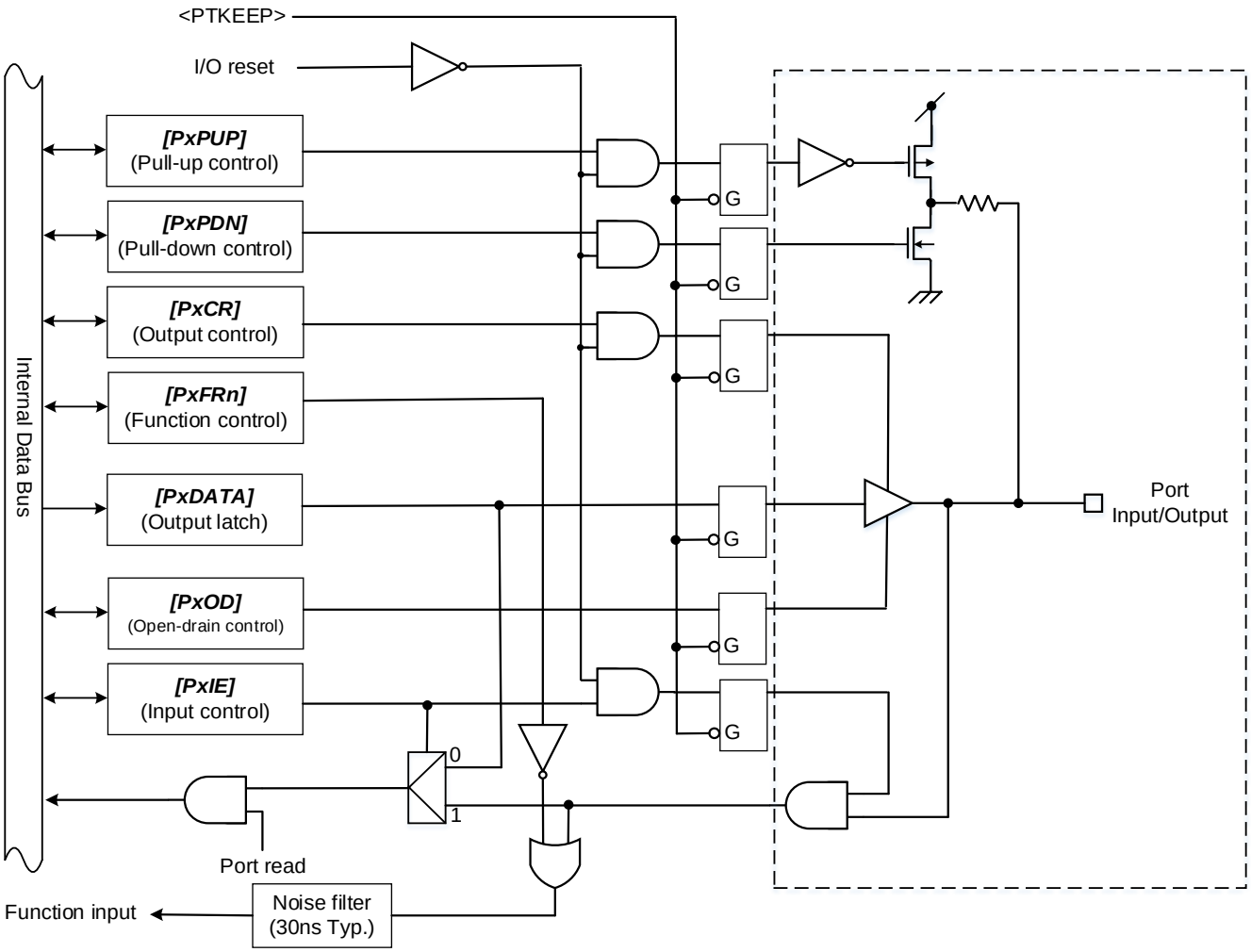


Figure 5.3 Port Type FT3

5.4. Type FT4

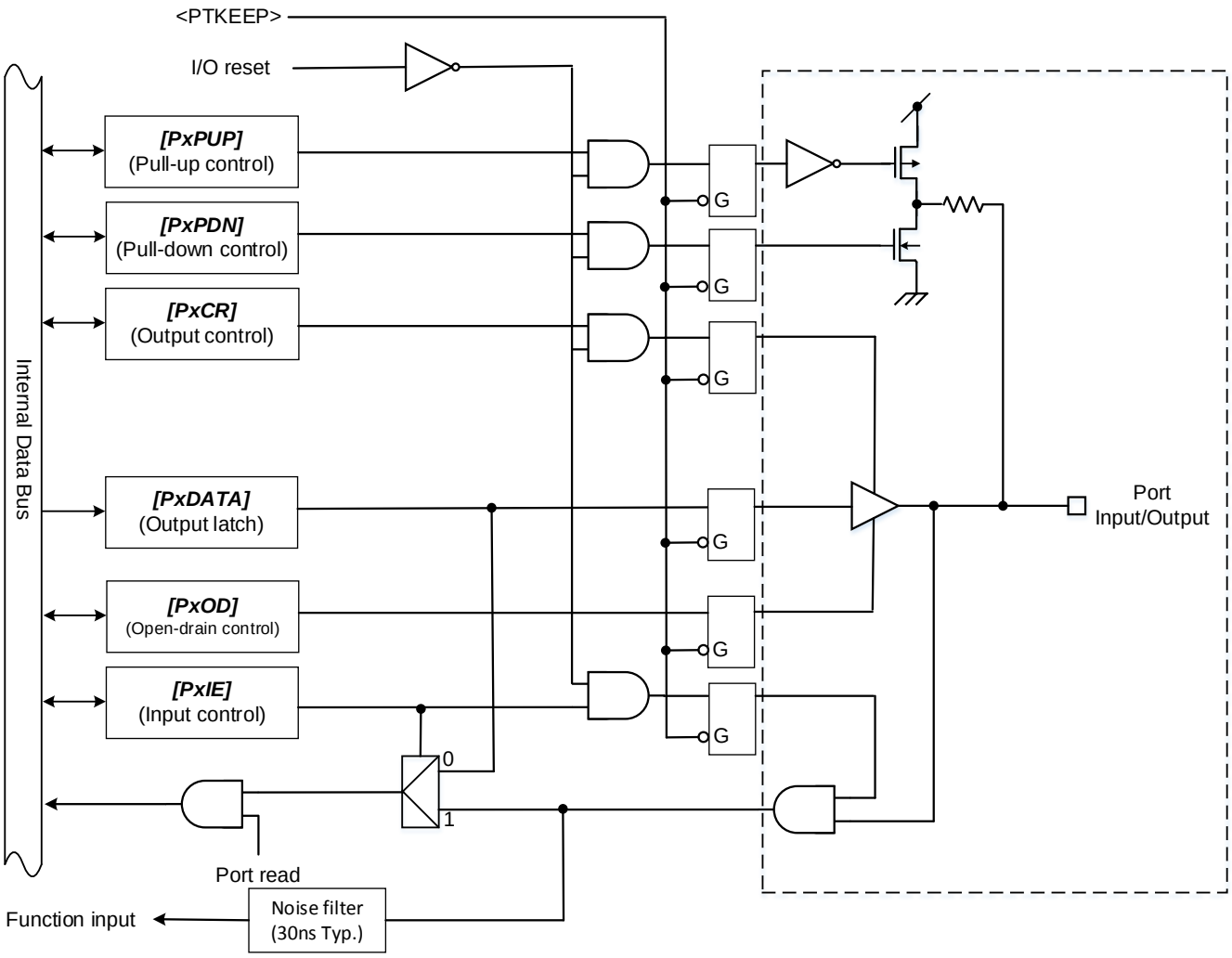


Figure 5.4 Port Type FT4

5.5. Type FT5

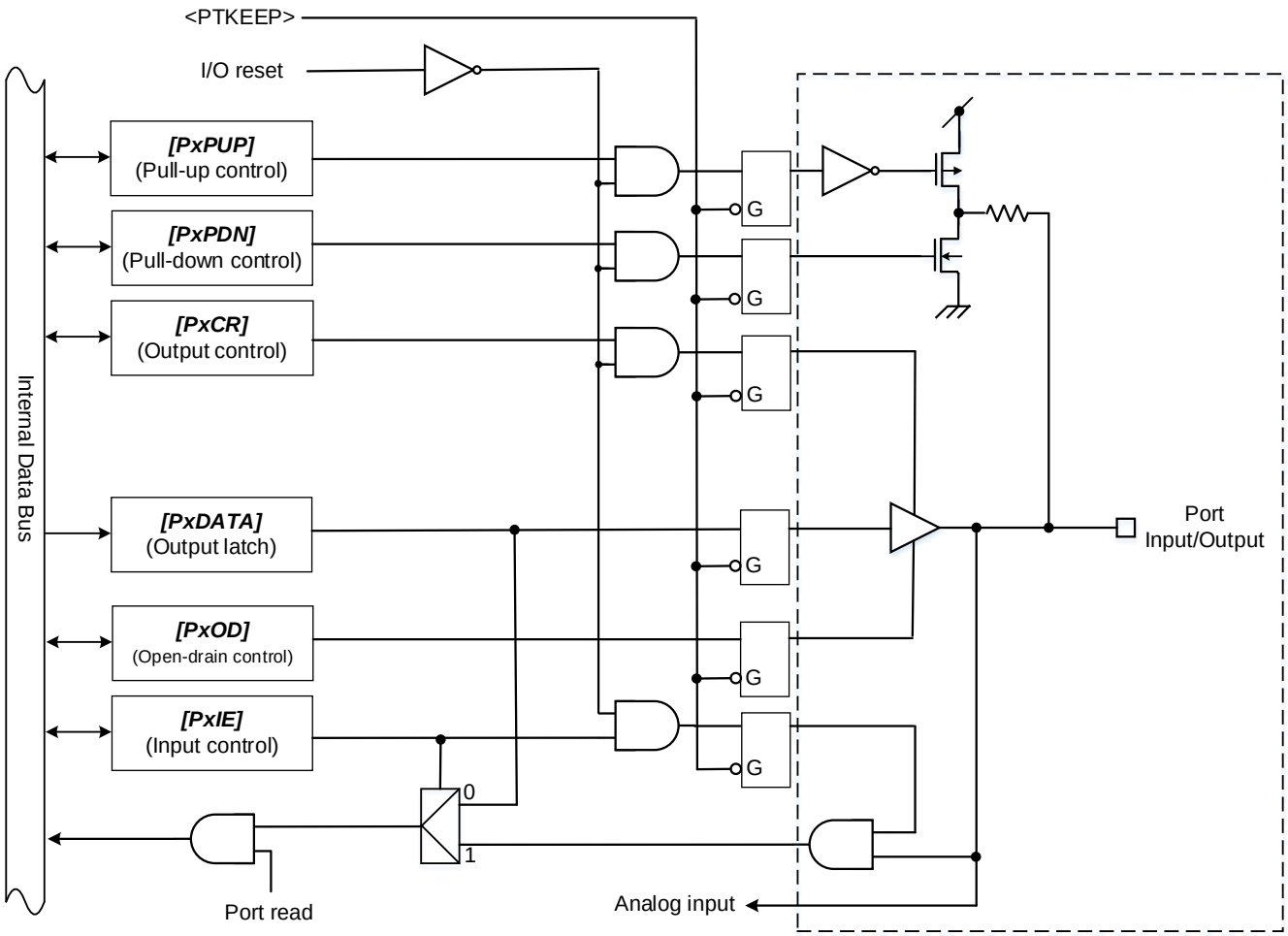


Figure 5.5 Port Type FT5

5.6. Type FT6

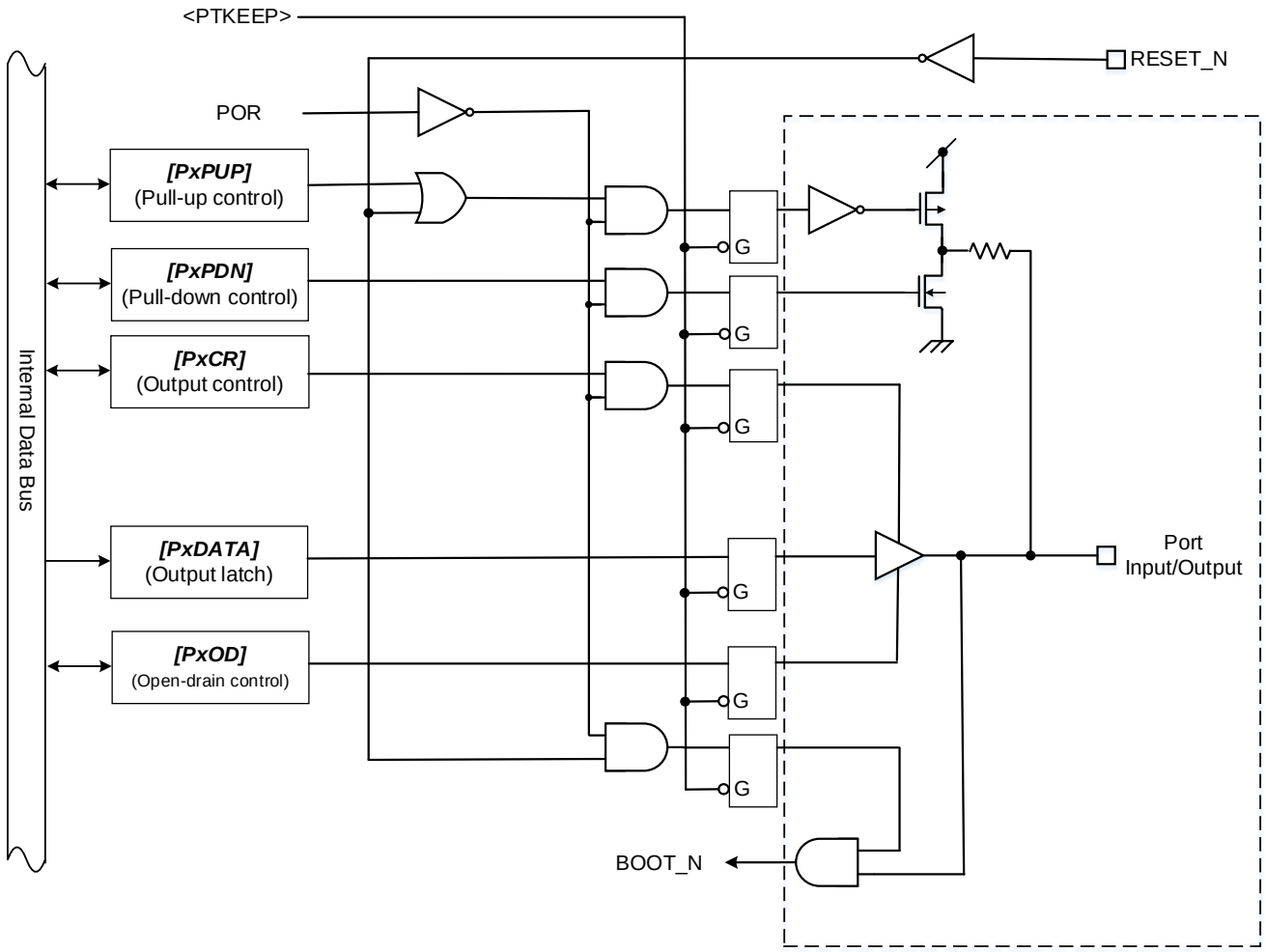


Figure 5.6 Port Type FT6

5.7. Type FT11

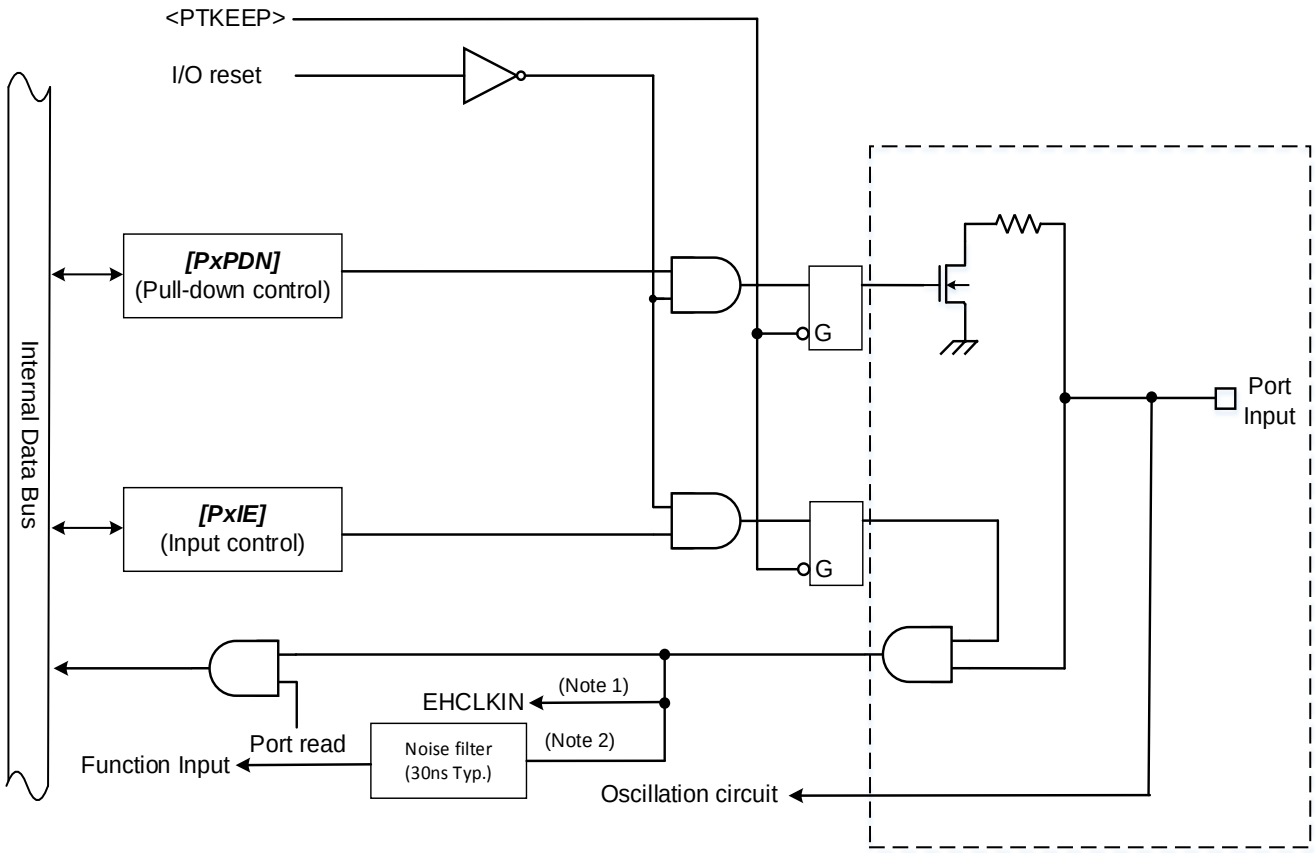


Figure 5.7 Port Type FT11

Note 1: PH0/X1/EHCLKIN pin

Note 2: PH3/XT2/INT06 pin

5.8. Type FT12

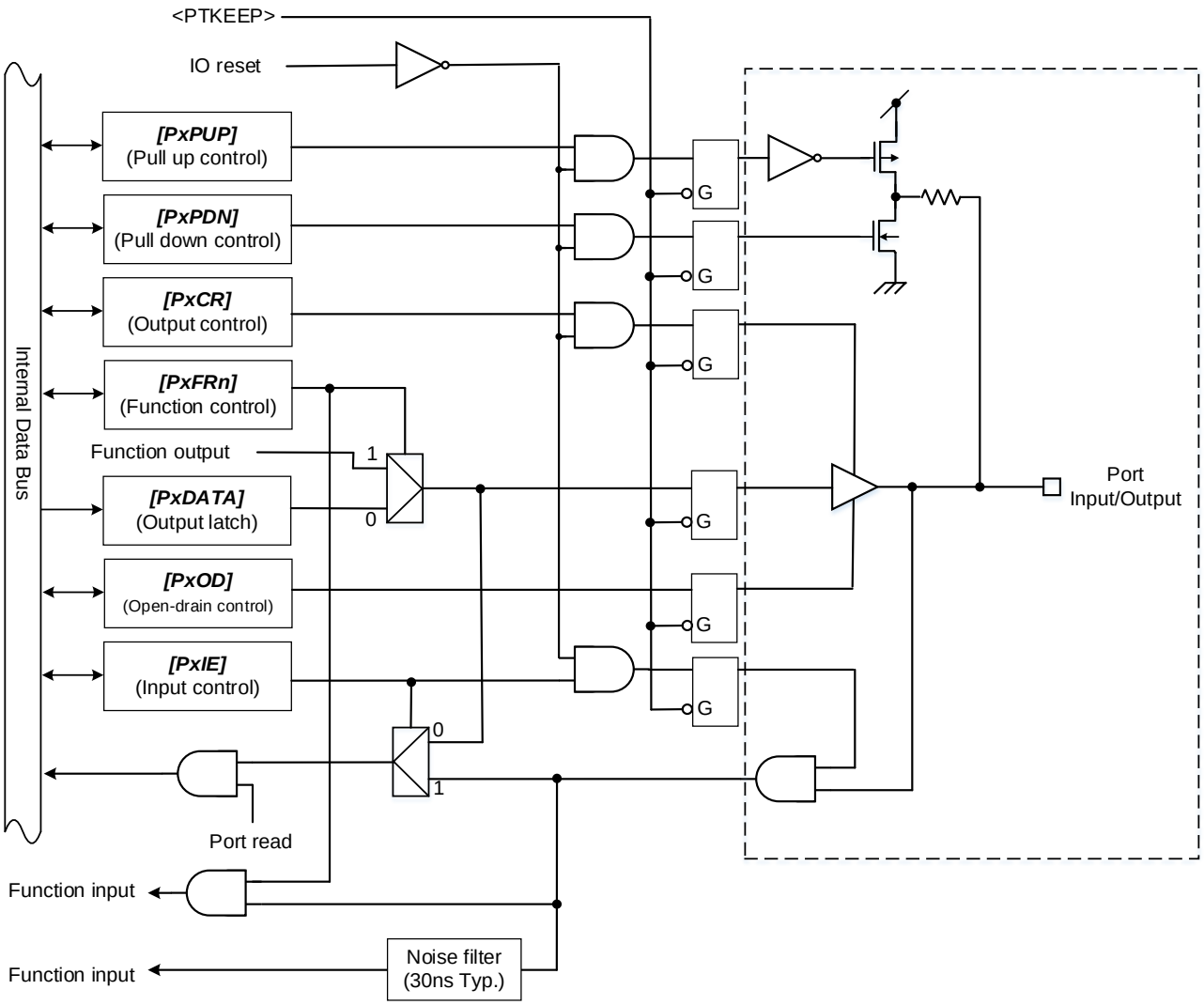


Figure 5.8 Port Type FT12

5.9. Type FT13

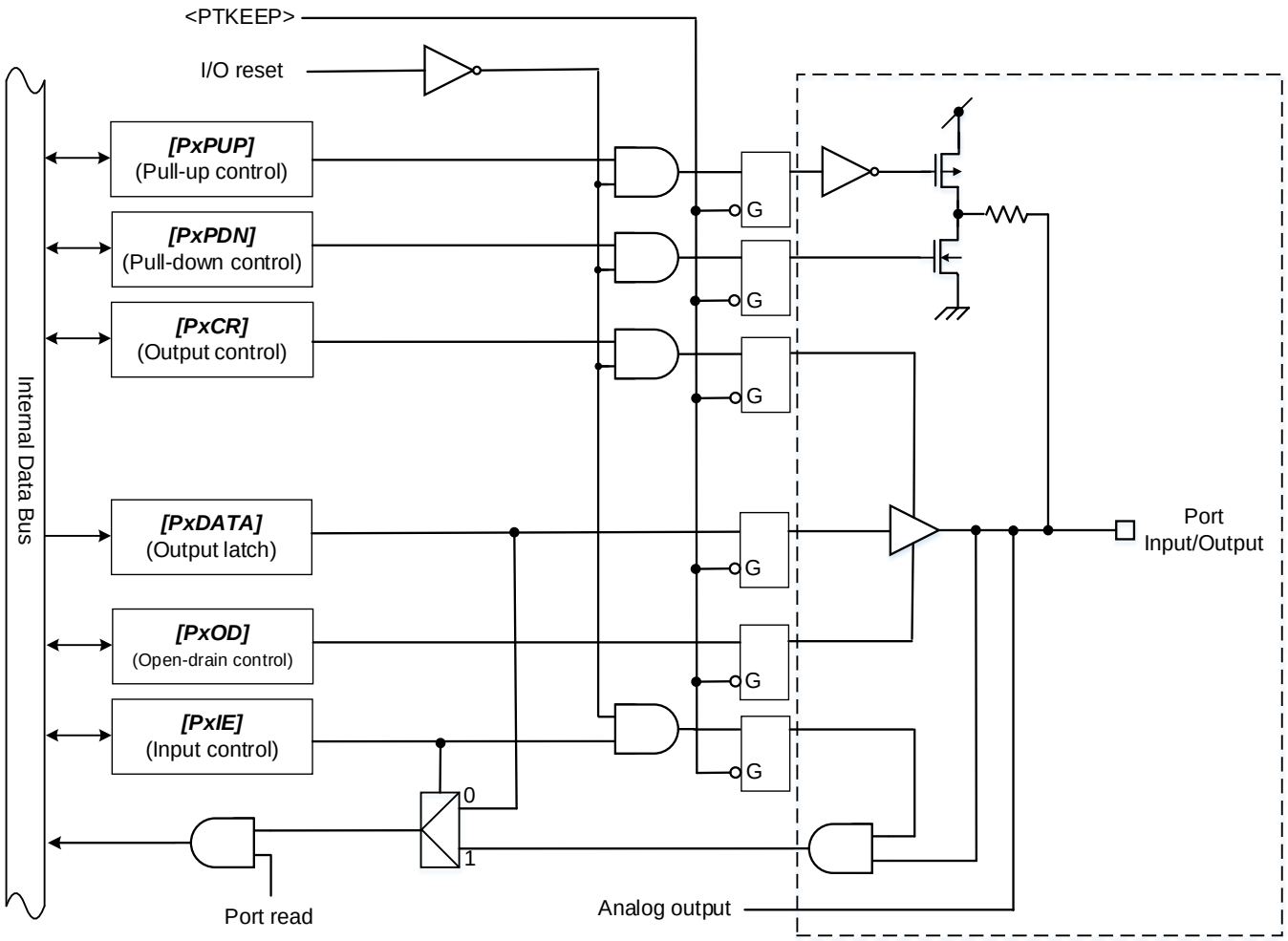


Figure 5.9 Port Type FT13

6. Precaution

6.1. pin status during a reset period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins(PK2-PK6) are debug pin status.
- PB0(BOOT_N) works as a BOOT function. It is enabled to be input and pulled-up during pin reset period. At the rising edge of the reset signal, if PB0 is "High", the device enters single chip mode and boots from the on chip flash memory. If PB0 is "Low", the device enters single BOOT mode and boots from the internal BOOT program.

6.2. Unused pins

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important points of using debug interface pins used as general-purpose ports

After releasing reset, If the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected.

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer reference manual of "Flash Memory".

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2017-09-08	First release
2.0	2018-03-05	- 1. Outlines Corrected: Table 1.1(Function) "Interrupt control"→"External Interrupt" "High frequency resonator"→"High speed clock" "Low frequency resonator"→"Low speed clock" Corrected: Table 1.1(Description) "High frequency resonator connection pin" →"High speed resonator connection pin, External high speed clock input" - 2.1. Clock supply Added: "Some products do not have all registers. " - 3. Signal connection list Add item column (Table3.1 to 3.3, 3.5 to 3.7) Corrected: Table 3.7 (Function name: "SCOUT" move down) - 4. Registers Corrected: ***[PxIE]*** Description column in the table "It takes some time that an external data is reflected on ***[PxDATA]*** after the [PxIE] is enabled. " →"It takes 100ns(Max) that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled. " - 4.1. List of Register Added: Table 4.2 "Note: Do not access the addresses described as "-" " (2 places) - 4.2.1. Setting of using the function pin Corrected: Explanation contents - 4.2.2. PORT A Corrected: Table 4.3 I2C1SCL "FT12"→"FT1" , I2C1SDA "FT12"→"FT1" - 4.2.9. PORT H Corrected: Table 4.10 PH0(EHCLKIN) ***[PHIE]*** "0"→"1" - 4.2.11. PORT K Corrected: Table 4.12 PK7(T32A04INB1) ***[PKFRn]*** " ***[PKFR2]*** "→" ***[PKFR3]*** " - 4.2.12. PORT L Corrected: Table 4.3 I2C2SCL "FT12"→"FT1" , I2C2SDA "FT12"→"FT1" - 5.7. Type FT11 Corrected: Figure 5.7 Branch of EHCLKIN signal. - 5.8. Type FT12 Corrected: Figure 5.8 Noise filter position.
2.1	2018-10-18	- Conventions Modified explanation of trademark - 4. Registers Added: "Type" field to the table. - 4.2.5. PORT D, - 4.2.6. PORT E, - 4.2.7. PORT F Modifyed: Note "When using analog input," → "When using analog input(AINAx)," - 4.2.8. PORT G Modifyed: Note "When using analog output," → "When using analog output(DACx)," - 4.2.11. PORT K Correted: PK1 OVV0_N "Output" → "Input", ***[PKCR]*** "1" → "0", ***[PKIE]*** "0" → "1" - 6.1. pin status during a reset period Corrected: "It is enabled to be input and pulled-up during reset period." → "It is enabled to be input and pulled-up during pin reset period." Corrected: ", the device enters single BOOT mode and boots from the internal BOOT ROM program." → ", the device enters single BOOT mode and boots from the internal BOOT program."

		- RESTRICTIONS ON PRODUCT USE Replaced
2.2	2019-07-26	1. Outlines Corrected Function Classification: Debug pin to Debug pins, Control pin to Control pins 2.1 Clock supply Deleted unused register name 3. Signal connection list Corrected M3H1/M3H2 of Boundary Scan in Table 3.7 : each pin No to "-" Divided "Debug interface" and "Boundary Scan" in Table 3.7 Added Note in Table 3.7 4.2.11 PORT K Corrected Port Type of TDI,TDO/SWV: FT2 to FT1 4.2.12 PORT L Corrected ***[PLFRn]*** of PL4 0 to N/A 5. Block Diagrams of Ports Added description 5.1 Type FT1 Added Note 5.7 Type FT11 Corrected connection of Function Input

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