32-bits RISC Microcontroller

TMPM3H Group(1)

Reference manual
Memory Map
(MMAP-M3H(1))

Revision 1.2

2019-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

Related document

Document name
Arm® documentation set for the Arm Cortex®-M3 processor

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

APB	Advanced Peripheral Bus
ADC	Analog to Digital Converter
A-ENC	Advanced Encoder Input Circuit
AO	Constant energization region(8bit Bus)
CG	Clock control & Generations
DAC	Digital to Analog Converter
D-Bus	DCode memory interface
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
I^2C	Inter-Integrated Circuit
I2CS	I^2C wake-up circuit from Stand-by mode
IA(INTIF)	Interrupt control register A
IB(INTIF)	Interrupt control register B
I-Bus	ICode memory interface
IMN	Interrupt Monitor
IO	IO Bus(32bit Peripheral Bus)
LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
PMD+	Programmable Motor Control Circuit Plus
RLM	Low speed oscillation / power supply control / reset
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
S-Bus	System interface
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Memory Map

The memory maps for TMPM3H Group(1) are based on the Arm Cortex-M3 processor core memory map. The internal ROM, internal RAM and special function registers (SFR) of TMPM3H Group(1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M3 respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register region is the processor core’s internal register region.

For more information on each region, see the "Arm documentation set for the Arm Cortex-M3 processor".

Note that access to regions indicated as "Fault" causes a bus fault if bus faults are enabled, or causes a hard fault if bus faults are disabled. Also, do not access the vendor-specific region.

1.1. TMPM3HxFW

Code Flash	:	128KB
RAM	:	16KB
Data Flash	:	32KB
Target product	:	TMPM3H6FWFG, TMPM3H6FWDFG, TMPM3H5FWFG, TMPM3H5FWDFG, TMPM3H4FWUG, TMPM3H4FWFG, TMPM3H3FWUG, TMPM3H2FWQG, TMPM3H2FWDUG, TMPM3H1FWUG

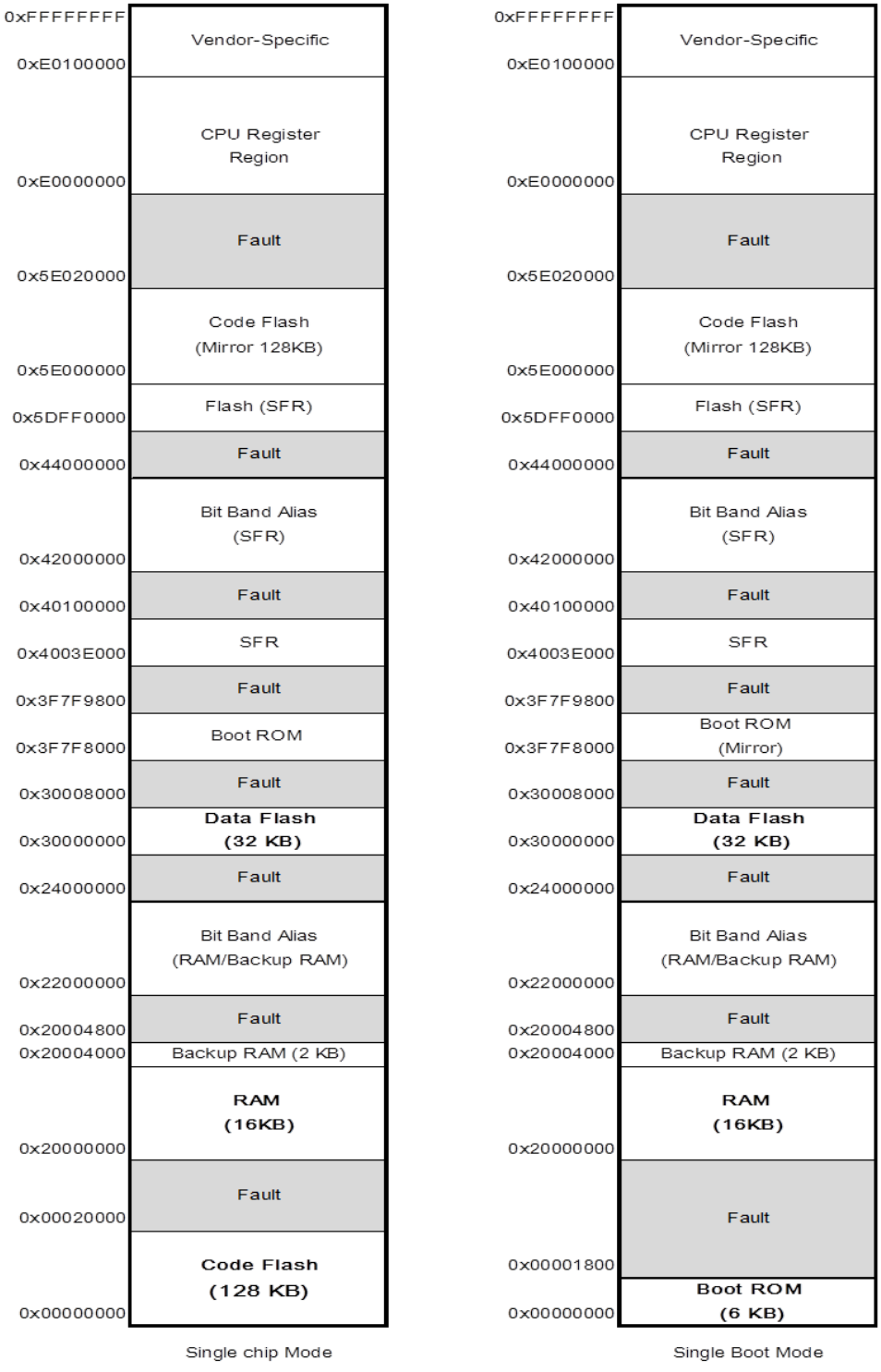

Figure 1.1 TMPM3HxFW

1.2. TMPM3HxFU

Code Flash : 96KB
RAM : 12KB
Data Flash : 32KB
Target product : TMPM3H6FUFG, TMPM3H6FUDFG, TMPM3H5FUFG, TMPM3H5FUDFG, TMPM3H4FUUG, TMPM3H4FUFG, TMPM3H3FUUG, TMPM3H2FUQG, TMPM3H2FUDUG, TMPM3H1FUUG

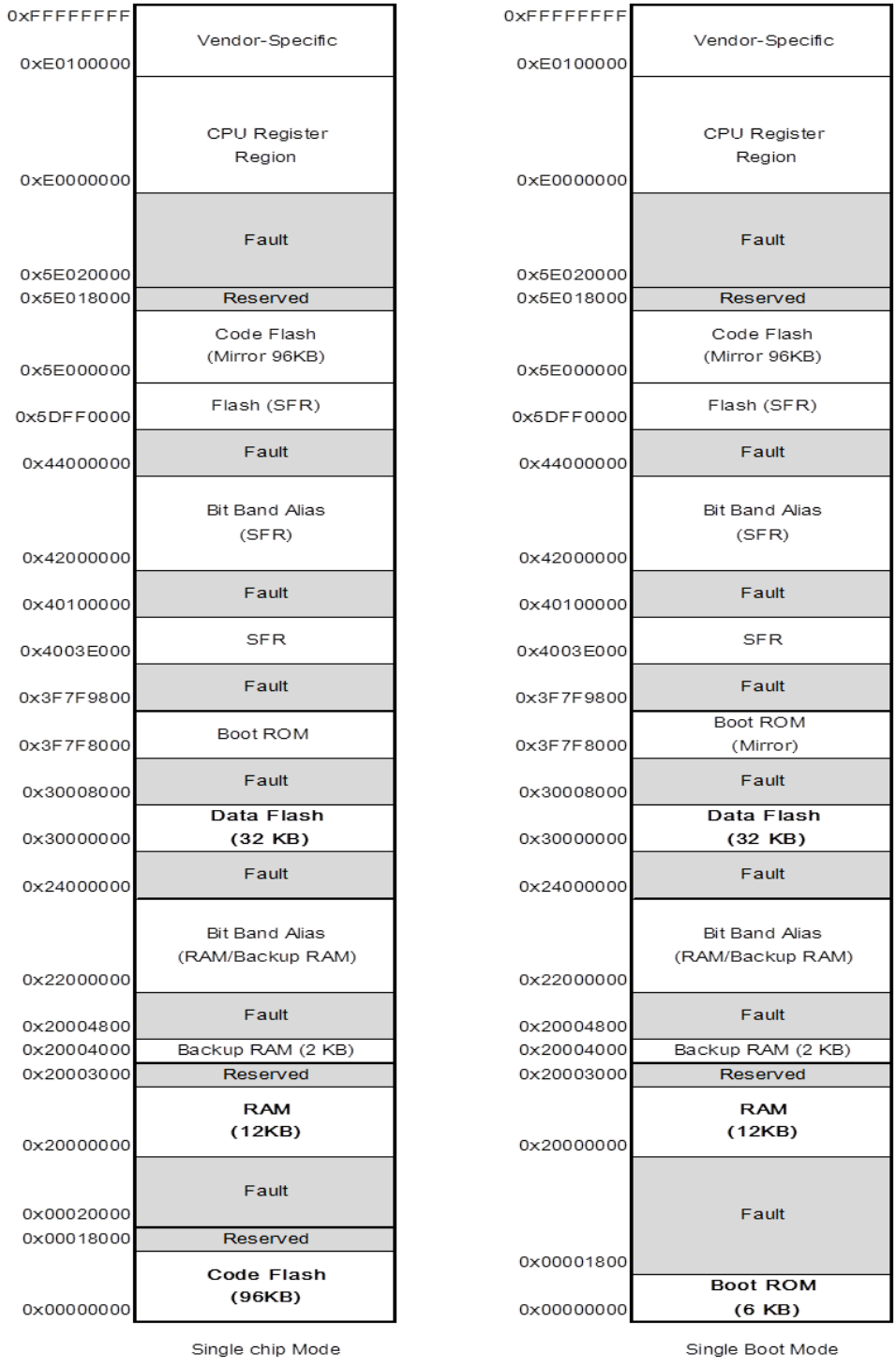

Figure 1.2 TMPM3HxFU

1.3. TMPM3HxFS

Code Flash	:	64KB
RAM	:	8KB
Data Flash	:	16KB
Target product	:	TMPM3H6FSFG, TMPM3H6FSDFG, TMPM3H5FSFG, TMPM3H5FSDFG, TMPM3H4FSUG, TMPM3H4FSFG, TMPM3H3FSUG, TMPM3H2FSQG TMPM3H2FSDUG, TMPM3H1FSUG, TMPM3H0FSDUG

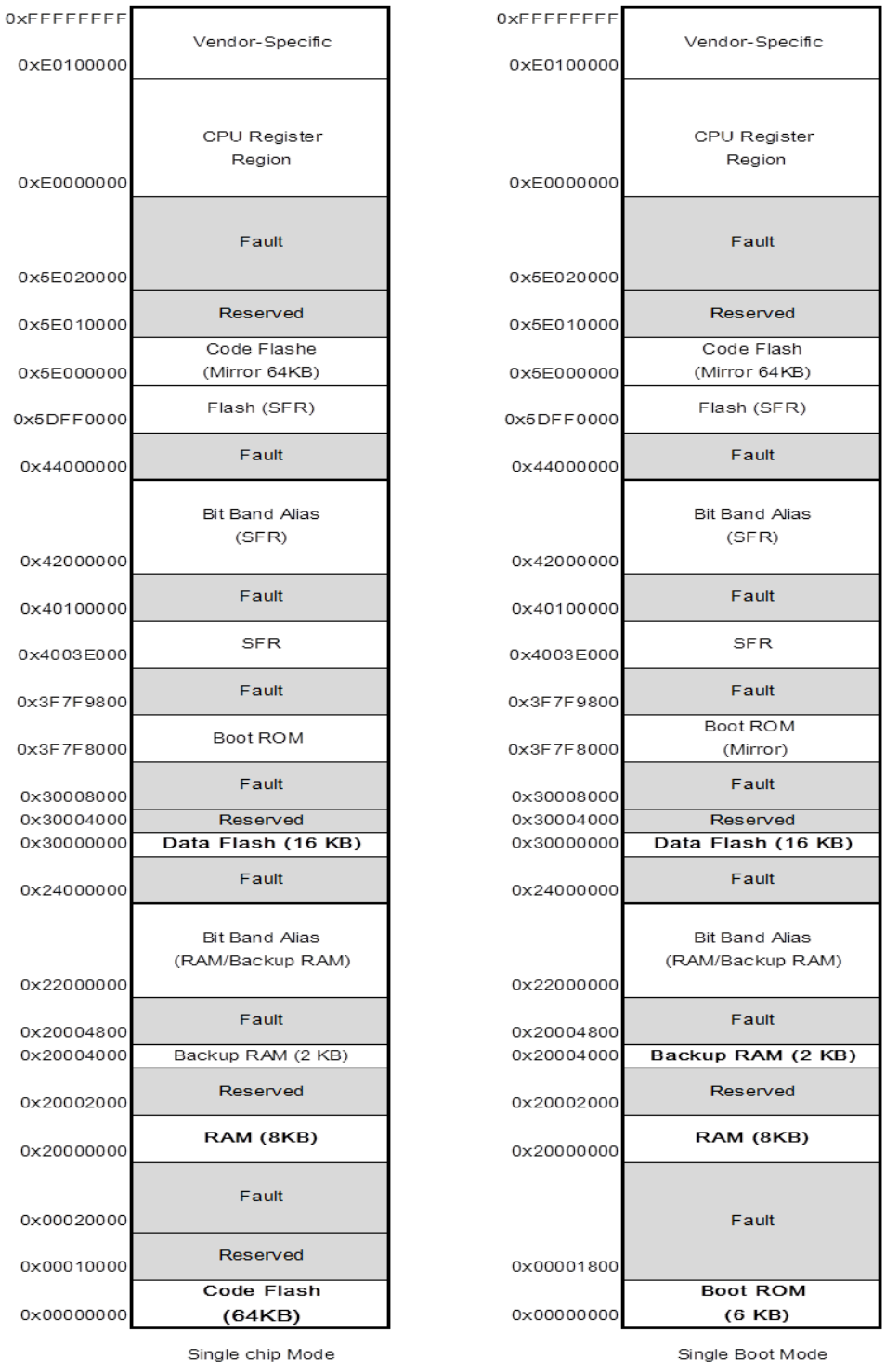

Figure 1.3 TMPM3HxFS

1.4. TMPM3HxFP

Code Flash	:	48KB
RAM	:	6KB
Data Flash	:	8KB
Target product	:	TMPM3H1FPUG

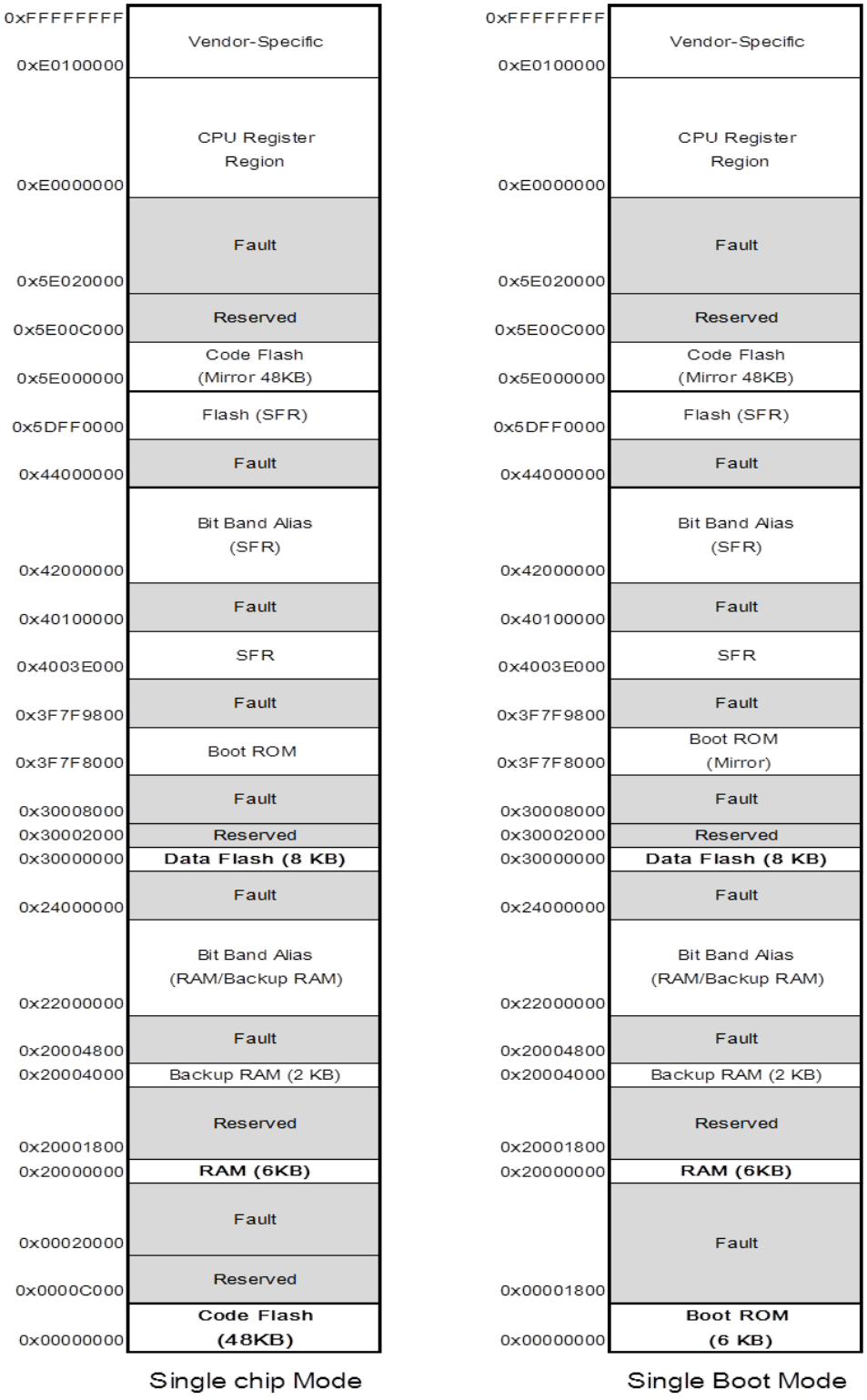

Figure 1.4 TMPM3HxFP

1.5. TMPM3HxFM

Code Flash : 32KB
RAM : 6KB
Data Flash : 8KB
Target product : TMPM3H0FMDUG

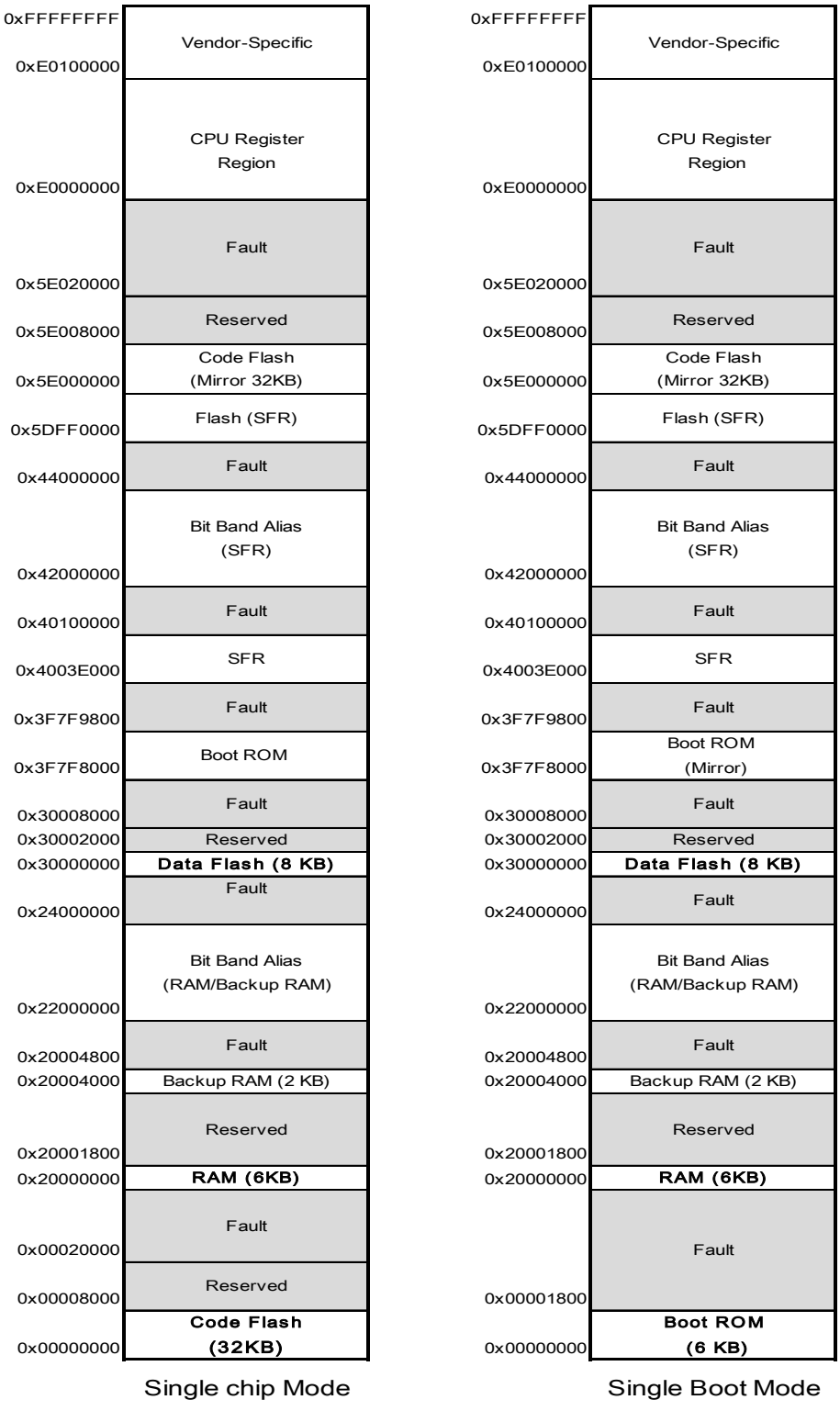

Figure 1.5 TMPM3HxFM

2. Bus Matrix

This MCU contains two bus masters such as a CPU core and DMA controllers.

Bus masters connect to slave ports (S0 to S3) of Bus Matrix. In the bus matrix, master ports (M0 to M14) connect to peripheral functions via connections described as (o) or (●) in the following figure. (●) shows a connection to a mirror area.

While multiple slaves are connected on the same bus master line in the Bus Matrix, if multiple slave accesses are generated at the same time, a priority is given to access from a master with the smallest slave number.

2.1. Structure

2.1.1. Single chip mode

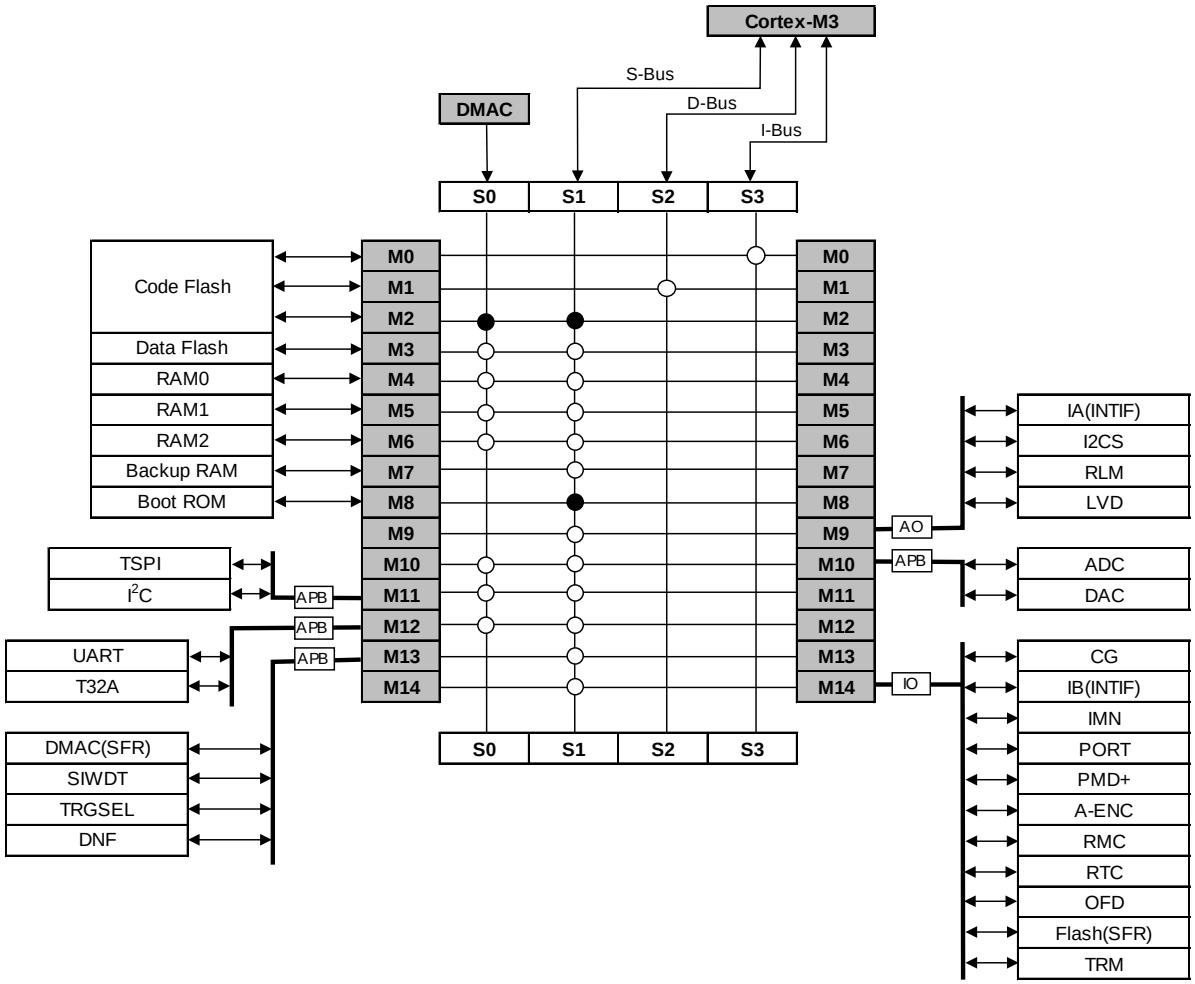

Figure 2.1 Single chip mode

2.1.2. Single boot mode

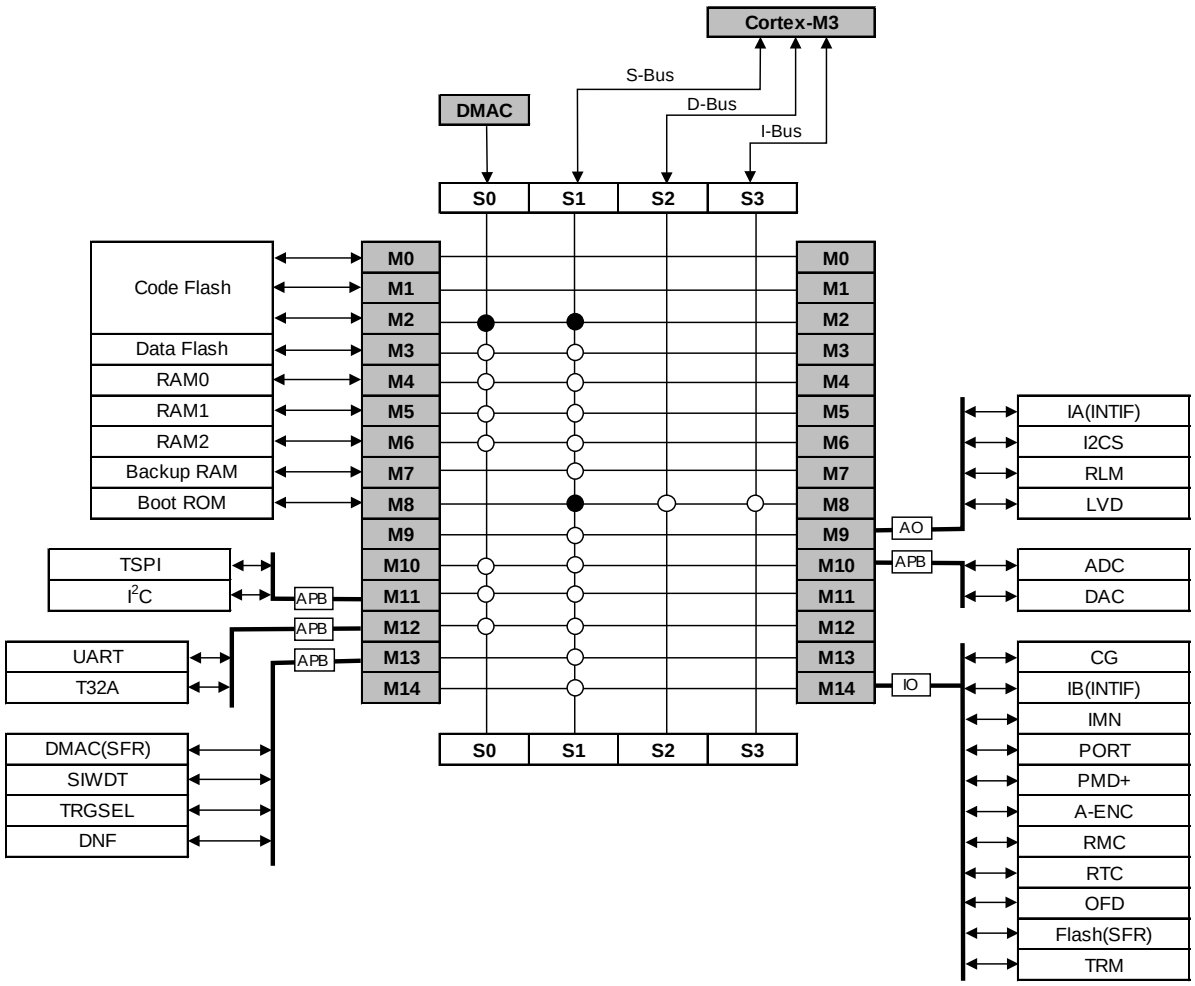

Figure 2.2 Single boot mode

2.2. Connection table

2.2.1. Memory connection

(1) Single chip mode

Table 2.1 Single chip mode

Start Address	Slave		Master			
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2	S3
0x00000000	Code Flash	M0	Fault	-	Fault	✓
		M1	Fault	-	✓	Fault
0x00020000	Fault	-	Fault	-	Fault	Fault
0x20000000	RAM0	M4	✓	✓	-	-
0x20001000	RAM1	M5	✓	✓	-	-
0x20002000	RAM2	M6	✓	✓	-	-
0x20004000	Backup RAM	M7	Fault	✓	-	-
0x20004800	Fault	-	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	✓	-	-
0x24000000	Fault	-	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	-	-
0x3F7F8000	Boot ROM	M8	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	-	-
For the address of this area, refer to "Table 2.3 Peripheral function conection".						
0x5E000000	Code Flash (Mirror)	M2	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(2) Single boot mode

Table 2.2 Single boot mode

Start Address	Slave		Master			
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2	S3
0x00000000	Boot ROM	M8	Fault	Fault	✓	✓
0x00001800	Fault	-	Fault	Fault	Fault	Fault
0x20000000	RAM0	M4	✓	✓	-	-
0x20001000	RAM1	M5	✓	✓	-	-
0x20002000	RAM2	M6	✓	✓	-	-
0x20004000	Backup RAM	M7	Fault	✓	-	-
0x20004800	Fault	-	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	✓	-	-
0x24000000	Fault	-	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M8	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	-	-
For the address of this area, refer to "Table 2.3 Peripheral function conection".						
0x5E000000	Code Flash (Mirror)	M2	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.2. Peripheral function conection

Table 2.3 Peripheral function conection

Start Address	Slave		Master			
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2	S3
0x40000000	Fault	-	Fault	Fault	-	-
0x4003E000	IA (INTIF)	M9	Fault	✓	-	-
0x4003E400	RLM		Fault	✓	-	-
0x4003E800	I2CS		Fault	✓	-	-
0x4003EC00	LVD		Fault	✓	-	-
0x4004C000	DMAC (SFR)	M13	Fault	✓	-	-
0x40054000	DAC (ch0-1)	M10	✓	✓	-	-
0x40098000	TSPI (ch0-1)	M11	✓	✓	-	-
0x400A0000	I^2C (ch0-2)	M11	✓	✓	-	-
0x400B8800	ADC	M10	✓	✓	-	-
0x400BA000	T32A (ch0-5)	M12	✓	✓	-	-
0x400BB000	UART (ch0-3)	M12	✓	✓	-	-
0x400BB400	SIWDT	M13	Fault	✓	-	-
0x400BB600	DNF		Fault	✓	-	-
0x400BB800	TRGSEL		Fault	✓	-	-
0x400C0000	PORT	M14	Fault	✓	-	-
0x400CC000	RTC		Fault	✓	-	-
0x400E7000	RMC		Fault	✓	-	-
0x400F1000	OFD		Fault	✓	-	-
0x400F3000	CG		Fault	✓	-	-
0x400F3200	TRM		Fault	✓	-	-
0x400F4E00	IB (INTIF)		Fault	✓	-	-
0x400F4F00	IMN		Fault	✓	-	-
0x400F6000	PMD+		Fault	✓	-	-
0x400F7000	A-ENC		Fault	✓	-	-
0x40100000	Fault	-	Fault	Fault	-	-
0x42000000	Bit Band Alias	-	Fault	✓	-	-
0x44000000	Fault	-	Fault	Fault	-	-
0x5DFF0000	Flash(SFR)	M14	Fault	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2017-09-07	First release
1.1	2018-06-25	- Terms and Abbreviations: The mistyping was corrected. - 2.1.1. Single chip mode / 2.1.2 2.1.2. Single boot mode Deleted “APB: Advanced Peripheral Bus, AO: 8bit-Bus for the non-block domain, IO: 32bit-Bus for the block domain” in Figure 2.1 and Figure 2.2. - 2.2.1. Code area / SRAM area Corrected contents in Table 2.1 and Table 2.2. - 2.2.2. Peripheral area Corrected chapter name and table name (Table 2.3). Corrected contents in Table 2.3.
1.2	2019-07-23	- Related document Modified "Arm documentation set Cortex-M3" to "Arm® documentation set for the Arm Cortex®-M3 processor" - Conventions Updated convension and trademark - Terms and Abbreviations Added D-Bus, I-Bus and S-Bus Modified "INT-I/F" to "INTIF" - 1.Memory Map Modified "TMPM3H(1) group" and "TMPM3H group" to "TMPM3H group(1)" Modified "CPU register area" to "CPU register region" Modified "Arm documentation set Cortex-M3" to "Arm documentation set for the Arm Cortex-M3 processor" Modified "memory fault" to "bus fault" - 2.1.Structure Figure 2.1 and Figure 2.2: Modified "System" to "S-Bus" Modified "Data" to "D-Bus" Modified "Instruction" to "I-Bus" - 2.2.1. Title: Modified "Code area/SRAM area" to "Memory connection" Table 2.1 Start Address 0x00020000 / D-Bus and I-Bus: Modified "-" to "Fault" - 2.2.2. Title: Modified "Peripheral area" to "Peripheral function conection" Table 2.3 Title: Modified "Peripheral area" to "Peripheral function conection" - RESTRICTIONS ON PRODUCT USE Updated

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