Photocouplers IRED & Photo ICTLP555

TLP555

- Isolated Bus Driver
- High Speed Line Receiver
- Microprocessor System Interfaces
- O MOS FET Gate Driver
- Transistor Inverter

The TOSHIBA TLP555 consists of an infrared emitting diode and integrated high gain, high speed photodetector.

This unit is 8-lead DIP package.

The detector has a three state output stage that eliminates the need for pull-up resistor, and built-in Schmitt trigger. The detector has a Schmitt trigger circuit and 3 State output circuit, so both-directions of source and sink drive can be performed.

The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V / μs .

TLP555 is a buffer logic type. When an inverter logic type is required, there is TLP558.

- Input current : I_F = 1.6 mA (max.)
- Power supply voltage: V_{CC} = 4.5 to 20 V
- Switching speed : t_{pHL}, t_{pLH} = 400 ns (max.)
- Common mode transient immunity: ±1000V / μs (Min.)
- Guaranteed performance over temperature: −25 to 85°C
- Isolation voltage: 2500 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

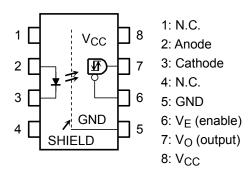
Unit: mm 7.62±0.25 0.25+0.10 JEDEC JEITA. TOSHIBA 11-10C4S

Weight: 0.54 g (typ.)

Truth Table (positive logic)

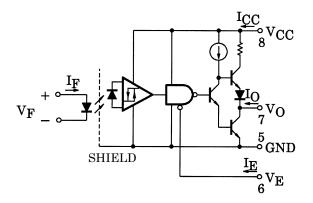
Input	Enable	Output
Н)#	Z (
✓ (()) н	Z
H		H
	\ \ \ \ \	

Pin Configuration (top view)



Start of commercial production 1986-07

Schematic



Note : 0.1- μF bypass capacitor must be connected between pin 8 and pin 5.

Absolute Maximum Ratings $(T_a = 25 \, ^{\circ}C)$

Characteristics		Symbol	Rating	Unit
	Input forward current	I_{F}	10	mA
LED	Peak transient input forward current (Note 1)	I _{FPT}	1	Α
LED	Input reverse voltage	V _R	5	V
	Input power dissipation(Ta= to 85°C)	P _D (7)	45	mW
	Output current	I ₀	40 / –25	mA
Detector	Peak output current (Note 2)	IOP	80 / -50	mA
	Output voltage	Vo	-0.5 to 20	V
	Supply voltage	Vcc	-0.5 to 20	V
	Three state enable voltage	VE	-0.5 to 20	V
	Output power dissipation (Note 3)	PO	100	mW
	Total package power dissipation (Note 4)	P _T	200	mW
Common	Operating temperature range	T _{opr}	-40 to 85	°C
	Storage temperature range	T _{stg}	-55 to 125	°C
	Lead solder temperature (10 s) **	T _{sol}	260	°C
	Isolation voltage (AC 60 s, R.H. ≤ 60 %) (Note 5)	BVS	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) \leq 1 μ s, 300 pps

Note 2: PW \leq 5 μ s, Duty \leq 0.025%

Note 3: Derate 1.8 mW / °C above 70 °C ambient temperature.

Note 4: Derate 3.6 mW / °C above 70 °C ambient temperature.

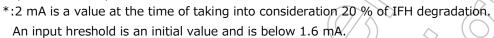
Note 5: Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5,6,7 and 8 shorted together

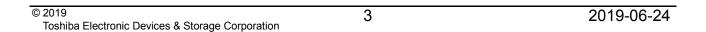
** : More than 2 mm from the root of a lead.

Recommended Operating Conditions

Characteristics	Symbol	Min.	Тур.	Max	Unit
Input on-state current	I _{F (ON)}	2*	_	5	mA
Input off-state voltage	V _F (OFF)	0	/	0.8	V
Supply voltage	V _{CC}	4.5	1	20	V
Enable voltage high	V _{EH}	2.0		20	V
Enable voltage low	V _{EL}	(0)	<u> </u>	0.8	V
Fan out (TTL load)	N		リー	4	_
Operating temperature	Topr	-25		85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.





Electrical Characteristics

(Unless otherwise specified, Ta = -25 to $85^{\circ}C$, $V_{CC} = 4.5$ to 20 V)

Characteristics	Symbol	Test Co	ndition	Min.	Typ.(*)	Max	Unit
Input forward voltage	V _F	$I_F = 5 \text{ mA}, Ta = 2$	7	1.55	1.7	V	
Input forward voltage temperature coefficient	ΔV _F /ΔTa	I _F = 5 mA	(-2.0	_	mV /°C	
Input reverse curren	I _R	$V_R = 5 \text{ V, Ta} = 25$	77	_	10	μΑ	
Input capacitance	C _T	V _F = 0 V, f = 1 M	Hz, Ta = 25 °C	(\mathcal{A})	45	_	pF
Output leakage current $(V_0 > V_{CC})$	I _{OHH}	I _F = 5 mA, V _{CC} = 4.5 V V _F = GND	$V_0 = 5.5 \text{ V}$ $V_0 = 20 \text{ V}$)-	_ 2	100 500	μΑ
Logic low output voltage	V _{OL}	I _{OL} = 6.4 mA, V _F V _E = 0.8 V		_	0.4	0.5	V
Logic high output voltage	V _{OH}	$I_{OH} = -2.6 \text{ mA, I}$ $V_E = 0.8 \text{ V}$	E = 1.6 mA	2.4	3.3	> -	V
Logic low enable current	I _{EL}	V _E = 0.4 V			T0.13	0.32	mA
Logic high enable current	I _{EH}	$V_E = 2.7 V$ $V_E = 5.5 V$ $V_E = 20 V$	>	9		20 100 250	μА
Logic low enable voltage	V _{EL}	VE - 20 V	_ ((7)		0.01	0.8	V
Logic high enable voltage	V _{EH}			2.0	_	_	V
Logic low supply current	ICCL	$V_F = 0 \text{ V}, V_E = GI$	V _{CC} = 5.5	_	5	6.0	mA
			V _{CC} = 20 V	_	5.6	7.5	
Logic high cupply current	[CCH]	I _F = 5 mA	V _{CC} =5.5 V	_	2.5	4.5	mΛ
Logic high supply current		V _E = GND	V _{CC} = 20 V	_	2.8	6.0	mA
_ (7	// I _{OZL}	$I_F = 5 \text{ mA}, V_E = 2 \text{ V} V_O = 0.4 \text{ V}$		_	1	-20	
High impedance state output current	₇ I _{OZH}		$V_0 = 2.4 \text{ V}$		20		
riigii irripedance state output current		$V_F = 0 V, V_E = 2$	$V V_0 = 5.5 V$	_	_	100	μΑ
~~			$V_0 = 20 \text{ V}$	_	0.01	500	
Logic low short circuit output current	I _{OSL}	4/C — O 4	$V_{CC} = V_{CC} = 5.5 \text{ V}$	25	55		mA
(Note 6)		$V_E = 0.8 \text{ V}$	$v_0 = V_{CC} = 20 \text{ V}$	40	80	_	ША
Logic high short circuit output current	Iosh	$I_F = 5 \text{ mA}, V_O = GN$	_{GND} V _{CC} =5.5 V	-10	-25	<u> </u>	mA
(Note 6)		$V_E = 0.8V$ $V_{CC} = 20 \text{ V}$		-25	-60	_	111/4
Threshold input current (L/H)	IFH	V _E = 0.8 V, I _O = V _O > 2.4 V	−2.6 mA	_	0.4	1.6	mA
Threshold input voltage (H/L)	VFL	V _E = 0.8 V, I _O = V _O < 0.4 V	0.8	_	_	V	
Input current hysteresis	I _{HYS}	$V_{CC} = 5 \text{ V}, V_{E} = 0$		0.05		mA	
Isolation resistance	R _S	$V_S = 500 \text{ V, R.H.}$ Ta = 25 °C	5×10 ¹⁰	10 ¹⁴	-	Ω	
Total capacitance (input to output)	C _S	$V_S = 0 V, f = 1 M$	_	1.0	_	pF	

^{* :} All typ. values are at Ta = 25 °C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

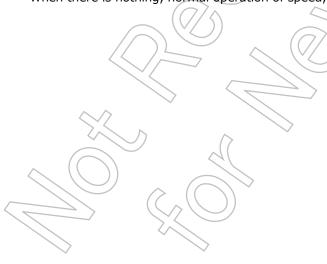
Note 6: Duration of output short circuit time should not exceed 10 ms.

Switching Characteristics (unless otherwise specified, Ta = 25°C, $V_{CC} = 4.5$ to 20 V)

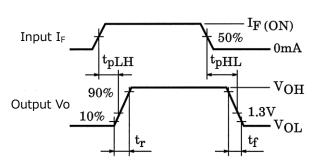
Characteristic	Symbol	Test Circuit	Test Condition	Min.	Тур. (*)	Max.	Unit
Propagation delay time to logic high output level (L \rightarrow H) (Note 7)	t _{pLH}		$I_F = 0 \rightarrow 3 \text{ mA}$	1	235	400	ns
Propagation delay time to logic low output level ($H \rightarrow L$) (Note 7)	t _{pHL}	1	I _F = 3→0 mA		250	400	ns
Output rise time (10-90%)	t _r		$I_F = 0 \rightarrow 3 \text{ mA}, V_{CC} = 5 \text{ V}$	7/1	35	75	ns
Output fall time (90–10%)	t _f		$I_F = 3 \rightarrow 0 \text{ mA, } V_{CC} = 5 \text{ V}$		20	75	ns
Common mode transient immunity at logic high output (Note 8)	CM _H	3	I _F = 1.6 mA, V _{CM} = 50 V V _{O (min)} = 2 V	1000	_	_	V / μs
Common mode transient immunity at logic low output (Note 8)	CML	3	I _F = 0 mA, V _{CM} = 50 V V _{O (max)} = 0.8 V	1000		/	V / μs

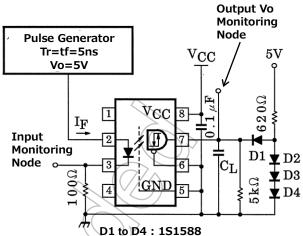
- *: All typ. values are at Ta = 25 °C, V_{CC} = 5 V unless otherwise specified.
- Note 7: The t_{pLH} propagation delay is measured from the 50 % point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{pHL} propagation delay is measured from the 50 % point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
- Note 8: CML is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (Vo ≤ 0.8 V).

 CMH is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (Vo ≥ 2.0 V).
- Note 9: Output photo IC should build in the amplifier of high sensitivity very much, and should attach bypass capacitor 0.1 uF with a sufficient high frequency characteristic to the place within 1 cm from a pin between the pin 8 (VCC) and the pin 5 (GND) as an object for oscillation prevention. When there is nothing, normal operation of speed, or ON/OFF may not be carried out.



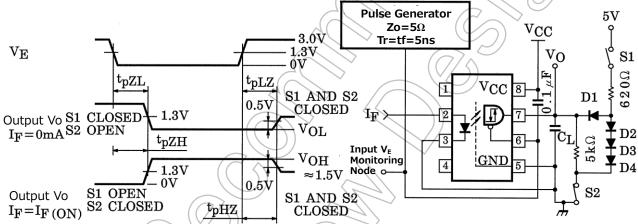
Test Circuit 1 tpHL, tpLH, tr and tf





C_L is approximately 15pF which includes probe and stray wiring capacitance.

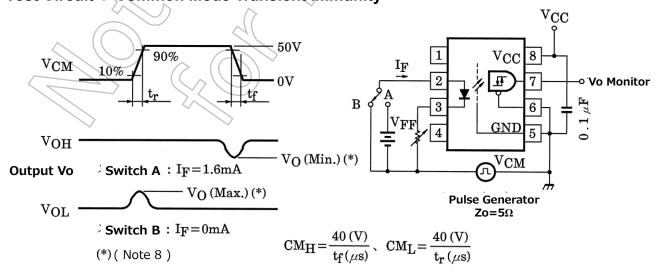
Test Circuit 2 t_{pHZ}, t_{pZH}, t_{pLZ}, and t_{pZL}



D1 to D4: 1S1588

 C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 3 Common Mode Transient Immunity



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