TC78B015AFTG
Usage considerations

Rev.1.1

Summary

The TC78B015AFTG is a 150°-trapezoid chopper typed PWM driver for three-phase brushless motors. It controls motor rotation speed by changing the PWM duty ratio, based on the speed control input.
Hall signal is supported to 1 sensor for the TC78B015AFTG.

Table 1 Product pattern

Product name	TC78B015FTG	TC78B015AFTG	TC78B015BFTG	TC78B015CFTG
Absolute maximum ratings (Power supply voltage)	25V	36V	25V	36V
Operation range (Power supply voltage)	6 to 22V	6 to 30V	6 to 22V	6 to 30V
Hall sensor spec.	1 sensor	1 sensor	3 sensors	3 sensors

This document is a reference data for designing support.
In designing final equipment, please sufficiently consider parts variations, usage conditions, etc.

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1. Power supply voltage

The absolute maximum rating of the power supply voltage (VM) must not be exceeded even for a moment. Do not exceed any of these ratings.
Please use the IC within the operation range of the power supply voltage at VM terminal. When the voltage of VM is less than 6 V, the output voltage of VREG sinks and then the IC may malfunction. Please use the IC within the VM voltage range of 6 V to 30 V.

Table 2 Absolute maximum ratings of power supply voltage (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power supply voltage	VM	36	V

Table 3 Power supply voltage operation range (Ta = 25°C)

Characteristic	Symbol	Operation range	Unit
Power supply voltage	VM_{opr}	6 to 30 V	V

2. Output current

The absolute maximum rating is 3 A that must not be exceeded, even for a moment. Design an actual application system with the IC so as not to make the inrush current and the lockout current exceed the absolute maximum ratings, especially when a motor starts up and gets stuck in the lockout.
Available average output current changes depending on the usage conditions (ambient temperature, mounting board method, and so on). Design an actual application system with a sufficient margin in order that Tj does not exceed 150°C.

3. Maximum of rotation number

The TC78B015AFTG (1-sensor spec.) recognizes its operation abnormal when the position signal frequency increases to the electrical angle frequency (3 kHz (typ.)) or more. Please determine the maximum rotation number by considering the allowance of the IC and that of the external parts of the OSCCR terminal.
During high speed rotation, disturbance of motor-current waveform and voltage boosting of VM terminal might increase. In this high-speed operation, please evaluate the operation by using an actual motor.

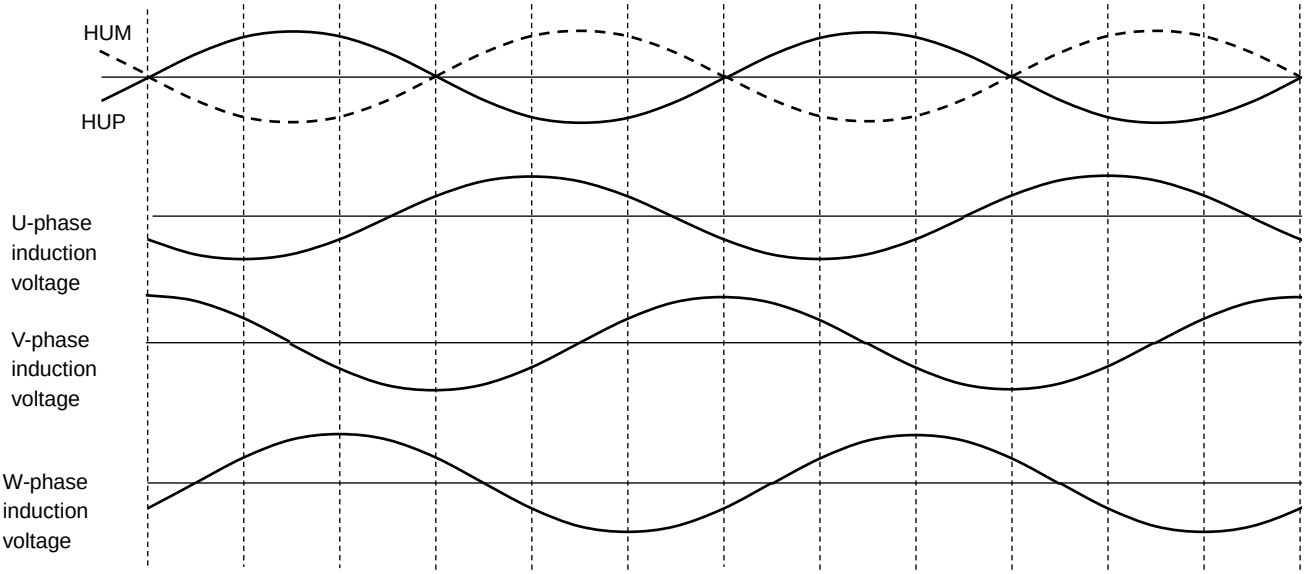
Table 4 Abnormal detection frequency of position signal and maximum of rotation number

Item	TC78B015AFTG
Abnormal detection frequency of position signal	3 [kHz] (typ.)
Maximum of rotation number (In case of 4-pole motor)	90 k [rpm] (typ.)
Maximum of rotation number (In case of 8-pole motor)	45 k [rpm] (typ.)

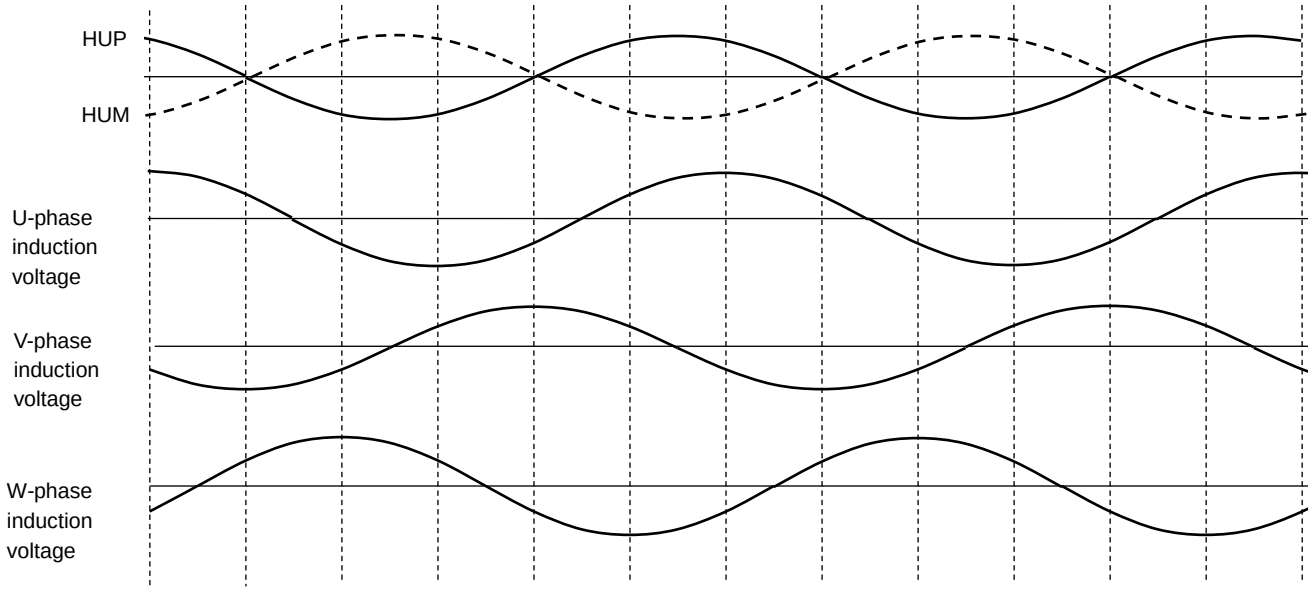
4. Notes in using the motor

Please use the motor whose phase relation between a hall sensor and induction voltage corresponds to the following timing chart.

CW/CCW=L



CW/CCW=H



5. Confirmation of start set

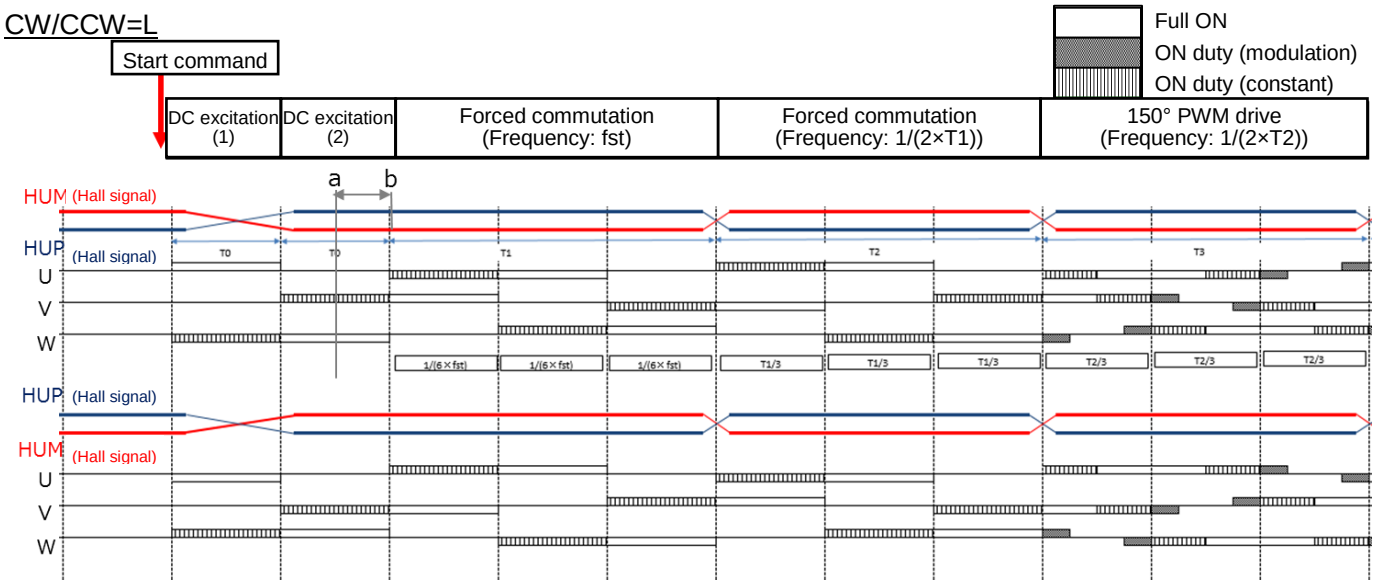
The TC78B015AFTG is one sensor drive IC. To provide enough margins in startup, please see below figures and confirm that following three conditions are satisfied.

(1) Logic of the hall signal does not switch during the term of 'a' to 'b' (T0/2) in the DC excitation mode (2).
Please confirm the logic of the hall signal with FG_OUT signal by setting FG_SEL = 3.

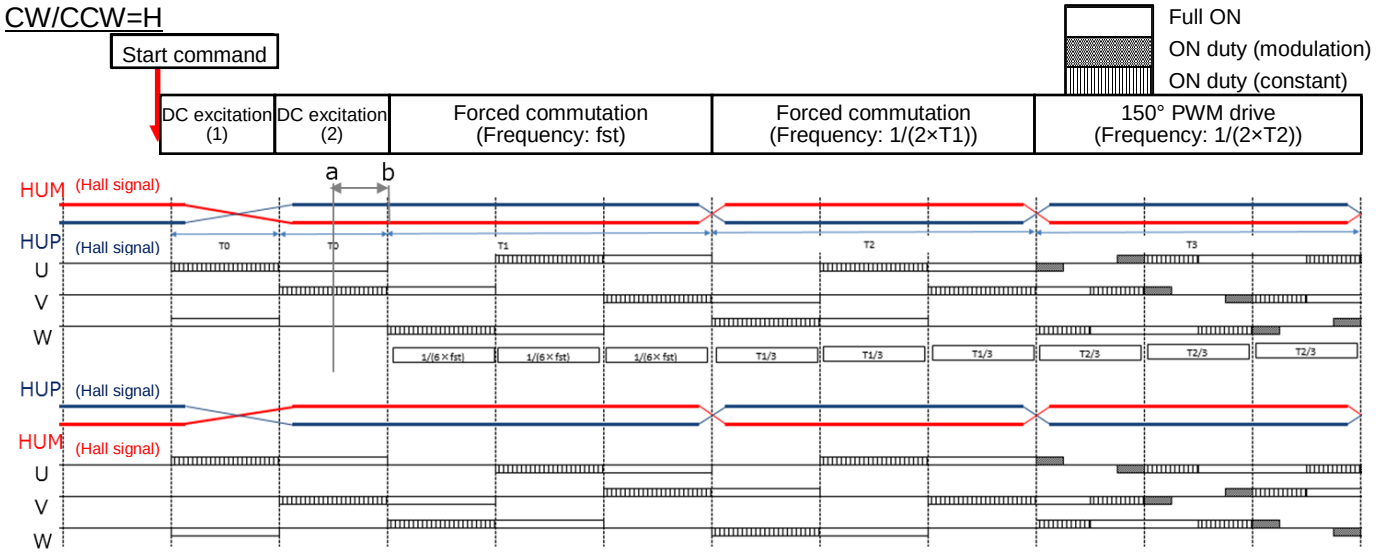
(2) T1 and T2 ≤ 1/(2×fst)

(3) Rotation direction configured by CW/CCW terminal corresponds to the motor rotation direction in the following two terms; the term of moving modes (from DC excitation mode (1) to (2)), and the term of forced commutation.

CW/CCW=L



CW/CCW=H



Note.

- In above timing chart, the lead angle is assumed zero. Commutation pattern in startup is different depending on the logics of the hall signal and the CW/CCW signal in starting.
- After forced commutation starts, each rising and falling edge of the hall signal is detected at every 180° electrical angle.
- Forced commutation starts with the frequency configured by FST terminal. Then, when the frequency of the hall signal is detected higher than this commutation frequency, the operation is switched to the 150° drive (1-sensor drive).

- During the 150° PWM drive mode, the commutation pattern of 180° electrical angle is generated between previous edges. When the edge of the hall signal is detected while the motor operation is accelerated, the commutation pattern is moved to the next pattern.
- During the forced commutation and 150° PWM drive, the detection of the hall signal is masked. The masking term corresponds to the time that the electrical angle leads to 90° from the switching timing of the hall signal.

6. Auto lead angle

When SEL_LA=1, lead angle is controlled automatically by LA terminal. The value of the lead angle changes automatically according to the frequency of the position signal as shown below. The threshold of the frequency of the position signal has the hysteresis (+0 Hz/50 Hz).

Value of lead angle [deg]

LA Number of steps	Frequency of electrical angle [Hz]									
	0 to 100	100 to 200	200 to 300	300 to 400	400 to 500	500 to 600	600 to 700	700 to 800	800 to 900	900 to 1000
7	0	1.875	1.875	1.875	1.875	3.750	3.750	3.750	3.750	5.625
6	0	1.875	1.875	3.750	3.750	5.625	5.625	7.500	7.500	9.325
5	0	1.875	1.875	3.750	5.625	7.500	7.500	9.325	11.250	13.125
4	0	1.875	3.750	5.625	9.325	11.250	13.125	15.000	18.750	20.625
3	0	1.875	5.625	7.500	11.250	13.125	16.875	18.750	22.500	24.375
2	0	3.750	5.625	9.325	13.125	16.875	18.750	22.500	26.250	30.000
1	0	3.750	7.500	11.250	15.000	18.750	22.500	26.250	30.000	33.750
0	0	1.875	3.750	5.625	7.500	9.325	11.250	13.125	15.000	16.875

Value of lead angle [deg]

LA Number of steps	Frequency of electrical angle [Hz]										
	1000 to1100	1100 to 1200	1200 to 1300	1300 to1400	1400 to1500	1500 to1600	1600 to1700	1700 to1800	1800 to1900	1900 to 2000	Over 2000
7	5.625	5.625	5.625	7.500	7.500	7.500	7.500	9.375	9.375	9.375	9.375
6	9.325	11.250	11.250	13.125	13.125	15.000	15.000	16.875	16.875	18.750	18.750
5	13.125	15.000	16.875	18.750	18.750	20.625	22.500	24.375	24.375	26.250	28.125
4	22.500	24.375	28.125	30.000	31.875	33.750	37.500	39.375	41.250	43.125	46.875
3	28.125	30.000	33.750	35.625	39.375	41.250	45.000	46.875	50.625	52.500	56.250
2	31.875	35.625	39.375	43.125	45.000	48.750	52.500	56.250	58.125	58.125	58.125
1	37.500	41.250	45.000	48.750	52.500	56.250	56.250	56.250	56.250	56.250	56.250
0	18.750	20.625	22.500	24.375	26.250	28.125	30.000	31.875	33.750	35.625	37.500

7. Application circuit example

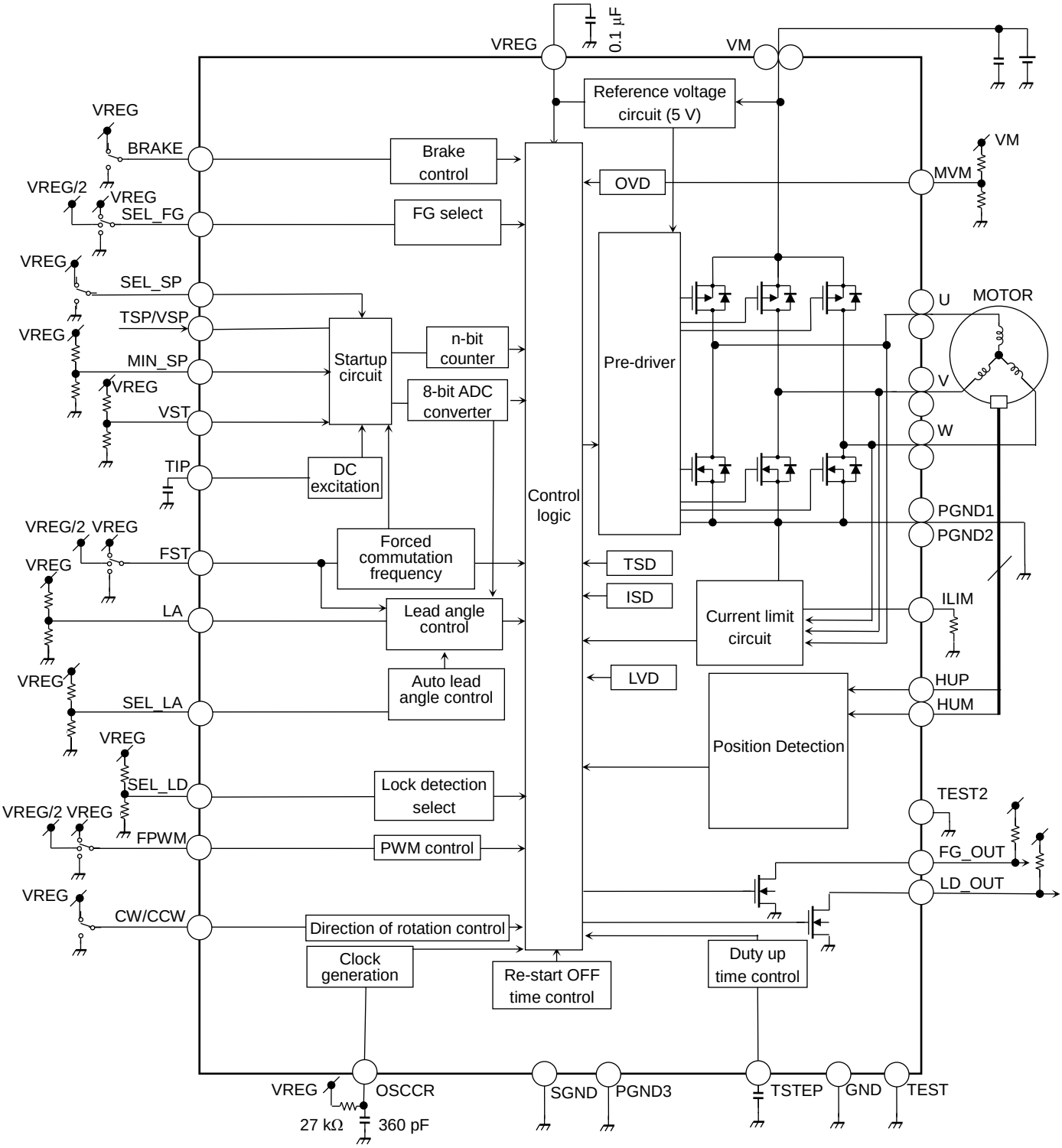


Figure 1 Application circuit example: TC78B015AFTG

(1) Capacitor for VM terminal

Take the VM wiring pattern on a print circuit board widely because large current flows from the power supply to the motor through VM terminal.
Connect an appropriate capacitor between VM terminal and PGND to stabilize the supply voltage and reduce the noise.
Moreover, place the capacitor as close to the IC as possible. In particular, the power supply variation and the noise, which generate at high frequency, can be effectively reduced by connecting ceramic capacitors (0.01 to 1 μF) in parallel near the IC.

Table 5 Capacitor of VM terminal

Item	Parts	Typ.	Recommended range
Between VM and PGND	Ceramic/electrolytic capacitor	10 μF	2.2 to 47 μF

Notes: Capacitors other than a recommendation value (excluding each part) can be used depending on the motor load conditions and the board pattern, etc.

(2) Capacitor for VREG terminal

Please connect the capacitor of 0.1 μF between VREG and SGND as close to the IC as possible in order to reduce the noise and the fluctuation of the voltage at VREG terminal.

Table 6 Capacitor of VREG terminal

Item	Parts	Typ.
Between VREG and SGND	Ceramic capacitor	0.1 μF

(3) Setting OSCCR terminal

OSCCR terminal sets reference oscillating frequency.
Please connect the capacitor of 360 pF between OSCCR terminal and SGND as close to the IC as possible not to be influenced by noise and wiring impedance. Moreover, please connect the resistor of 27 kΩ between OSCCR terminal and VREG as close to the IC as possible. 27 kΩ (typ.) and 360 pF (typ.) should be adopted as an external capacitor and resistor respectively. Please select the resistor and capacitor high-precision as much as possible. When their accuracy is low, the setting time and the frequency might be different from the typical values greatly. Recommended accuracy of the capacitor × resistor is ±30 % or less including the temperature characteristics. (When the accuracy of the capacitor is ±20 %, please apply the resistor whose accuracy is ±5 % or less.)

In addition, internal oscillating frequency can be indirectly checked by measuring the frequency of OSCCR terminal. Internal oscillating frequency and frequency of OSCCR terminal can be gained from the following formula. When internal oscillating frequency is 13 MHz, the frequency of OSCCR terminal is 406.25 kHz.

$$\text{Internal oscillating frequency [MHz]} = \text{Frequency of OSCCR terminal [kHz]} \times 32 \times 1000$$

(4) Setting ILIM terminal

ILIM terminal sets current limit value of output.
Please connect the resistor between ILIM terminal and SGND as close to the IC as possible.
The relation of the current limit value (IOUT) and the external resistance (R) is calculated in the following formula.

IOUT = 39000 / R [A]

When the external resistance is 39 kΩ, the current limit value of output is 1 A (typ.).

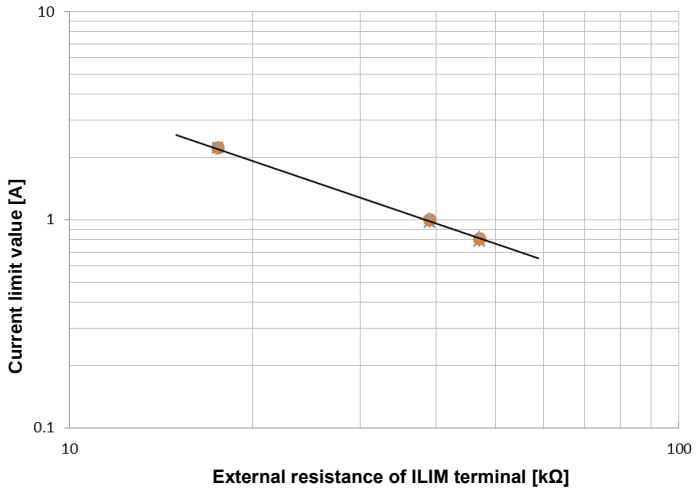


Figure 2 Relation of external resistance and current limit value

(5) Setting TIP terminal

TIP terminal sets the term of DC excitation. There are two modes in the DC excitation; DC excitation (1) and DC excitation (2). The operation moves from DC excitation (1) to DC excitation (2). Please connect the capacitor between TIP terminal and SGND and set the term of DC excitation. The range of recommended capacitance is 1 nF to 1 µF. Each term of DC excitation (1) and (2) is gained from below formula.

Term of DC excitation (1) or (2) = $32 \times 0.313 \times C \times 10^6$ [s]

When the capacitance of the external capacitor is 0.01 µF, each term of DC excitation (1) and (2) is about 0.100 s.

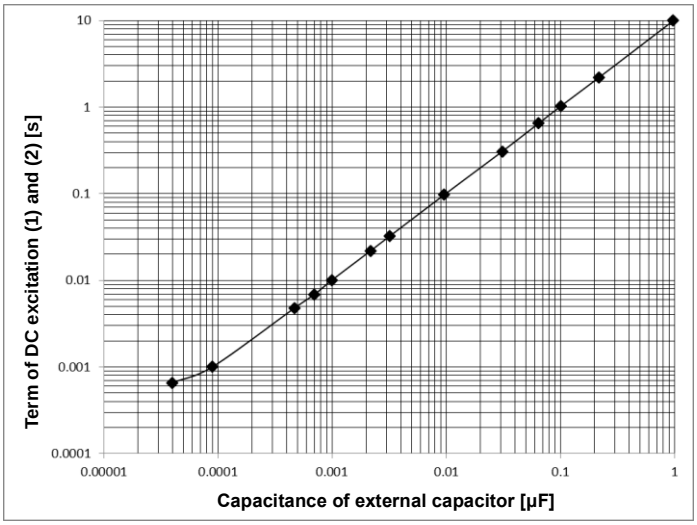


Figure 3 Relation of external capacitor and DC excitation term

(6) Setting TSTEP terminal

The duty of the input control signal of TSP/VSP terminal is reflected on the output duty. TSTEP terminal sets this reflecting time by connecting the capacitor while the duty increases and decreases. It controls rapid change of the motor rotation speed.
Please connect the capacitor between TSTEP terminal and SGND to configure the reflecting time.
It is recommended to adopt the capacitor of 1 µF or less. In case of shorting the reflecting time, please set TSTEP terminal open state.
When the duty-command value configured by TSP/VSP input changes by 2.5%, the reflecting time is calculated from following formula.

Reflecting time = $32 \times 0.313 \times C \times 10^6$ [s]

When the external capacitor is 0.01 µF, the reflecting time is about 0.100 s.

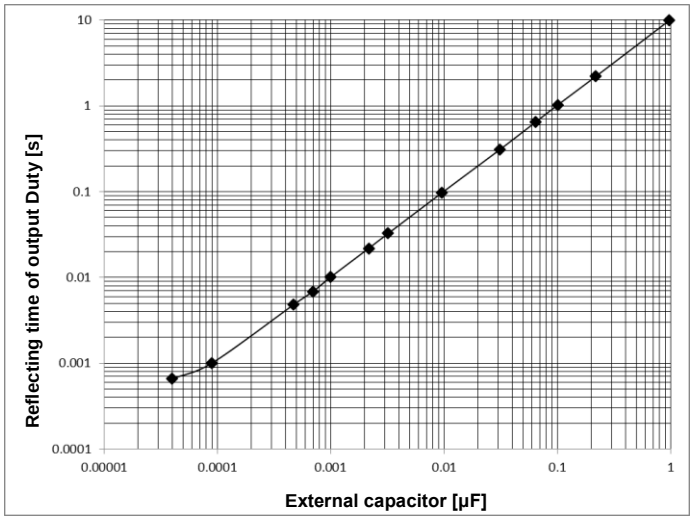


Figure 4 Relation of external capacitor and reflecting time of output duty

(7) Setting FG_OUT and LD_OUT terminals

It is an open-drain output. So, the voltage should be pulled-up by a resistor to either the external power supply or VREG terminal to output high level.
When pulling up to the VREG terminal, it is recommended to connect the resistor of 1 kΩ to 100 kΩ.
When pulling up to the external power supply, do not exceed absolute maximum rating.

(8) Setting TSP/VSP terminal

Please input signal of output PWM duty command. In controlling the analog voltage by setting SEL_SP terminal ”2”, connect the pull-down resistor between TSP/VSP terminal and SGND externally. It is recommended to connect the pull-down resistor of 10 kΩ to 100 kΩ.

(9) Setting TEST terminal

It is a terminal for shipping test of the IC. Be sure to set to a low level. It is recommended to connect TEST terminal to SGND. It incorporates the pull-down resistor of 100 kΩ. However, in setting it open, it is concerned that the terminal voltage rises rapidly influenced by board wirings. In setting it open unavoidably, please confirm that IC terminal voltage is 0.8 V or less.

(10) Setting TEST2 terminal

It is a terminal for shipping test of the IC. Be sure to set to a low level. It is recommended to connect TEST2 terminal to SGND. The state of TEST2 terminal is high impedance by inputting voltage to the comparator. The circuit operation is not influenced by the input voltage. In setting it open, it is concerned that the terminal voltage rises rapidly influenced by board wirings. In setting it open unavoidably, please confirm that IC terminal voltage is VREG+0.3 V or less.

(11) Setting CW/CCW terminal

Please connect this terminal to VREG terminal and SGND, or input the external control signal. In connecting to VREG terminal, the voltage becomes H level. In connecting to SGND, the voltage becomes L level. Please confirm the voltage of the IC terminal is 0.8 V or less in setting it open state unavoidably, though pull-down resistor of 50 kΩ is incorporated.

(12) Setting BRAKE terminal

Please connect this terminal to SGND, or input the external control signal. In connecting to SGND, the voltage becomes L level. Please confirm the voltage of the IC terminal is 0.8 V or less in setting it open state unavoidably, though pull-down resistor of 50 kΩ is incorporated.

(13) Setting FST, SEL_SP, and SEL_LA terminals

Please configure the voltage by resistive dividing voltage between VREG terminal and SGND, or connect these terminals to VREG terminal or GND terminal. In setting them open state, the function becomes middle level. So, please evaluate the IC on the actual board enough before setting them open state. It is recommended to connect the resistor of 10 kΩ to 100 kΩ between VREG terminal and SGND.

(14) Setting SEL_FG, MIN_SP, LA, FPWM, and SEL_LD terminals

Please configure the voltage by resistive dividing voltage between VREG terminal and SGND, or connect it to VREG terminal or GND terminal. It is recommended to connect the resistor of 10 kΩ to 100 kΩ between VREG terminal and SGND.

(15) Setting VST terminal

Please configure the voltage by resistive dividing voltage between VREG terminal and SGND. It is recommended to connect the resistor of 10 kΩ to 100 kΩ between VREG terminal and SGND.

(16) Setting MVM terminal

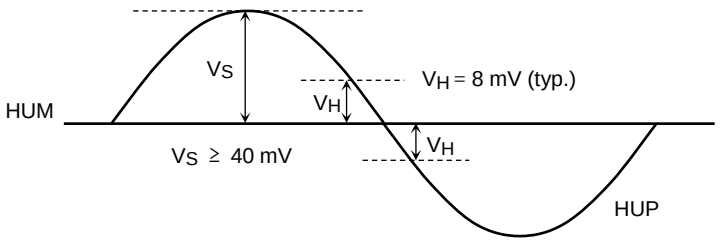
Please configure the voltage by resistive dividing voltage between VM terminal and SGND. It is recommended to connect the resistor of 10 kΩ to 100 kΩ between VREG terminal and SGND. When this function is not used, please connect it SGND terminal.

(17) HUP and HUM terminals

Please input hall signals to HUP and HUM terminals. Select hall elements or hall ICs to provide hall signals. Connect output terminals of U, V, and W, and the hall signal terminals of HUP and HUM, to the motor to have the relation shown in the timing chart of "4. Notes in using the motor".

<Notes in using the hall device>

- When 5 V of VREG supplies power to the hall element, add the limiting resistor to the power supply terminal of the hall element. This resistor avoids exceeding the maximum input current of the hall element.
- To recognize switching of the hall signal correctly, the amplitude of the hall device should be 40 mV or more and the input voltage range should be 0.5 V to 3.5 V.
- Hall amplifier has a hysteresis. When the amplitude of it is small, the phase gap of the switching timing becomes large. So, please make the amplitude of it as large as possible.
- When the capacitor for reducing the noise of the hall signal is attached, please arrange it close to HUP and HUM terminals. The recommended capacitor is 0.001 µF to 0.1 µF.

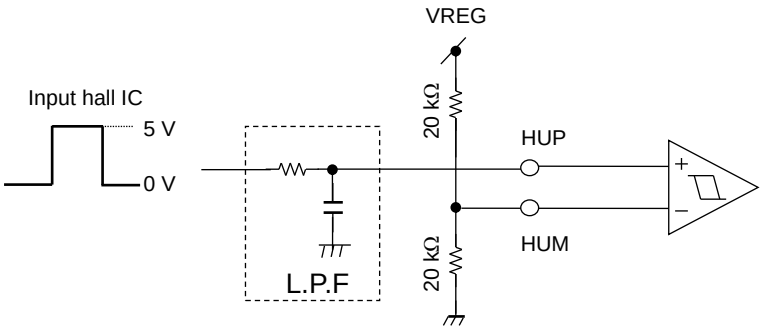


< Notes in using the hall IC>

Please configure HUP and HUM terminals as follows;

(1) HUP: Input voltage: H level = VREG, L level = SGND
HUM: Input voltage: VREG/2 * Configure it with resistive dividing voltage between VREG terminal and SGND.

(2) HUP: Input voltage: VREG/2 * Configure it with resistive dividing voltage between VREG terminal and SGND.
HUM: Input voltage: H level = VREG, L level = SGND



*: In case of V phase and W phase are also the same.

When the operation malfunctions because of the noise of the hall signal, please add the low-pass filter (LPF) for CR. Please add it between the hall IC and the input terminal externally. The standard of the constant number of this CR filter is described as follows. Its cut-off frequency (fcut) should be 100 times or more of the maximum frequency of the hall signal (Fhall).

Cut-off frequency: $fcut = 1/(2\pi CR)$ [Hz]

When maximum frequency of the hall signal (Fhall) = 1 kHz, $fcut > 100 \times Fhall$, and $CR < 1.59 \times 10^{-6}$.

Please confirm the operation by setting R to 1 kΩ and setting C to 1000 pF for example. Finally, determine the constant number of CR by considering the impedance of the output circuit of the hall IC.

(18) Connecting U, V, and W terminals

Connect output terminals of U, V, and W, and the hall signal terminals of HUP and HUM, to the motor to have the relation shown in the timing chart of "4. Notes in using the motor".

8. Notes in designing circuit board

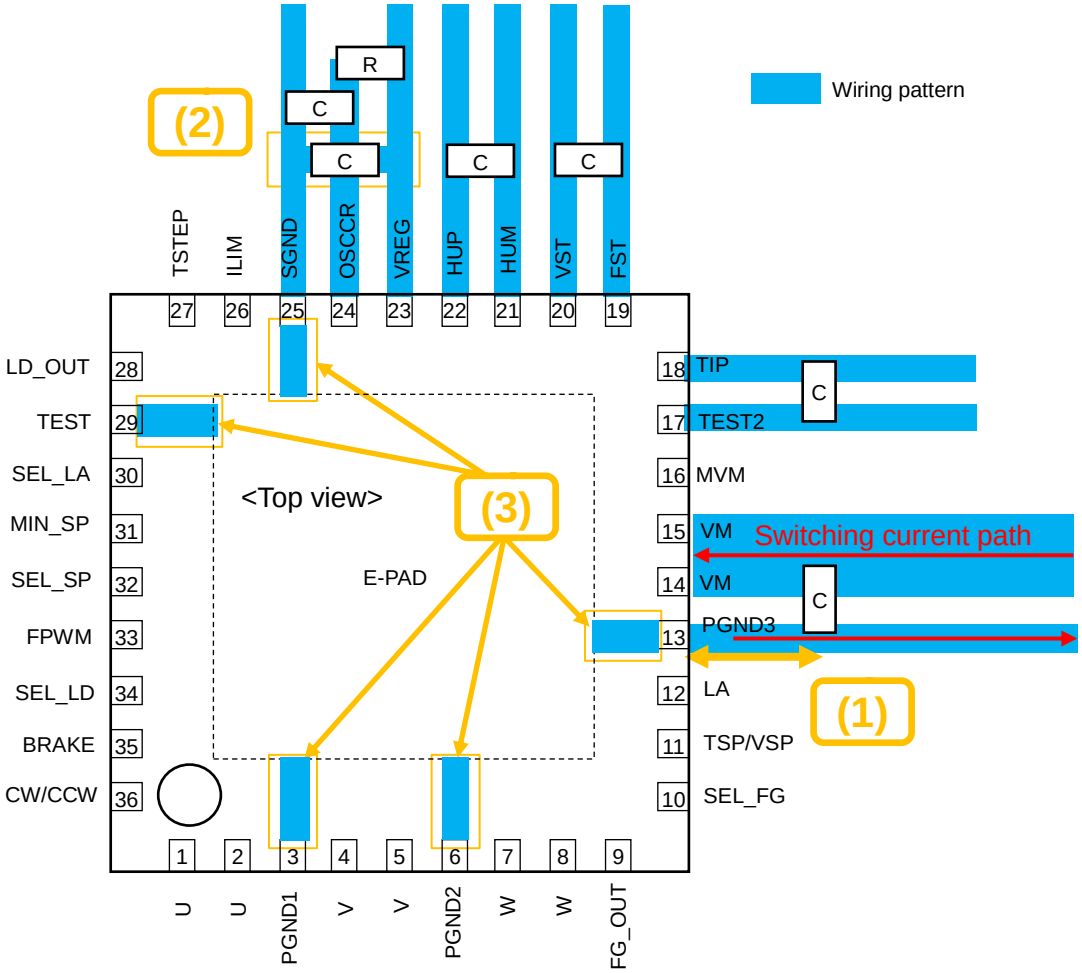
In designing board patterns of VM, SGND, PGND1, PGND2, and PGND3, please pay attention to following notes.

(1) Place the capacitor between VM and PGND3 close to the IC as possible.
Shorten the wiring length between this capacitor and the IC terminal as much as possible to make wiring impedance low.

(2) Place the capacitor between VREG and SGND close to the IC as possible.
In order to stabilize the VREG voltage, shorten the wiring length between this capacitor and the IC terminal as much as possible to make wiring impedance low. Especially, shorten the wiring length between the capacitor and SGND terminal to reduce the path for flowing the switching current.

(3) Short-circuit each terminal of PGND1, PGND2, PGND3, and SGND near the IC.
Please refer to the connection example shown below. Each terminal is connected to the back side of the IC (E-PAD).

<Board layout example: TC78B015AFTG>
Layout examples of VM, PGND1, PGND2, PGND3, SGND, VREG, OSCCR, HUP, HUM, VST, FST, TIP, TEST, and TEST2 terminals are shown to simplify the description.



<How to improve IC heat dissipation and reduce heat generation>

- Increase the number of thermal Via.
  Especially, the heat dissipation improves by arranging the thermal Via on the back side of the IC (E-PAD) and by increasing the number of thermal via.

- Enlarge the ratio of wiring cover of the board.
  When the ratio of wiring cover of the board is enlarged, the temperature gradient of the board surface is equalized and the heat dissipation improves.

- Decrease the output current of VREG terminal
  When the resistor configured by resistive dividing voltage between VREG and SGND is enlarged and the hall bias power supply is changed from VREG terminal to another power supply, the output current of VREG is decreased and the consumption current of the IC is suppressed. So, heat generation is reduced.

9. Land pattern dimensions (for reference only)

Unit: mm

P-WQFN36-0505-050-001

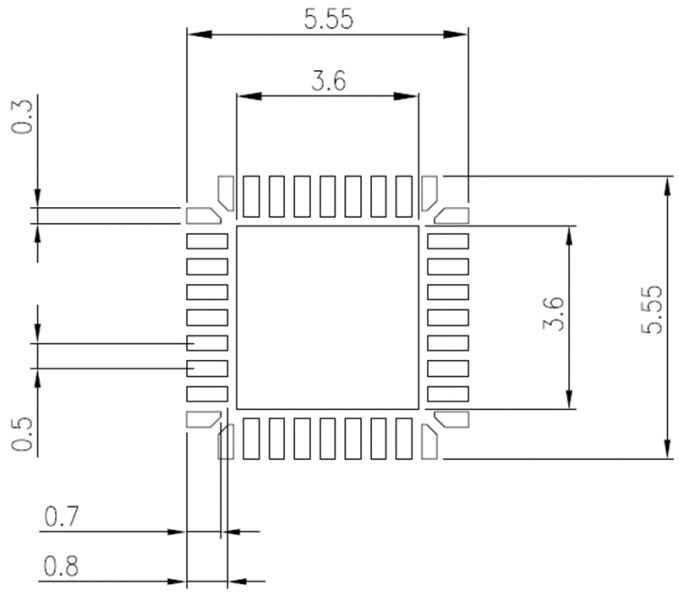


Figure 5 Land pattern dimensions: P-WQFN36-0505-050-001 (for reference only)

On the actual designing of the PCB, please consider below conditions enough and decide the optimum pattern.

- Solder bridge
- Solder joint strength
- Pattern accuracy when board is produced
- Heat radiation from lead consideration
- Installing accuracy of the machine equipped with IC

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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