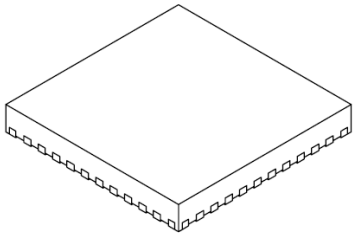
TOSHIBA BiCD Process Integrated Circuit Silicon Monolithic

TB62D787FTG

24-channel constant current LED driver with single wire

The TB62D787FTG is a constant current driver designed for LED illumination.
This product incorporates 7-bit PWM dimming controllers and 24-channel constant current drivers. 24-channel constant current circuits are divided into three blocks corresponding to LED luminescence colors, and each output current can be adjusted by the external resistors.
This product is controlled using only single DATA-IN input signal. It can be configured up to 64 recognition addresses with the ID setting pin.
This product includes a linear regulator (7.0 to 28 V) function, which shares with the power supply of LEDs.
Additionally, data can be transferred at high speed with BiCD process.

TB62D787FTG



P-VQFN40-0606-0.50-001
Weight: 0.097g (typ.)

Feature

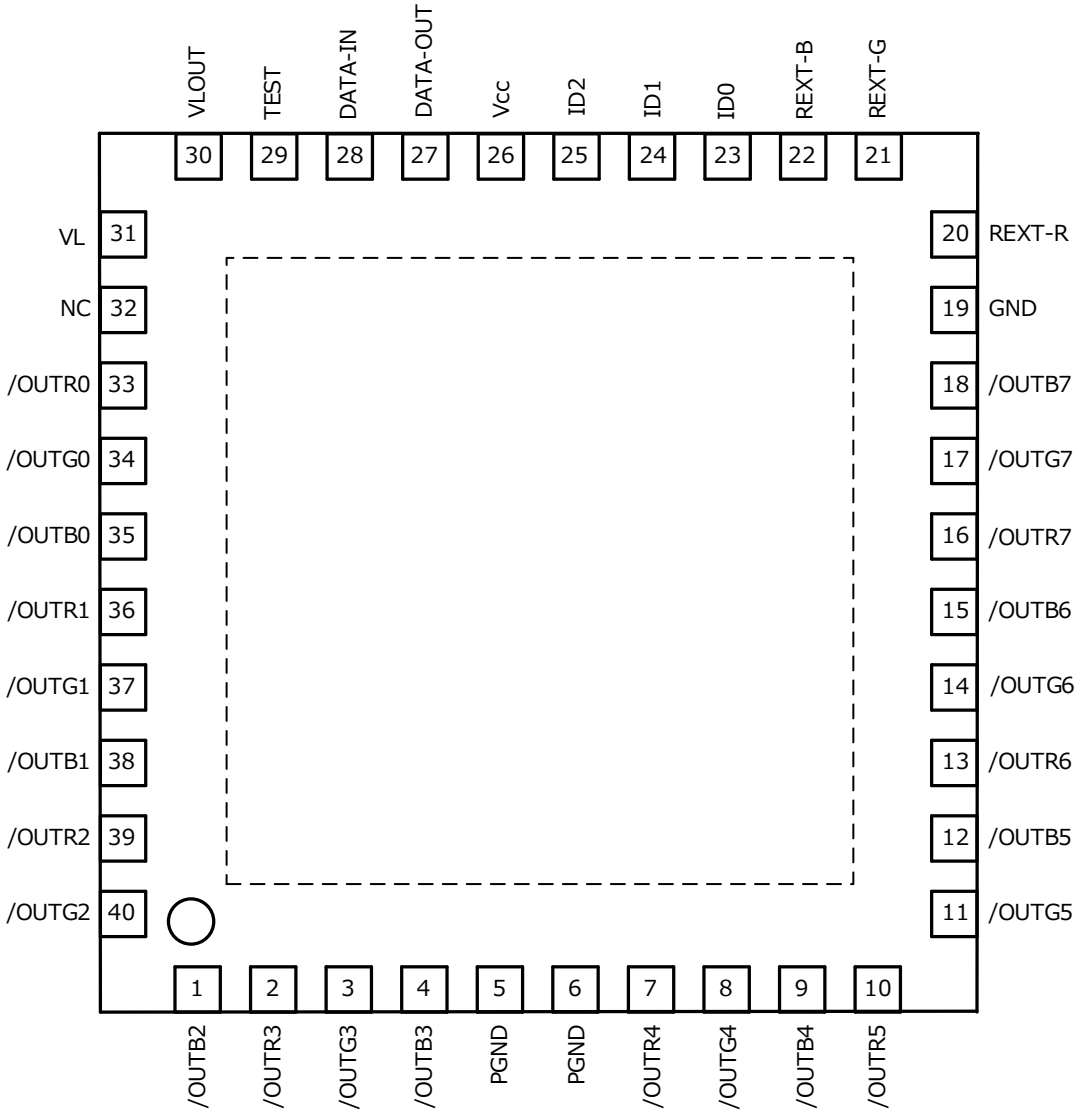
- Power supply voltage: VL = 7.0 to 28 V (The case used by sharing with a power supply of LED)
  Vcc = 5.0 V ±10% (The case that the power supply of LED and that of this IC separately.)
- Output withstand voltage: 28 V (max)
- Output current capability: 85 mA (max) × 24 channels
- Constant current output range: 5 to 40 mA × 24 channels
- Output voltage at constant-current drive: 0.5 V (min, constant current 5 to 40 mA)
- Designed for common-anode LEDs.
- The input interface is controlled by DATA-IN (single wire)
- Logical input signal voltage level: 5 V CMOS Interface
- PWM control circuit included: 7-bit PWM
- Driver identification: Up to 64 driver ICs can be controlled individually
- Thermal shut down (TSD) included.
- Operating temperature range: Topr = -40 to 85°C
- Package: P-VQFN40-0606-0.50-001

- Constant current accuracy

Condition	Constant-current accuracy between channels	Constant-current accuracy between ICs
Output voltage: 0.5 V Output current: 15 mA	±3.0%	±6.0%

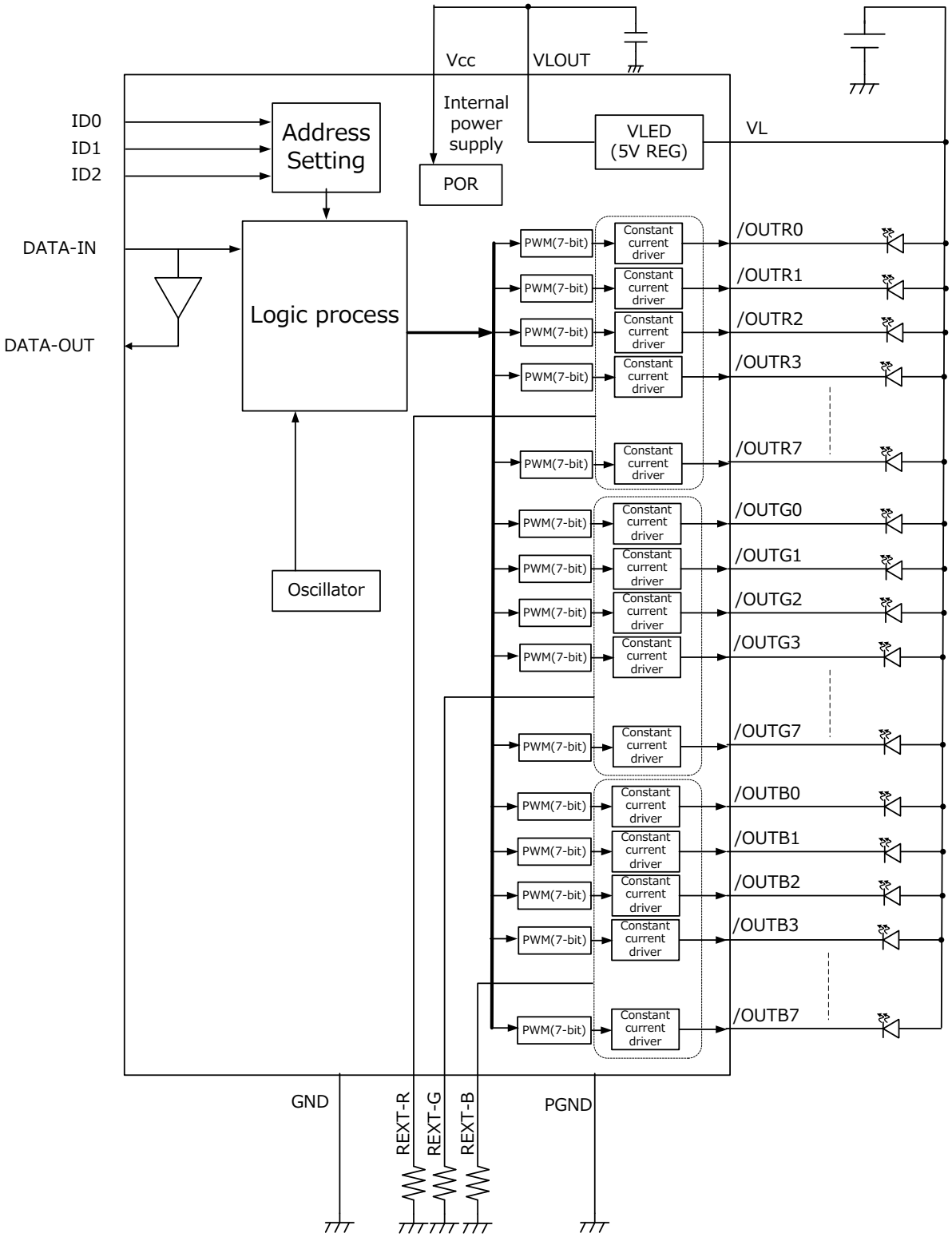
This product is very delicate because of elements of MOS structure. In handling, please take care of measures of static electricity, such as use of a ground band or an electric conduction mat, removal of static electricity by an ionizer, and management of temperature and humidity.

Pin Assignment (top view)



Please be sure to connect the back radiation PAD of a QFN package to GND of a substrate.

Block Diagram



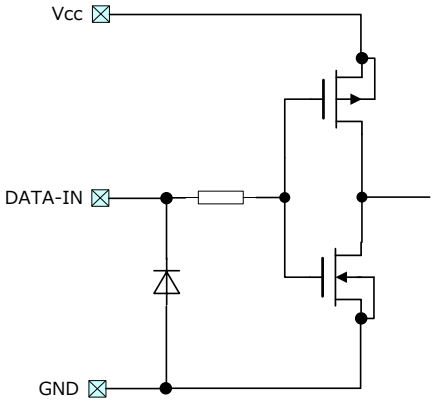
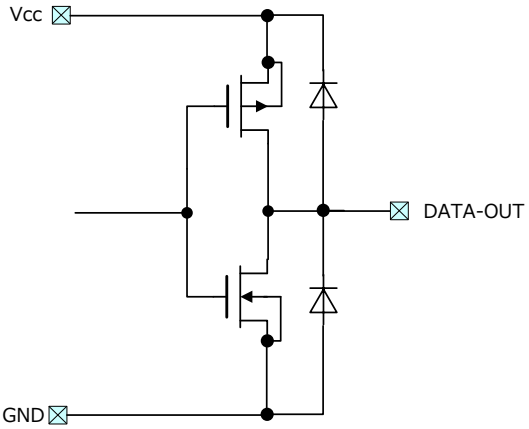
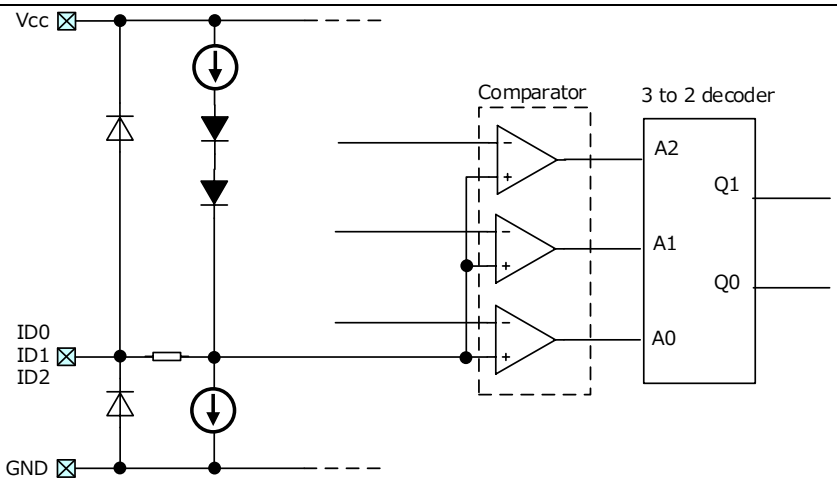
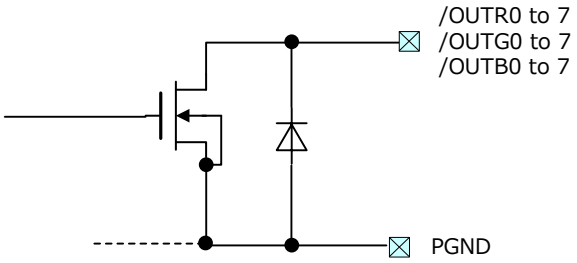
Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Pin Description

Pin No.	Pin name	Function description
33	/OUTR0	Constant current output pin. (Open-drain type)
34	/OUTG0	Constant current output pin. (Open-drain type)
35	/OUTB0	Constant current output pin. (Open-drain type)
36	/OUTR1	Constant current output pin. (Open-drain type)
37	/OUTG1	Constant current output pin. (Open-drain type)
38	/OUTB1	Constant current output pin. (Open-drain type)
39	/OUTR2	Constant current output pin. (Open-drain type)
40	/OUTG2	Constant current output pin. (Open-drain type)
1	/OUTB2	Constant current output pin. (Open-drain type)
2	/OUTR3	Constant current output pin. (Open-drain type)
3	/OUTG3	Constant current output pin. (Open-drain type)
4	/OUTB3	Constant current output pin. (Open-drain type)
7	/OUTR4	Constant current output pin. (Open-drain type)
8	/OUTG4	Constant current output pin. (Open-drain type)
9	/OUTB4	Constant current output pin. (Open-drain type)
10	/OUTR5	Constant current output pin. (Open-drain type)
11	/OUTG5	Constant current output pin. (Open-drain type)
12	/OUTB5	Constant current output pin. (Open-drain type)
13	/OUTR6	Constant current output pin. (Open-drain type)
14	/OUTG6	Constant current output pin. (Open-drain type)
15	/OUTB6	Constant current output pin. (Open-drain type)
16	/OUTR7	Constant current output pin. (Open-drain type)
17	/OUTG7	Constant current output pin. (Open-drain type)
18	/OUTB7	Constant current output pin. (Open-drain type)
5,6	PGND	Power ground pin. It should be connected to 19 pin (GND) externally.
20	REXT-R	External resistor pin for output current configuration (/OUTR0 to 7)
21	REXT-G	External resistor pin for output current configuration (/OUTG0 to 7)
22	REXT-B	External resistor pin for output current configuration (/OUTB0 to 7)
19	GND	Ground pin
23	ID0	ID setting pin
24	ID1	ID setting pin
25	ID2	ID setting pin
26	Vcc	5 V of supply voltage input pin
27	DATA-OUT	Serial data output pin (Buffer output of DATA-IN input signal)
28	DATA-IN	Serial data input pin
29	TEST	The pin for vendor use. Please connect surely to GND in normal operation because it does not operate normally in high level or open process.
30	VLOUT	5 V Regulator output pin. Please connect this pin and Vcc pin directly when internal power supply is used. In case the Vcc voltage is applied from external power supply, please connect VL pin to GND pin.
31	VL	Power supply input pin in the case of sharing a power supply of LED and the power supply of this product.
32	NC	Connect to GND in normal operation.

Note: Please pay attention to short circuiting between adjacent pins when pin 29 is connected to GND.

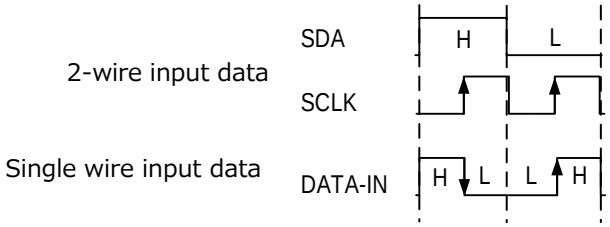
Equivalent circuit for inputs and outputs

Pin name	Equivalent circuit
DATA-IN	
DATA-OUT	
ID0 to 2	
/OUTR0 to 7 /OUTG0 to 7 /OUTB0 to 7	

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Programming the TB62D787FTG

This product performs the control with single wire data signal. As compared with 2-wire data signal synchronous with the clock signal in conventional products, this product assigns each data state to the transition state (H to L or L to H) as shown below.



(1) Data setting format

Each command setting input to DATA-IN is set with the following format.

This product recognizes the communication frequency (rising interval of input data) by taking in the start command (the start condition of data input).

Start command: 1010101010101010=0xAA,0xAA (original binary: 11111111)

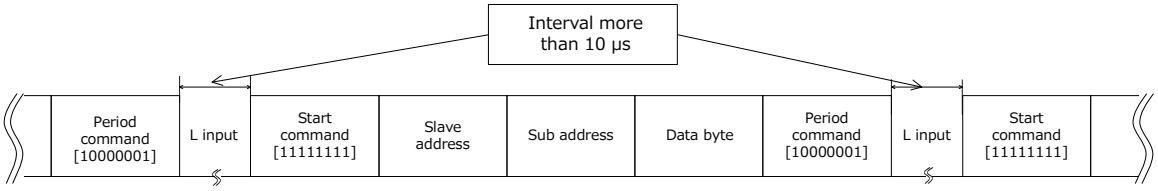
Since this product continues to recognize the signal interval which recognizes at the start command until the period command, input the pulse width in 1 bit within 50% duty so that the period is not collapsed until completion of the period command.

Period command: 1001010101010110=0x95,0x56 (original binary: 10000001)

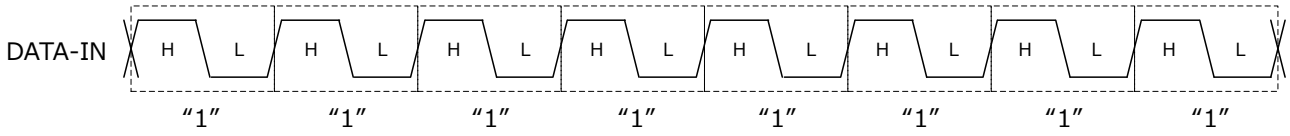
After the completion of the period command input, make sure to set the interval ("L") more than 10 μs until next start command input.

<Input format>

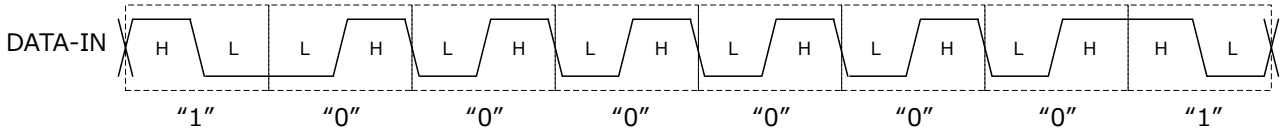
Example) Basic input mode



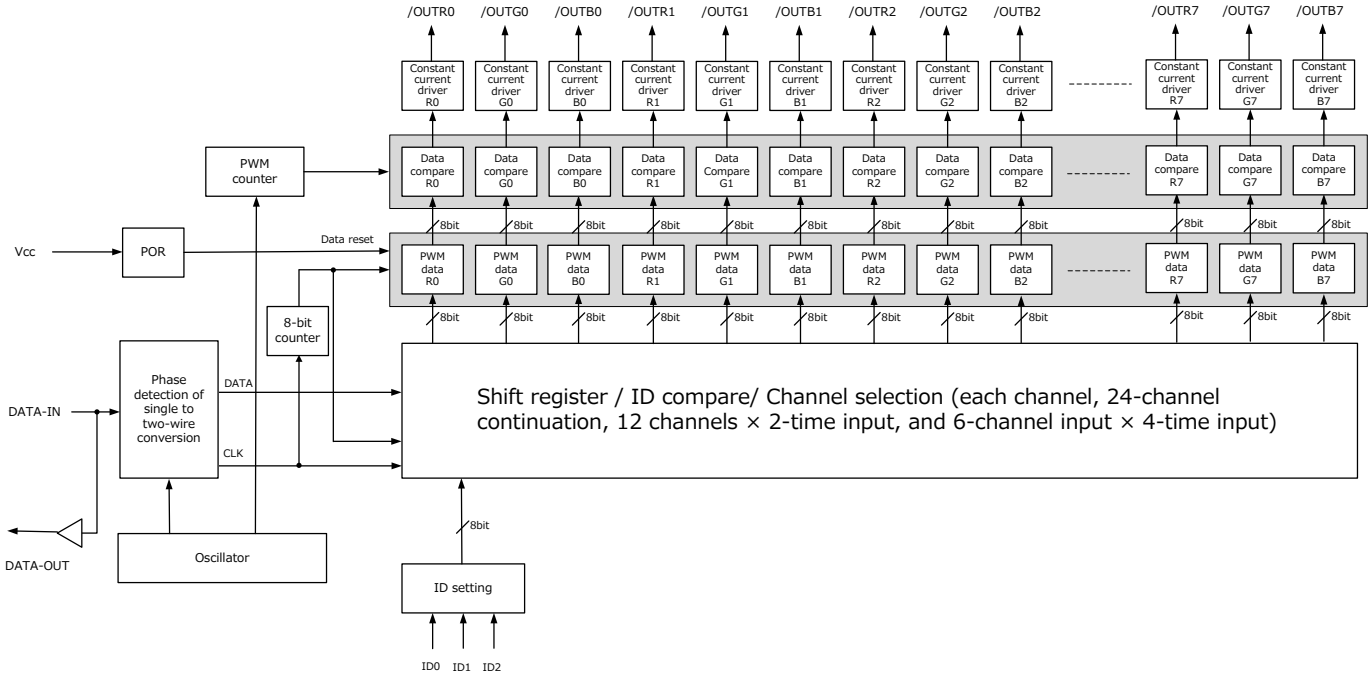
Example 1) Start command 0xAA and 0xAA setting (original binary 11111111)



Example 2) Period command setting 0x95 and 0x56 (original binary 10000001)



<Block diagram of data setting block>



(2) Normal programming mode

Normal programming mode should be set as the following flow.

Start command -> Slave address -> Sub-address -> Data byte -> Period command

Slave address: ID setting of the chip, Sub-address: Output channel setting, Data byte: Data for PWM setting

For each setting data, refer to the descriptions later.

Interval ("L" more than 10 μs)	Start Command	Slave Address	Sub-address (channel select)	Data byte (PWM configuration)	Period Command	Interval ("L" more than 10 μs)

(3) Special programming mode

This is how to set when all channels are set individually.

●Special mode setting (In case that all channels are selected in order))

When the special mode is set to the sub-address, the illumination data of all channels can be set.

Special mode setting: 0110100101010101=0x69 and 0x55 (original binary: 01100000)

If it returns to Normal programming mode, input the start command (ALL "H" 8 bits). When this mode setting is used, the quantity of the data to be set can be reduced.

Interval ("L" more than 10 μs)	Start command	Slave Address	Sub-address (Special mode setting)	Data OUTR0	Data OUTG0	Data OUTB0	Data OUTR1	Data OUTG1	Data OUTB1

Data OUTR2	Data OUTG2	Data OUTB2	Data OUTR3	Data OUTG3	Data OUTB3	Data OUTR4	Data OUTG4	Data OUTB4	Data OUTR5	Data OUTG5	Data OUTB5

Data OUTR6	Data OUTG6	Data OUTB6	Data OUTR7	Data OUTG7	Data OUTB7	Period command

Please set 24-channel data surely. (In case the data (more than 24 channels) provided the 25th and subsequent data are treated as invalid.)

(4) Dividing programming mode

a) 12-channel programming mode (12ch+12ch=24ch)

If 12-channel mode is set to sub-address, illumination data can be set in the range.

12-channel programming mode (1/2): 0110100101011001=0x69 and 0x59 (original binary: 01100010)

12-channel programming mode (2/2): 0110100101100101=0x69 and 0x65 (original binary: 01100100)

Interval ("L" more than 10 μs)	Start command	Slave address	Sub-address (12ch programming 1/2) (12ch programming 2/2)	Data OUTR0 OUTR4	Data OUTG0 OUTG4	Data OUTB0 OUTB4	Data OUTR1 OUTR5	Data OUTG1 OUTG5	Data OUTB1 OUTB5

Data OUTR2 OUTR6	Data OUTG2 OUTG6	Data OUTB2 OUTB6	Data OUTR3 OUTR7	Data OUTG3 OUTG7	Data OUTB3 OUTB7	Period command

b) 6-channel programming mode (6ch+6ch+6ch+6ch=24ch)

If 6-channel mode is set to sub-address, illumination data can be set in the range.

6-channel programming mode (1/4): 0110100101101001=0x69 and 0x69 (original binary: 01100110)

6-channel programming mode (2/4): 0110100110010101=0x69 and 0x95 (original binary: 01101000)

6-channel programming mode (3/4): 0110100110011001=0x69 and 0x99 (original binary: 01101010)

6-channel programming mode (4/4): 0110100110100101=0x69 and 0xA5 (original binary: 01101100)

Interval ("L" more than 10 μs)	Start command	Slave address	Sub-address (6ch programming 1/4) (6ch programming 2/4) (6ch programming 3/4) (6ch programming 4/4)	Data OUTR0 OUTR2 OUTR4 OUTR6	Data OUTG0 OUTG2 OUTG4 OUTG6	Data OUTB0 OUTB2 OUTB4 OUTB6	Data OUTR1 OUTR3 OUTR5 OUTR7	Data OUTG1 OUTG3 OUTG5 OUTG7	Data OUTB1 OUTB3 OUTR5 OUTB7	Period command

(5) Data settings

The start command at the beginning and the period command at the end are shown in the following table.

The slave address, sub-address, and PWM data byte shown below are input to between the start command and period command.

	Original binary	Single wire input	Hexadecimal	Decimal
Start	11111111	1010101010101010	0xAA,0xAA	170,170

	Original binary	Single wire input	Hexadecimal	Decimal
Period	10000001	1001010101010110	0x95,0x56	149,86

a) Slave address

Input voltages and logic states of the ID0, ID1, and ID2 pins are determined as follows.

*: Please set it as a pin for one of REXT-R, -G, and -B.

ID	Slave address				ID setting		
	Original binary	Single wire input	Hexadecimal	Decimal	ID2	ID1	ID0
0	00000000	0101010101010101	0x55,0x55	85,85	GND	GND	GND
1	00000010	0101010101011001	0x55,0x59	85,89	GND	GND	REXT-R/G/B*
2	00000100	0101010101100101	0x55,0x65	85,101	GND	GND	Open
3	00000110	0101010101101001	0x55,0x69	85,105	GND	GND	Vcc
4	00001000	0101010110010101	0x55,0x95	85,149	GND	REXT-R/G/B*	GND
5	00001010	0101010110011001	0x55,0x99	85,153	GND	REXT-R/G/B*	REXT-R/G/B*
6	00001100	0101010110100101	0x55,0xA5	85,165	GND	REXT-R/G/B*	Open
7	00001110	0101010110101001	0x55,0xA9	85,169	GND	REXT-R/G/B*	Vcc
8	00010000	0101011001010101	0x56,0x55	86,85	GND	Open	GND
9	00010010	0101011001011001	0x56,0x59	86,89	GND	Open	REXT-R/G/B*
10	00010100	0101011001100101	0x56,0x65	86,101	GND	Open	Open
11	00010110	0101011001101001	0x56,0x69	86,105	GND	Open	Vcc

a) Slave address (continues) **: The original binary number of all the selections is defined as x = 0.

ID	Slave address				ID setting		
	Original binary	Single wire input	Hexadecimal	Decimal	ID2	ID1	ID0
12	00011000	0101011010010101	0x56,0x95	86,149	GND	Vcc	GND
13	00011010	0101011010011001	0x56,0x99	86,153	GND	Vcc	REXT-R/G/B*
14	00011100	0101011010100101	0x56,0xA5	86,165	GND	Vcc	Open
15	00011110	0101011010101001	0x56,0xA9	86,169	GND	Vcc	Vcc
16	00100000	0101100101010101	0x59,0x55	89,85	REXT-R/G/B*	GND	GND
17	00100010	0101100101011001	0x59,0x59	89,89	REXT-R/G/B*	GND	REXT-R/G/B*
18	00100100	0101100101100101	0x59,0x65	89,101	REXT-R/G/B*	GND	Open
19	00100110	0101100101101001	0x59,0x69	89,105	REXT-R/G/B*	GND	Vcc
20	00101000	0101100110010101	0x59,0x95	89,149	REXT-R/G/B*	REXT-R/G/B*	GND
21	00101010	0101100110011001	0x59,0x99	89,153	REXT-R/G/B*	REXT-R/G/B*	REXT-R/G/B*
22	00101100	0101100110100101	0x59,0xA5	89,165	REXT-R/G/B*	REXT-R/G/B*	Open
23	00101110	0101100110101001	0x59,0xA9	89,169	REXT-R/G/B*	REXT-R/G/B*	Vcc
24	00110000	0101101001010101	0x5A,0x55	90,85	REXT-R/G/B*	Open	GND
25	00110010	0101101001011001	0x5A,0x59	90,89	REXT-R/G/B*	Open	REXT-R/G/B*
26	00110100	0101101001100101	0x5A,0x65	90,101	REXT-R/G/B*	Open	Open
27	00110110	0101101001101001	0x5A,0x69	90,105	REXT-R/G/B*	Open	Vcc
28	00111000	0101101010010101	0x5A,0x95	90,149	REXT-R/G/B*	Vcc	GND
29	00111010	0101101010011001	0x5A,0x99	90,153	REXT-R/G/B*	Vcc	REXT-R/G/B*
30	00111100	0101101010100101	0x5A,0xA5	90,165	REXT-R/G/B*	Vcc	Open
31	00111110	0101101010101001	0x5A,0xA9	90,169	REXT-R/G/B*	Vcc	Vcc
32	01000000	0110010101010101	0x65,0x55	101,85	Open	GND	GND
33	01000010	0110010101011001	0x65,0x59	101,89	Open	GND	REXT-R/G/B*
34	01000100	0110010101100101	0x65,0x65	101,101	Open	GND	Open
35	01000110	0110010101101001	0x65,0x69	101,105	Open	GND	Vcc
36	01001000	0110010110010101	0x65,0x95	101,149	Open	REXT-R/G/B*	GND
37	01001010	0110010110011001	0x65,0x99	101,153	Open	REXT-R/G/B*	REXT-R/G/B*
38	01001100	0110010110100101	0x65,0xA5	101,165	Open	REXT-R/G/B*	Open
39	01001110	0110010110101001	0x65,0xA9	101,169	Open	REXT-R/G/B*	Vcc
40	01010000	0110011001010101	0x66,0x55	102,85	Open	Open	GND
41	01010010	0110011001011001	0x66,0x59	102,89	Open	Open	REXT-R/G/B*
42	01010100	0110011001100101	0x66,0x65	102,101	Open	Open	Open
43	01010110	0110011001101001	0x66,0x69	102,105	Open	Open	Vcc
44	01011000	0110011010010101	0x66,0x95	102,149	Open	Vcc	GND
45	01011010	0110011010011001	0x66,0x99	102,153	Open	Vcc	REXT-R/G/B*
46	01011100	0110011010100101	0x66,0xA5	102,165	Open	Vcc	Open
47	01011110	0110011010101001	0x66,0xA9	102,169	Open	Vcc	Vcc
48	01100000	0110100101010101	0x69,0x55	105,85	Vcc	GND	GND
49	01100010	0110100101011001	0x69,0x59	105,89	Vcc	GND	REXT-R/G/B*
50	01100100	0110100101100101	0x69,0x65	105,101	Vcc	GND	Open
51	01100110	0110100101101001	0x69,0x69	105,105	Vcc	GND	Vcc
52	01101000	0110100110010101	0x69,0x95	105,149	Vcc	REXT-R/G/B*	GND
53	01101010	0110100110011001	0x69,0x99	105,153	Vcc	REXT-R/G/B*	REXT-R/G/B*
54	01101100	0110100110100101	0x69,0xA5	105,165	Vcc	REXT-R/G/B*	Open
55	01101110	0110100110101001	0x69,0xA9	105,169	Vcc	REXT-R/G/B*	Vcc
56	01110000	0110101001010101	0x6A,0x55	106,85	Vcc	Open	GND
57	01110010	0110101001011001	0x6A,0x59	106,89	Vcc	Open	REXT-R/G/B*
58	01110100	0110101001100101	0x6A,0x65	106,101	Vcc	Open	Open
59	01110110	0110101001101001	0x6A,0x69	106,105	Vcc	Open	Vcc
60	01111000	0110101010010101	0x6A,0x95	106,149	Vcc	Vcc	GND
61	01111010	0110101010011001	0x6A,0x99	106,153	Vcc	Vcc	REXT-R/G/B*
62	01111100	0110101010100101	0x6A,0xA5	106,165	Vcc	Vcc	Open
63	01111110	0110101010101001	0x6A,0xA9	106,169	Vcc	Vcc	Vcc
**	0XXXXXX1	0101010101010110	0x55,0x56	85,86	All select		

b) Sub-address Output channels, all channels selection, special programming mode, 6-channel programming mode, or 12-channel programming mode can be set.

Sub-address				LED output	Target setting of PWM data
Original binary	Single wire input	Hexadecimal	Decimal		
00000010	0101010101011001	0x55,0x59	85,89	/OUTR0	One channel is set separately.
00000100	0101010101100101	0x55,0x65	85,101	/OUTG0	
00000110	0101010101101001	0x55,0x69	85,105	/OUTB0	
00001000	0101010110010101	0x55,0x95	85,149	/OUTR1	
00001010	0101010110011001	0x55,0x99	85,153	/OUTG1	
00001100	0101010110100101	0x55,0xA5	85,165	/OUTB1	
00001110	0101010110101001	0x55,0xA9	85,169	/OUTR2	
00010000	0101011001010101	0x56,0x55	86,85	/OUTG2	
00010010	0101011001011001	0x56,0x59	86,89	/OUTB2	
00010100	0101011001100101	0x56,0x65	86,101	/OUTR3	
00010110	0101011001101001	0x56,0x69	86,105	/OUTG3	
00011000	0101011010010101	0x56,0x95	86,149	/OUTB3	
00011010	0101011010011001	0x56,0x99	86,153	/OUTR4	
00011100	0101011010100101	0x56,0xA5	86,165	/OUTG4	
00011110	0101011010101001	0x56,0xA9	86,169	/OUTB4	
00100000	0101100101010101	0x59,0x55	89,85	/OUTR5	
00100010	0101100101011001	0x59,0x59	89,89	/OUTG5	
00100100	0101100101100101	0x59,0x65	89,101	/OUTB5	
00100110	0101100101101001	0x59,0x69	89,105	/OUTR6	
00101000	0101100110010101	0x59,0x95	89,149	/OUTG6	
00101010	0101100110011001	0x59,0x99	89,153	/OUTB6	
00101100	0101100110100101	0x59,0xA5	89,165	/OUTR7	
00101110	0101100110101001	0x59,0xA9	89,169	/OUTG7	
00110000	0101101001010101	0x5A,0x55	90,85	/OUTB7	
01000000	0110010101010101	0x65,0x55	101,85	All channel select	All 24 channels are set as same.
01100000	0110100101010101	0x69,0x55	105,85	Special programming mode	24 channels are set at one time.
01100010	0110100101011001	0x69,0x59	105,89	12-channel programming mode (1/2)	12 channels are set at two times.
01100100	0110100101100101	0x69,0x65	105,101	12-channel programming mode (2/2)	
01100110	0110100101101001	0x69,0x69	105,105	6-channel programming mode (1/4)	6 channels are set at four times.
01101000	0110100110010101	0x69,0x95	105,149	6-channel programming mode (2/4)	
01101010	0110100110011001	0x69,0x99	105,153	6-channel programming mode (3/4)	
01101100	0110100110100101	0x69,0xA5	105,165	6-channel programming mode (4/4)	

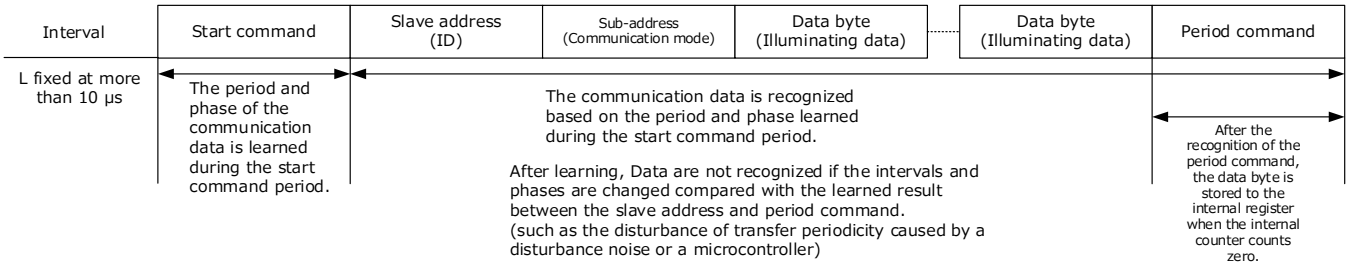
c) Data byte Data bytes set PWM dimming data.

PWM data byte				PWM dimming	Note
Original binary	Single wire input	Hexadecimal	Decimal		
00000000	0101010101010101	0x55,0x55	85,85	0/127	The initial state is set to 0/127 and is always OFF state. As the original binary, set "0" to LSB, and do not set "1." 127/127 is always ON state.
00000010	0101010101011001	0x55,0x59	85,89	1/127	
00000100	0101010101100101	0x55,0x65	85,101	2/127	
00000110	0101010101101001	0x55,0x69	85,105	3/127	
00001000	0101010110010101	0x55,0x95	85,149	4/127	
00001010	0101010110011001	0x55,0x99	85,153	5/127	
00001100	0101010110100101	0x55,0xA5	85,165	6/127	
00001110	0101010110101001	0x55,0xA9	85,169	7/127	
00010000	0101011001010101	0x56,0x55	86,85	8/127	
to	to	—	—	to	
00011110	0101011010101001	0x56,0xA9	86,169	15/127	
00100000	0101100101010101	0x59,0x55	89,85	16/127	
to	to	—	—	to	
00101110	0101100110101001	0x59,0xA9	89,169	23/127	
00110000	0101101001010101	0x5A,0x55	90,85	24/127	
to	to	—	—	to	
00111110	0101101010101001	0x5A,0xA9	90,169	31/127	
01000000	0110010101010101	0x65,0x55	101,85	32/127	
to	to	—	—	to	
01001110	0110010110101001	0x65,0xA9	101,169	39/127	
01010000	0110011001010101	0x66,0x55	102,85	40/127	
to	to	—	—	to	
01011110	0110011010101001	0x66,0xA9	102,169	47/127	
01100000	0110100101010101	0x69,0x55	105,85	48/127	
to	to	—	—	to	
01101110	0110100110101001	0x69,0xA9	105,169	55/127	
01110000	0110101001010101	0x6A,0x55	106,85	56/127	
to	to	—	—	to	
01111110	0110101010101001	0x6A,0xA9	106,169	63/127	
10000000	1001010101010101	0x95,0x55	149,85	64/127	
to	to	—	—	to	
10001110	1001010110101001	0x95,0xa9	149,169	71/127	
10010000	1001011001010101	0x96,0x55	150,85	72/127	
to	to	—	—	to	
10011110	1001011010101001	0x96,0xa9	150,169	79/127	
10100000	1001100101010101	0x99,0x55	153,85	80/127	
to	to	—	—	to	
10101110	1001100110101001	0x99,0xa9	153,169	87/127	
10110000	1001101001010101	0x9a,0x55	154,85	88/127	
to	to	—	—	to	
10111110	1001101010101001	0x9a,0xa9	154,169	95/127	
11000000	1010010101010101	0xa5,0x55	165,85	96/127	
to	to	—	—	to	
11001110	1010010110101001	0xa5,0xa9	165,169	103/127	
11010000	1010011001010101	0xa6,0x55	166,85	104/127	
to	to	—	—	to	
11011110	1010011010101001	0xa6,0xa9	166,169	111/127	
11100000	1010100101010101	0xa9,0x55	169,85	112/127	
to	to	—	—	to	
11101110	1010100110101001	0xa9,0xa9	169,169	119/127	
11110000	1010101001010101	0xaa,0x55	170,85	120/127	
to	to	—	—	to	
11111110	1010101010101001	0xAA,0xA9	170,169	127/127	

(6) Notes of data setting

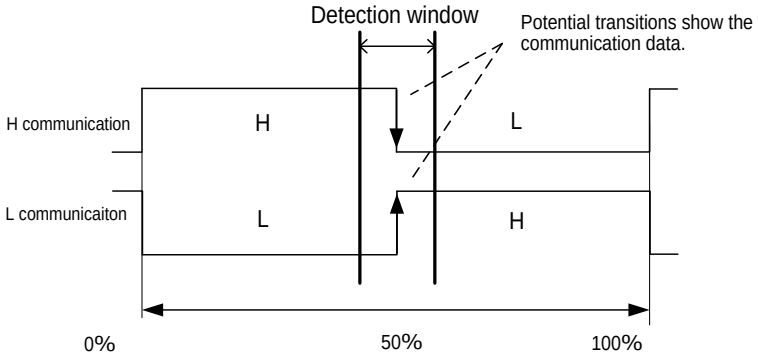
This product has the specification of data recognition or processing with only a data signal (asynchronous input signal). The data period (communication speed) is learned with the start command (data input start condition). Data are recognized according to this learning period, and are stored to the internal register after the period command (a condition of data input completion). Therefore, the data are not recognized if the data period is collapsed between the start command and the period command (see the following a)). Then the period learned during an interval period is reset and it waits for next communication.

a) Learning data period



b) Data recognition

The data input of this product makes data 2 bits (H, and L, or L and H) on the basis of a Manchester code, and transitions of the potential in a detection window show logic. Including jitter, communication delay and others, data are received by potential transitions in the detection window.



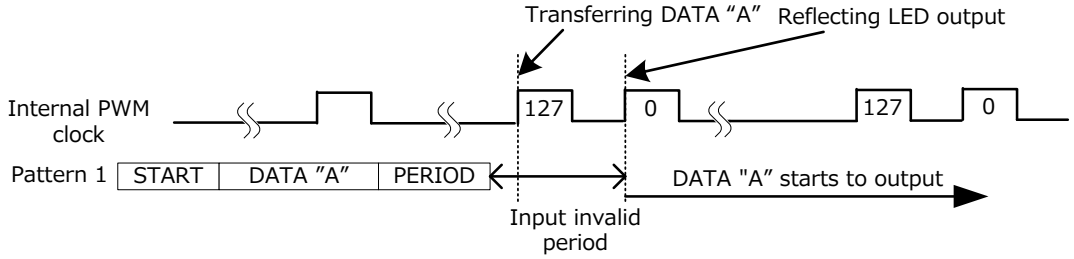
<Reference: Example of control data input>

(7) Example of basic data input to the same ID

When data are input to the same ID, next data should be input at the interval of 3 ms or more (128 times of internal PWM clocks) regardless of same or change of sub-address at last input. If the setting to the same channel is overlapped, PWM control cannot perform correctly.
If data is input to other slave address, it is not necessary.

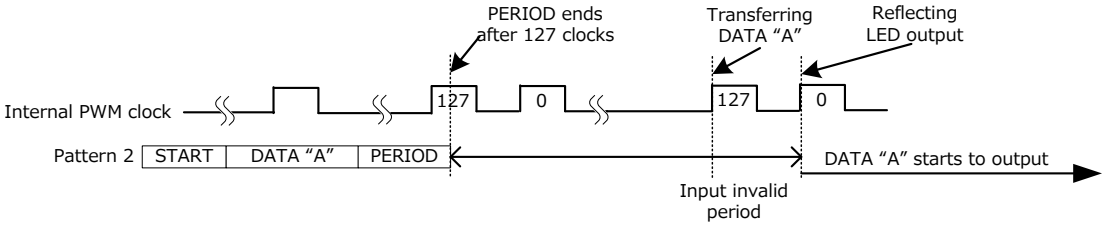
The following from a) to e) corresponds to them if a sub-address is in each output channel, all channels select or special programming mode.
Refer to f) to g) if a sub-address is in 6-channel programming mode or 12-channel programming mode.

a) In case DATA "A" is input up to the rising edge of 127 internal PWM clocks.



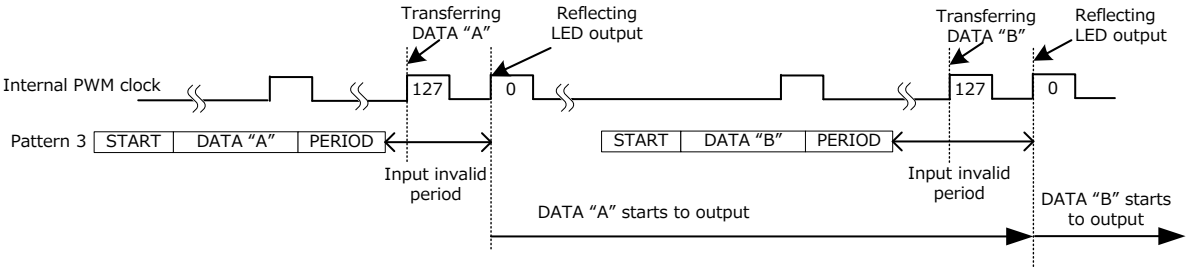
Output DATA "A" starts at the rising edge of zero internal PWM clocks.
Inputting is invalid from the rising edge of 127 internal PWM clocks to the rising edge of zero internal PWM clocks which are just after these 127 PWM clocks.

b) In case DATA "A" is input after the rising edge of 127 internal PWM clocks.



DATA "A" cannot be transferred at the rising edge of 127 internal PWM clocks just after inputting DATA "A." Therefore, DATA "A" starts an output at the rising edge of zero PWM clocks, after passing the rising edge of next 127 internal PWM clocks.
The input invalid period is the period to the rising edge of internal PWM clock 0 of which DATA "A" starts to output.

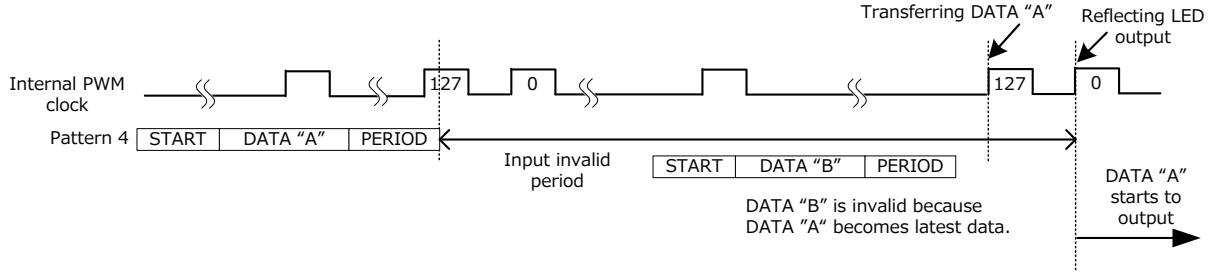
c) In case DATA "B" is input after starting the output of pattern 1



DATA "A" starts an output at the rising edge of zero internal PWM clocks just after DATA "A" period command. Then DATA "B" starts an output at rising edge of zero internal PWM clocks just after DATA "B" period command. The input invalid period is the period from the rising edge of 127 internal PWM clocks just after the period command input to the rising edge of zero internal PWM clocks.

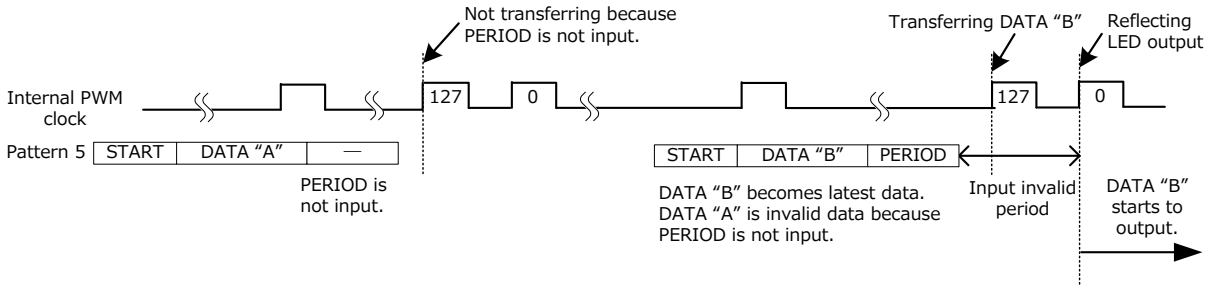
Pay attention that the IC does not operate according to the configuration while the following patterns (patterns 4 and 5) are input.

d) In case DATA "B" is input before DATA "A" starts output



After the period command of DATA “A”, the period is the input invalid period until the second rising edge of zero internal PWM clocks. Therefore, DATA "B" is invalid and DATA "A" is output.

e) In case the period command of DATA "A" is not recognized

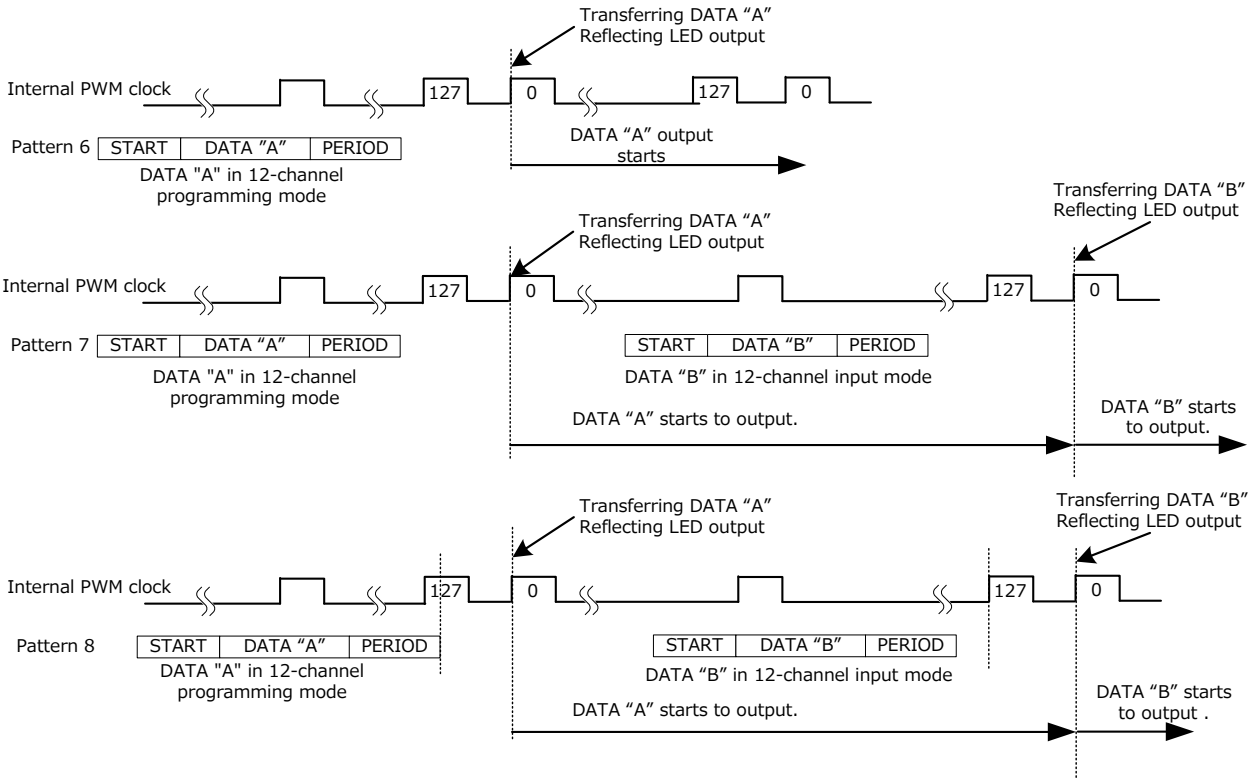


When the period command of DATA "A" is not input and the period command of next DATA "B" is input, DATA "B" starts output immediately after at the rising edge of zero internal PWM clocks.

f) 6-channel programming mode / 12-channel programming mode

When a 6-channel programming mode group (1/4 -> 2/4 -> 3/4 -> 4/4) or 12-channel programming mode group (1/2-> 2/2) is input continuously in order, the interval of 3 ms or more is not necessary.

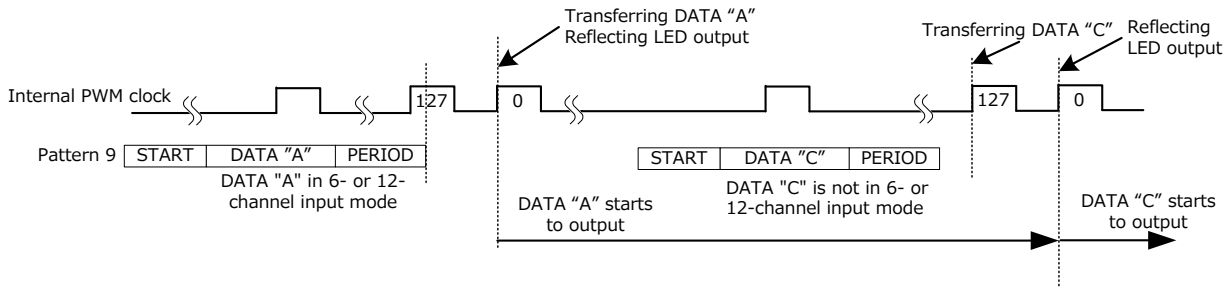
However, when same IDs and same channel data in 6 or 12-channel programming mode are input, the interval of 3 ms or more is necessary. PWM control may not be performed correctly.



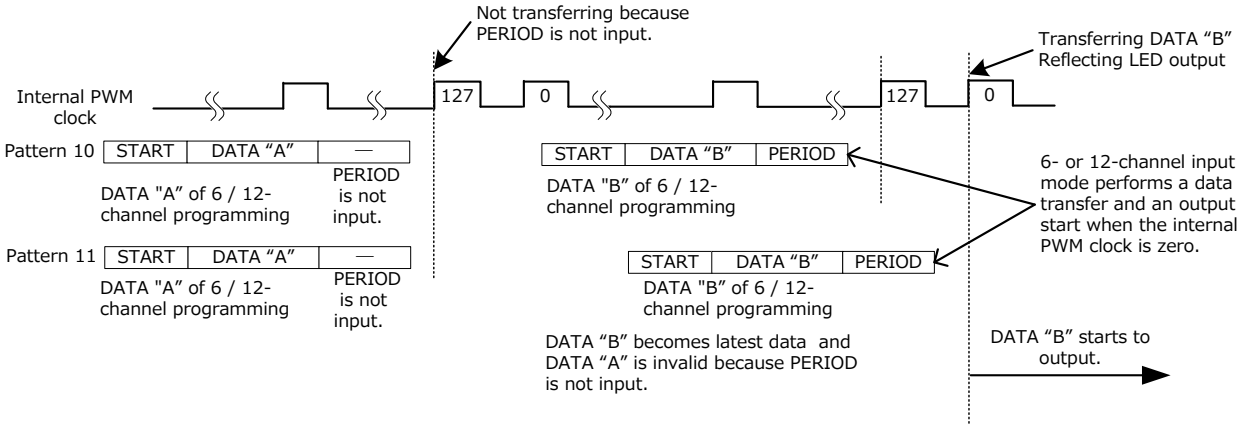
Since there is no input invalid period in 6-channel or 12-channel programming mode, an input data are started to output at the rising edge of the first zero internal PWM clocks after inputting the period command.

Therefore, when other programming mode is input immediately after 6-channel or 12-channel programming, the 6-channel or 12-channel programming data immediately before are re-written to the data input in other programming mode.

When 6-channel or 12-channel programming is used, 24-channel units of input are recommended.

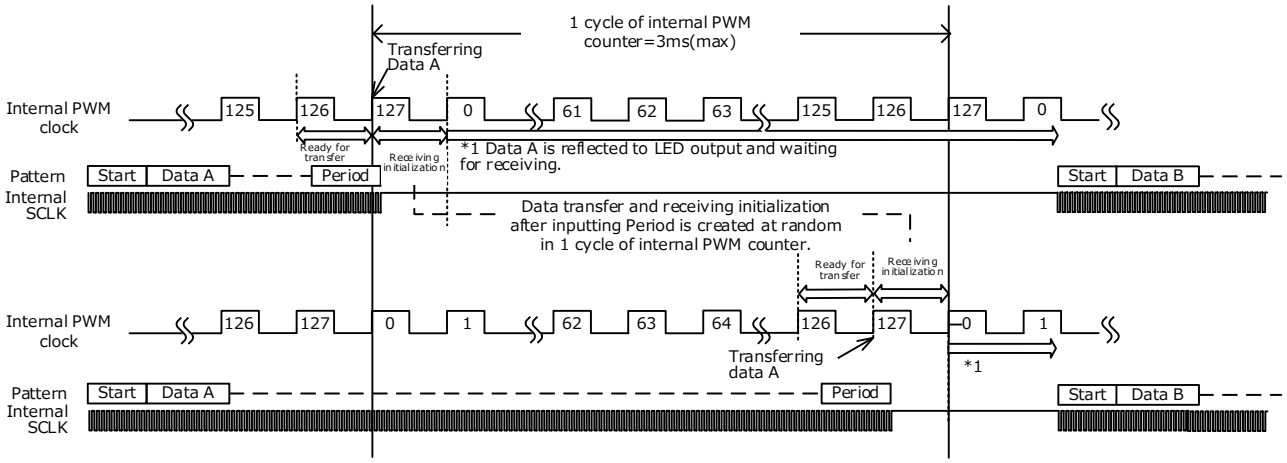


g) In case the period command mistakes



When the period command of DATA "A" is not input and the period command of next DATA "B" is input, DATA "B" starts output immediately after at the rising edge of zero internal PWM clocks.

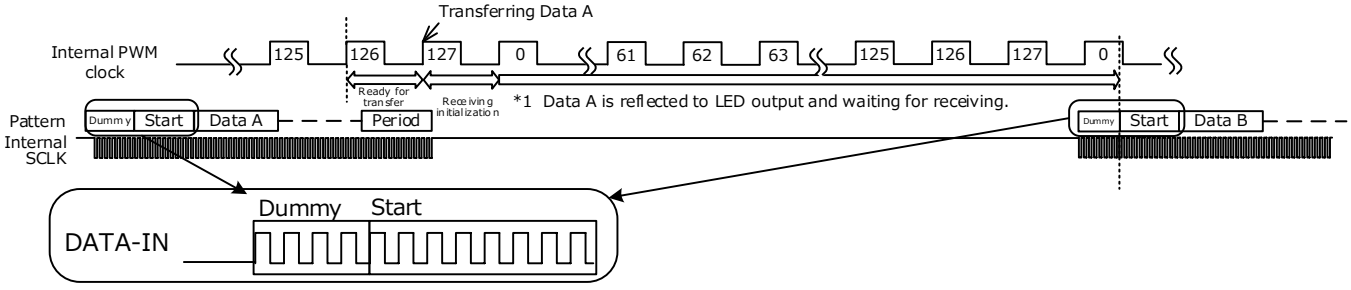
h) In case of matching asynchronously the timing between pattern end and internal data update



In case of matching asynchronously the timing between SCLK end and internal data update, the start command at the beginning of next pattern may not be received. That may occur in the pattern of first IC if there are patterns for two or more ICs. That does not occur if the pattern length is as follows.

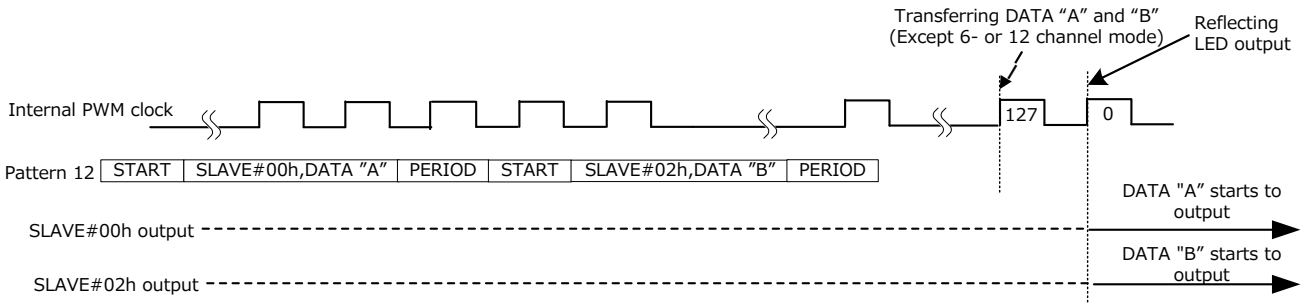
1. Less than minimum 10.6 μs after inputting period command
2. Exceeding maximum 3 ms from point of 1.

This time management is difficult. We recommend that the following measures are applied from initial state to avoid the occurrence of the event.
Dummy data are added to the beginning of the pattern, and 1 time or more SCLKs should be added.
The following figure shows the dummy data = L. However, the dummy data =H is also possible.



(8) Example of basic data input to the different ID.

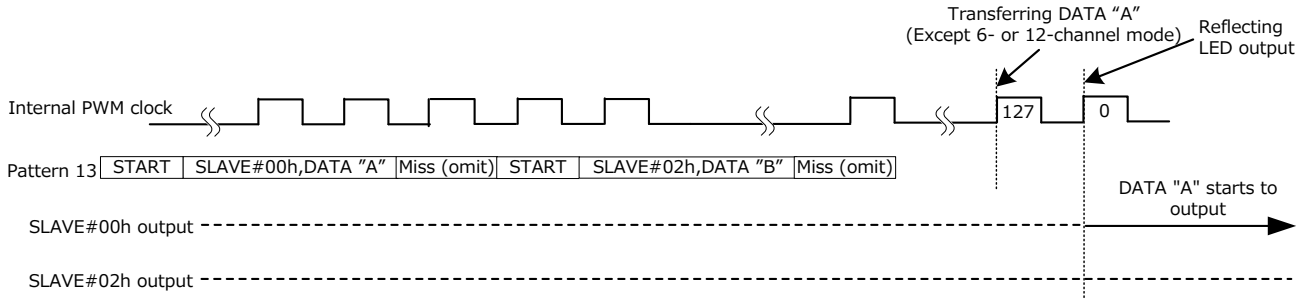
a) In case DATA "B" is input to slave (= 02h) just after DATA "A" is input to slave (= 00h).



Both DATA "A" and DATA "B" are output at the rising edge of zero internal PWM clock which is just after DATA "A" and DATA "B" inputs.

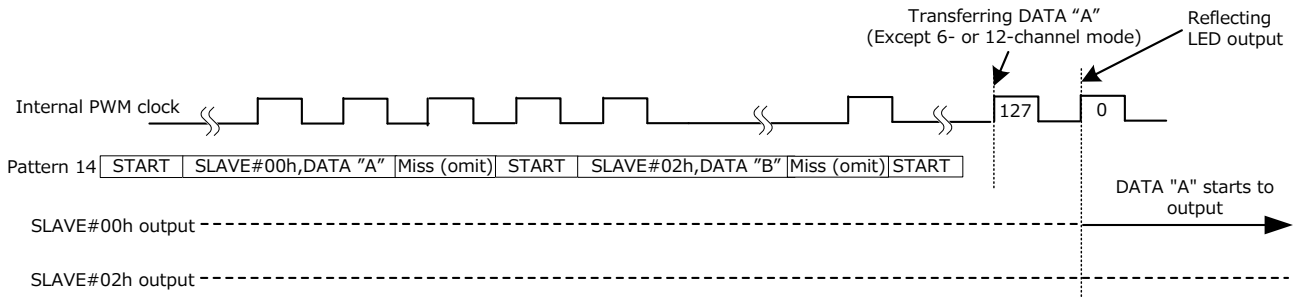
<Reference>
Pay attention that the IC does not operate according to the configuration while following patterns (patterns 13 and 14) are input.

b) In case period command after inputting DATA "A" to the slave (= 00h) is missed or omitted.
In case period command after inputting DATA "B" to the slave (= 02h) is missed or omitted.



DATA "A" is output. DATA "B" is not output.

c) In case start command is input after DATA "B" of pattern 13 is input.



DATA "A" is output. DATA "B" is not output.

Power Supply Block

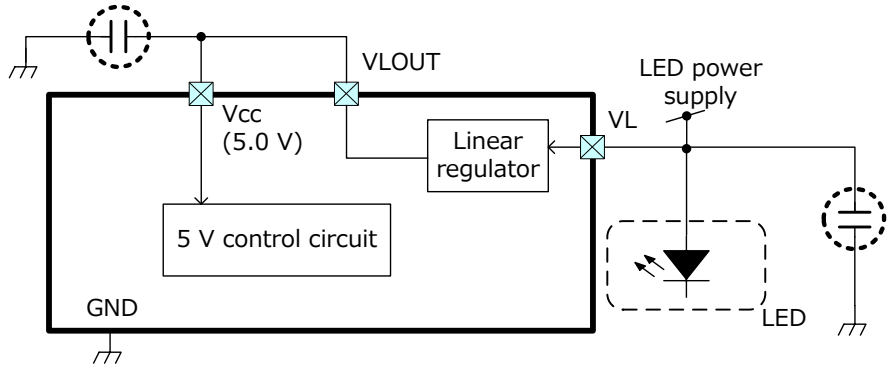
The power supply of this product can be set with the following 2 ways shown in (1) and (2).

(1) When the power supply of LEDs and those of this product are shared (The power supply function of this product is used.)

(2) When this product is operated with 5 V power supply input, not sharing the power supply of LEDs (The power supply function of this product is not used.)

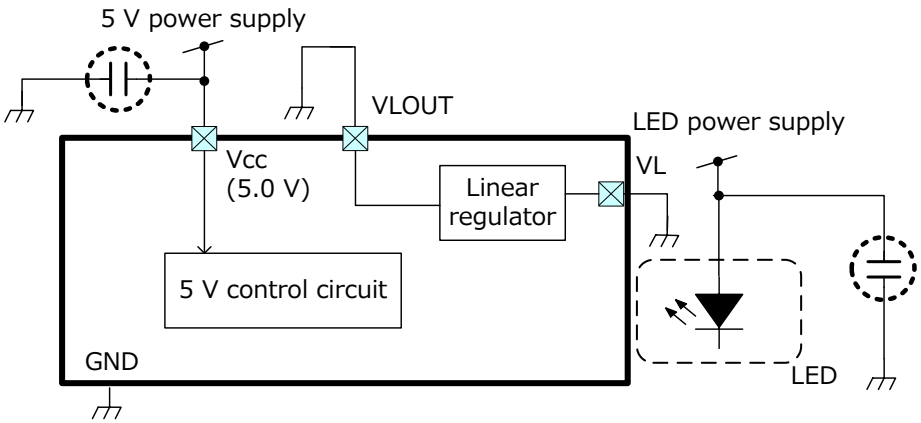
Each settings are shown below.

(1) When the power supply of LEDs and those of this product are shared



As shown in the above, the power supply (7.0 to 28 V) is applied to the VL pin, and VLOUT and Vcc pins are connected directly.
VLOUT pin output (5 V) should be connected within 15 mA (@ all LED outputs 40 mA) except connecting to Vcc of own product.

(2) When 5 V power supply is input to Vcc pin directly



When 5 V power supply is applied to this product without using the built-in power supply, ground VL pin and VLOUT pin to GND.

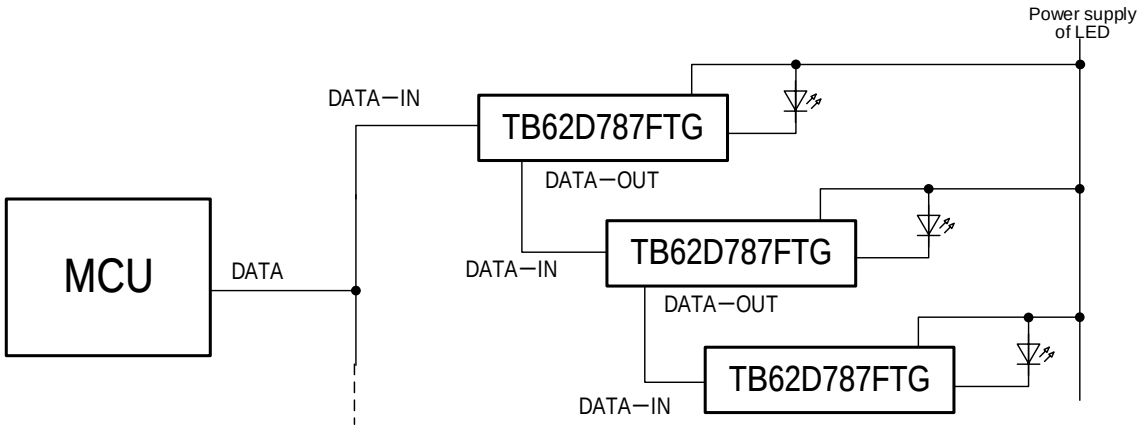
Note: Add decoupling capacitors to VL pin and Vcc pin. The recommended values are as follows.

Recommended value of decoupling capacitors between VL (LED power supply) and GND: 1μF of electrolytic capacitor
*: Evaluate appropriately since it is dependent on the main power supply performance.

Recommended value of decoupling capacitors between Vcc (5 V power supply) and GND: 1μF of electrolytic capacitor and 0.1μF of ceramic capacitor
*: Evaluate appropriately since it is dependent on the LED current to be set and current supply amount of VLOUT.

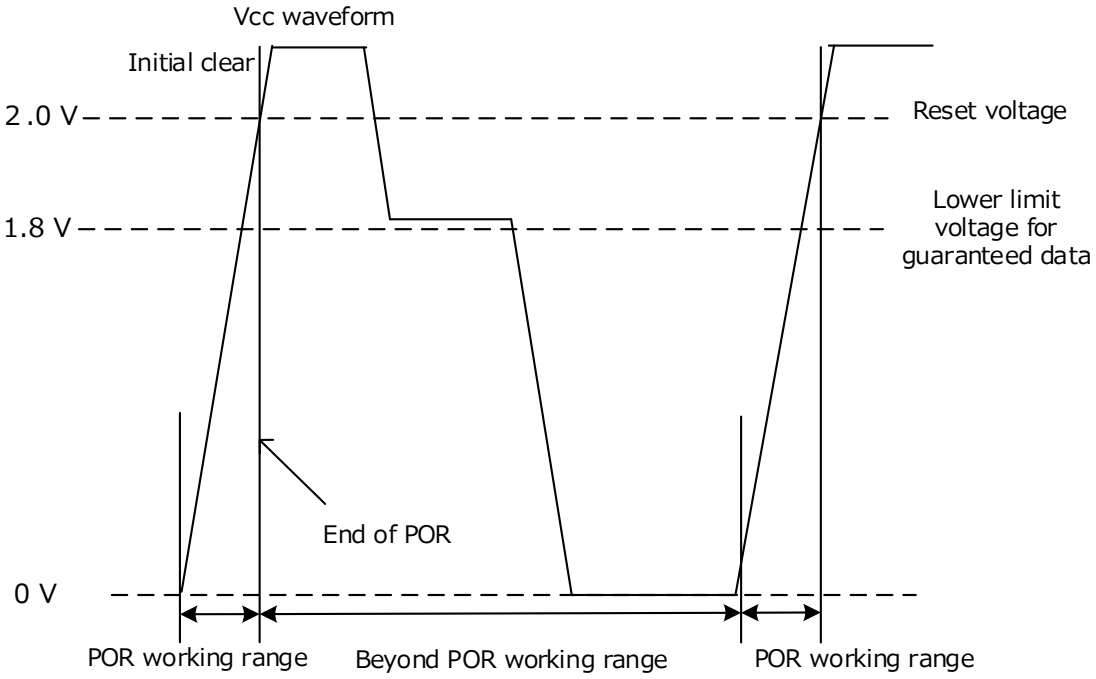
Data buffer

Data buffer is embedded between DATA-IN and DATA-OUT, and it can be used for the cascade connection of two or more these products.
In the case of cascade connection with this buffer, connect up to 5 pieces (@2MHz communication) on the same board.



Power on reset (POR)

It avoids the malfunction by the reset all internal data of IC and setting default in startup.
POR circuit operates only when VDD rises from 0 V. To restart POR, Vcc should be 0 V.
As for the voltage of storing the internal data, it is guaranteed after Vcc reaches 4.5 V or more once.



Thermal shutdown function (TSD)

When the temperature of internal IC exceeds 150°C, all constant current outputs are turned off by this function. The constant current is output again when the temperature decreases to the rating.

TSD operation temperature	150°C to 180°C
TSD reset temperature	20°C below TSD operation temperature

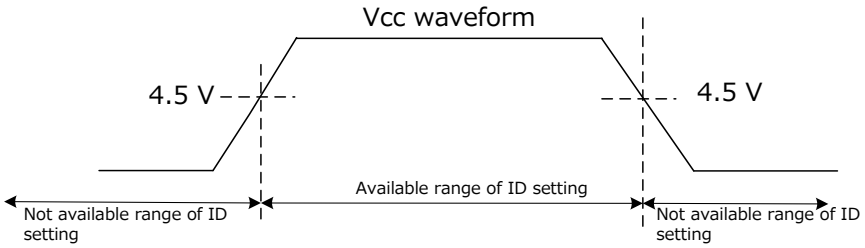
Note: TSD function aims at detecting abnormal heating of ICs. Please avoid positively using the TSD function.

Notes of setting

1. Output load
   This product is the driver in which loads are LEDs. Do not connect loads except LEDs to the output.

2. External resistor for LED drive current setting (REXT-R, REXT-G, and REXT-B)
   The external resistances to be connected to REXT-R, REXT-G, and REXT-B pins should be connected separately. Three resistors must not be collected as one resister. If they are collected, current error is generated in each RGB.

3. Operation sequence of ID setting
   The ID setting can be available when Vcc exceeds 4.5 V after turning on.
   However, in order to prevent malfunction of the ID setting, the transitional input signals of less than 2-clock period of external input data (DATA-IN) are not received.



4. Data setting
   The gradation signals should be input data for 24 channels in the special mode certainly.
   When the data are input to over 24 channels, the data until the input channel are held and the data in 25th channel are invalid.
   When the data are input to less than 24 channels, the data of channels to be input are held, and the data of channels not to be input are held data before the input.

   The gradation signals should be input data for specified channels in 6- or 12-channel programming mode.
   When the data are input to over specified channels, the data until input channel are held and the data over specified channels are invalid.
   When the data input to less than specified channels, the data of channels to be input are held, and the data of channels not to be input are held data before the input.

   Moreover, do not input data which are not indicated in this document.
   Confirm "Programming the TB62D787FTG" and "(6) Notes of data setting."

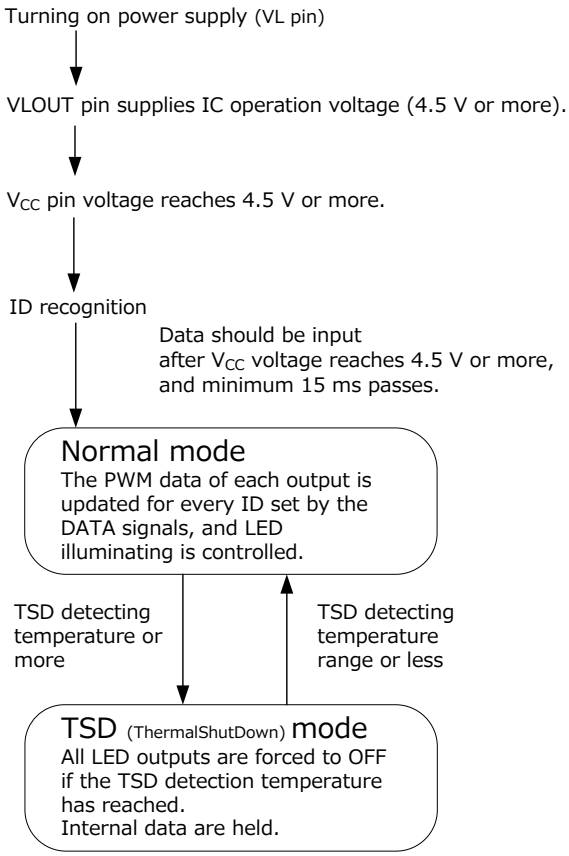
5. Data setting timing
   When data are input to same slave address, next data should be input with spacing the interval 3 ms or more (127 internal PWM clocks) because data may not be received.
   When data are input to different slave address, the interval 3 ms (127 internal PWM clocks) or more is not required.

6. Decoupling capacitor
   For the stabilization of power supply system, it is recommended that decoupling capacitor between power supply and GND should place as near IC as possible. For details, refer to "Power Supply Block."

State Transition Diagram

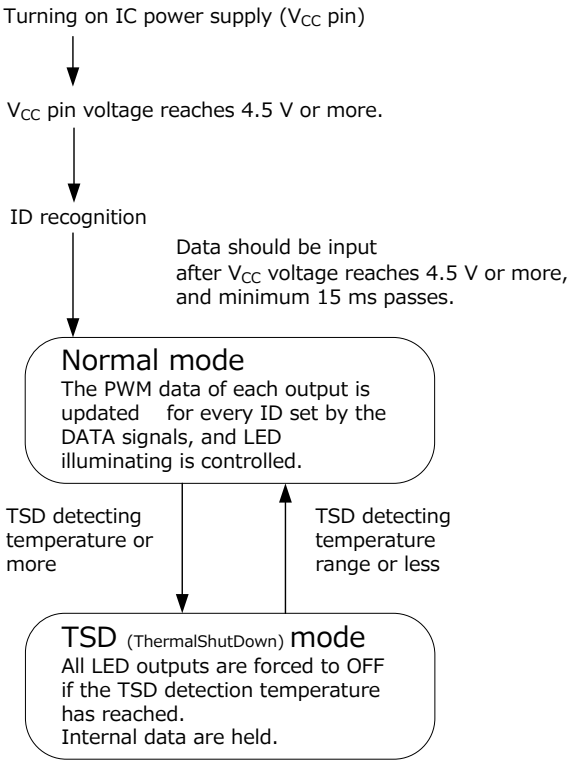
<With VL pin>

VLOUT pin and Vcc pin are wire-connected beforehand, and set each IC's ID (from ID0 to ID2 pin).



<Without VL pin>

VLOUT pin and VL pin are wire-connected to GND beforehand, and set each IC's ID (from ID0 to ID2 pin).



Absolute Maximum Ratings (T_a=25°C)

Characteristics	Symbol	Rating	Unit
VL pin power supply voltage	VL	29	V
Vcc pin power supply voltage	Vcc	6.0	V
Input voltage	V_{IN}	-0.3 to 6.0 (Note 1) -0.3 to Vcc + 0.3 (Note 2)	V
Output current	I_{OUT}	85 (Note 5)	mA/ch
Output voltage	V_{OUT}	-0.3 to 29	V
Power dissipation	P_d	4.3 (Note 3)(Note 4)	W
Thermal resistance	$R_{th\ (j\text{-}a)}$	29.1 (Note 3)	°C/W
Operating Temperature Range	T_{opr}	-40 to 85	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Maximum junction Temperature	T_j	150	°C

Note 1: DATA-IN pin

Note 2: ID0 to ID2 pin, do not exceed 6.0V.

Note 3: When mounted on a PCB (Material: FR-4 compliant with JEDEC 4 layers board, Board size:114.3×76.2mm t=1.6mm)

Note 4: Power dissipation is reduced by 1/ $R_{th(j\text{-}a)}$ for each °C above 25°C ambient.

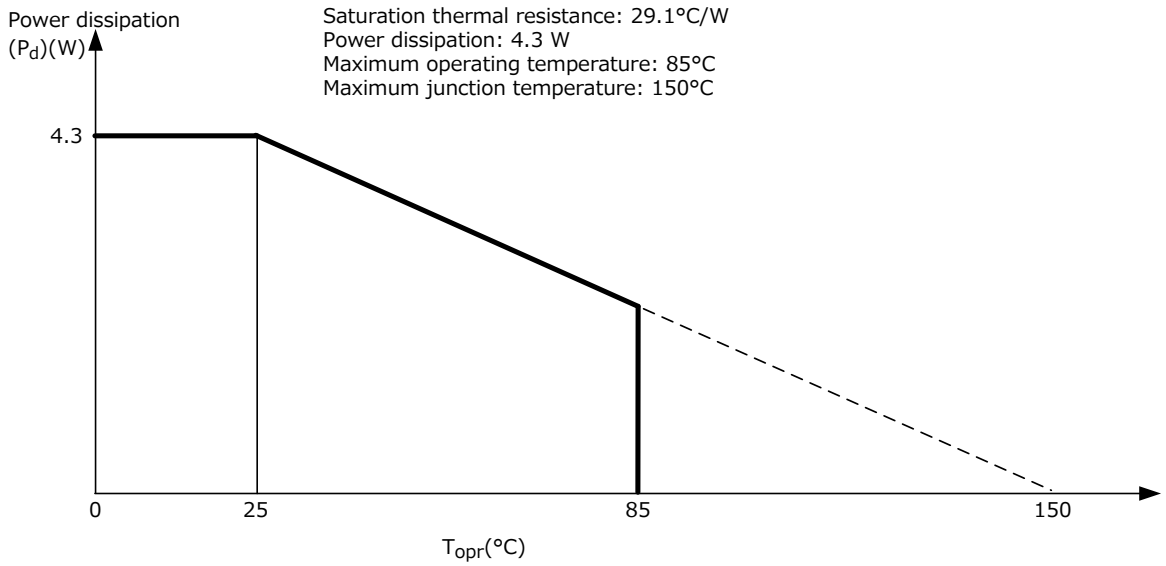
Note 5: Current may be further restricted due to ambient temperature or board condition.

T_a: Ambient temperature of ICs

T_{opr}: Ambient temperature of ICs to be operated

T_j: IC chip temperature during operating
For the design, it is recommended that the maximum of T_j is considered of the amount of use dissipation at about 120°C.

Power Dissipation of package

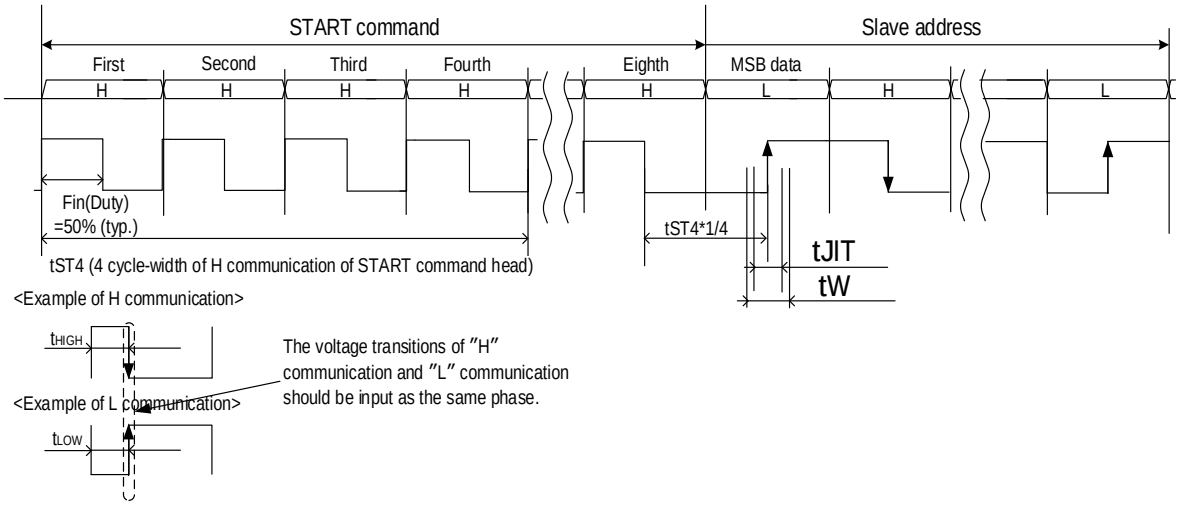


Operating Ranges (T_a=-40 to 85°C, Fin=0.5 to 2.0MHz, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
VL pin power supply voltage	VL	—	7.0	—	28	V
Vcc pin power supply voltage	Vcc	—	4.5	—	5.5	V
Output voltage	$V_{OUT(ON)}$	All outputs	0.5	—	4	V
Constant current output range	I_{OUT}	All outputs	5	—	40	mA/ch
Input DATA Frequency	Fin	—	0.5	—	2.0	MHz
DATA detection window width	tW	—	135	—	—	ns
Input DATA allowable input jitter width	tJIT	The transition of input DATA potential is the center.	—	—	±54	ns
Input DATA minimum pulse width	t_{HIGH}, t_{LOW}	—	100	—	—	ns
Input Voltage	V_{IH}	DATA-IN	0.7 × Vcc	—	Vcc	V
	V_{IL}		GND	—	0.3 × Vcc	
	V_{ID0}	ID0, ID1, ID2 VREXT=1.128 V (typ.)	0	—	0.1	
	V_{ID1}		VREXT -0.1	VREXT	VREXT +0.1	
	V_{ID2}		Vcc -0.1	—	Vcc	
VLOUT load current	ΔVl	Except Supply current LED current setting is up to 40 mA.	—	—	15	mA

Definition of input DATA (DATA-IN) and allowable width of jitter:

In the following figure, the START command communication is learned and the voltage transition is detected from Slave address communication. The data are received when the voltage transition is in the detection window including jitter and communication delay.



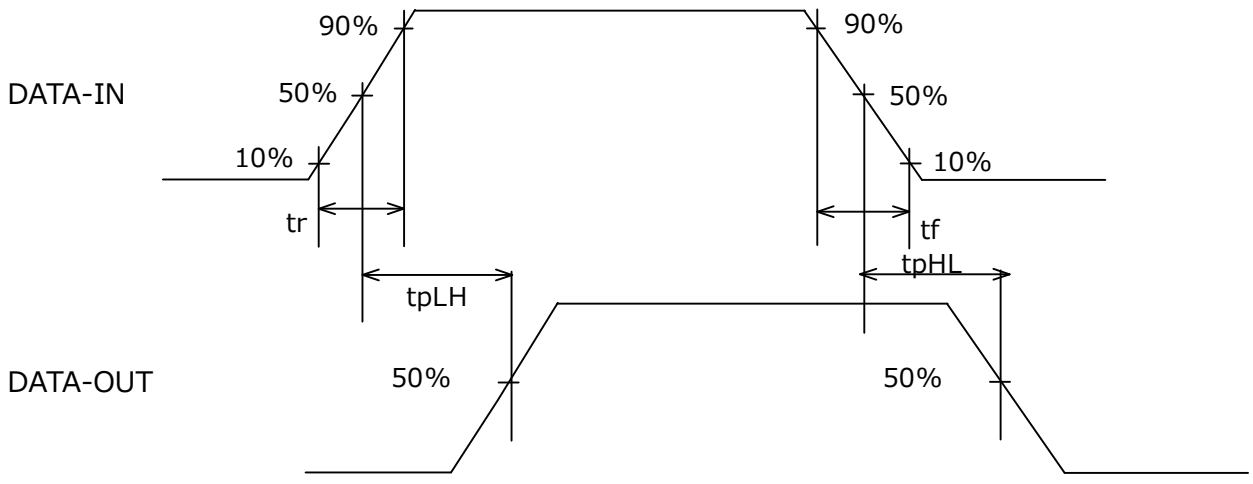
Note: Output format of control signal port

CMOS push-pull type is recommended for the output port of the controller.
When the open-drain output is used, the potential transition of H and L communications may not be same. Therefore, pay attention to the communication wave.

Electrical Characteristics (T_a=25°C, VL=15V, Vcc=VLOUT, Unless otherwise specified)

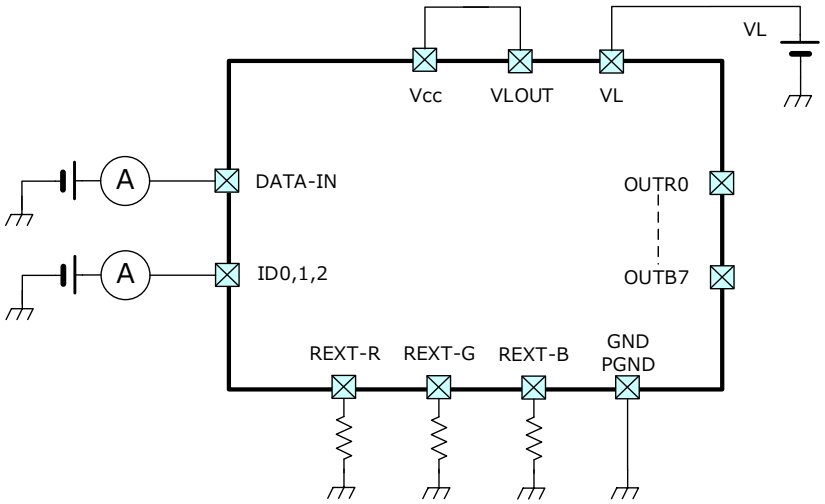
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output current	I_{OUT1}	V_{OUT} = 0.5 V, REXT = 1.2 kΩ	12.5	13.3	14.1	mA
Output current accuracy between channels	ΔI_{OUT2}	V_{OUT} = 0.5 V, REXT = 1.2 kΩ All LED outputs ON	—	—	±3.0	%
Output leakage current	I_{OZ}	V_{OUT} = 28 V	—	—	1	μA
VLOUT pin voltage	VLOUT	—	4.5	—	5.5	V
Input current	I_{IH}	DATA-IN	—	—	1	μA
	I_{IL}	DATA-IN	—	—	-1	
	I_{ID}	ID0, ID1, ID2	—	—	±10	
Output current dependent on Vcc	%/Vcc	When changed Vcc = 4.5 V to 5.5 V	—	1	2	%
Power supply current in operation	$I_{CC\ (VL)}$	When applied VL=15 V REXT = 1.2 kΩ, V_{OUT} = 0.5 V,	—	12	19	mA
	$I_{CC\ (Vcc)}$	When connected VL=GND REXT = 1.2 kΩ, V_{OUT} = 0.5 V,	—	11.5	16	
H Level DATA-OUT pin Output Voltage	VOH	IOH= -1 mA	Vcc -0.4	—	—	V
L Level DATA-OUT pin Output Voltage	VOL	IOL= 1 mA	—	—	0.4	V
DATA-IN–DATA-OUT Propagation Delay Time (Note)	tpLH	CL = 15 pF, tf = tf = 3 ns	—	—	20	ns
	tpHL		—	—	20	
PWM reference frequency	fPWM	Reference frequency of internal PWM counter	—	70	—	kHz

Note: DATA-IN – DATA-OUT definition

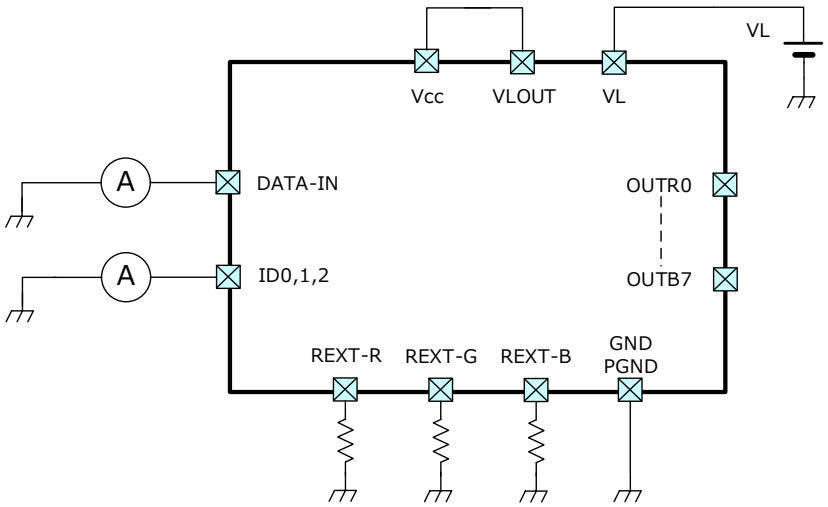


Test Circuit

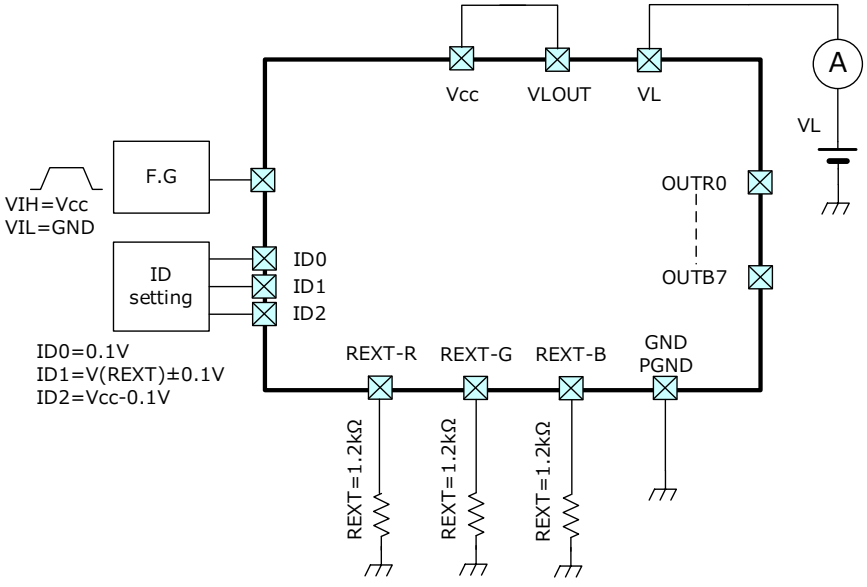
Test Circuit 1 Input Current (IIH)



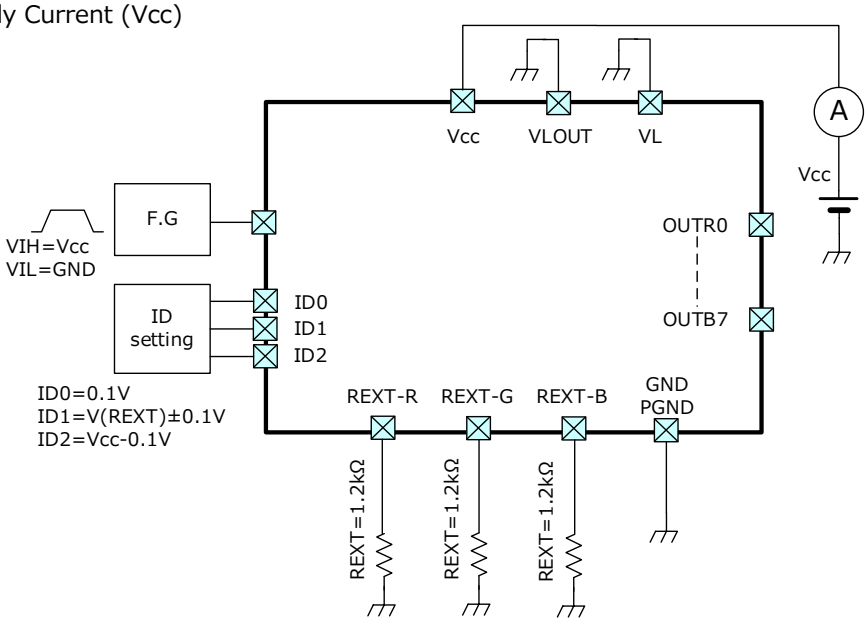
Test Circuit 2 Input Current (IIL)



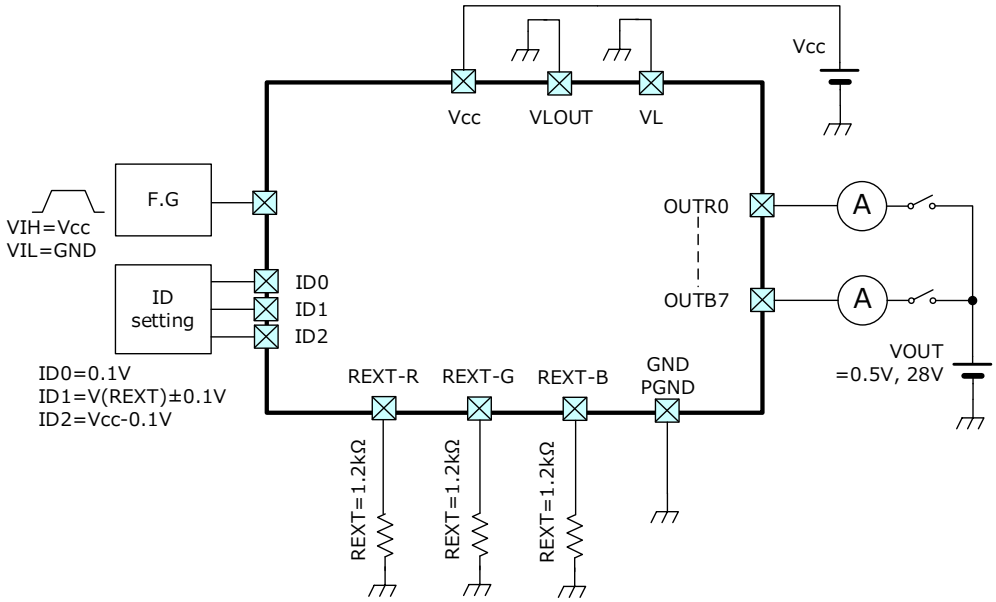
Test Circuit 3 Supply Current (VL)



Test Circuit 4 Supply Current (Vcc)

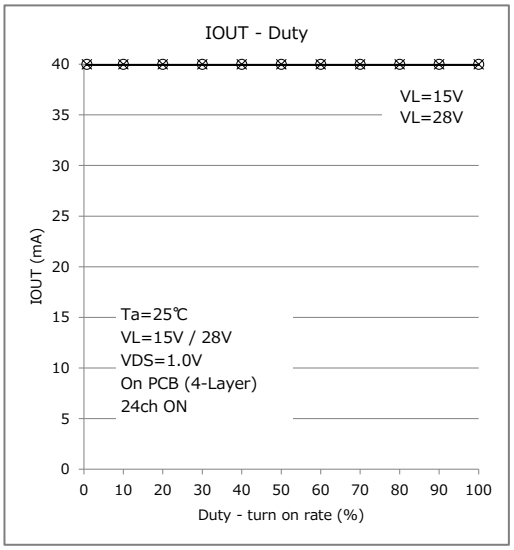


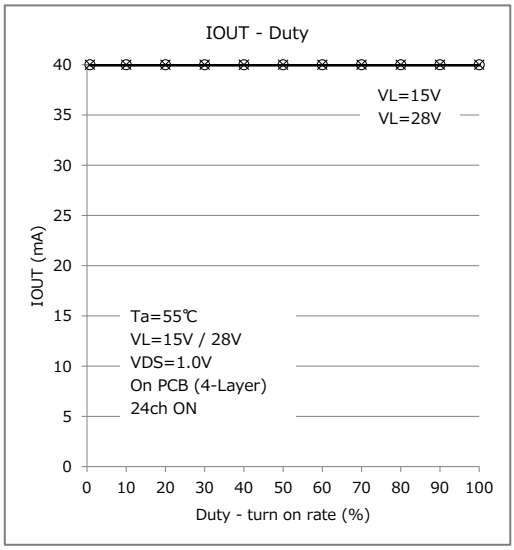
Test Circuit5 Output Current / Output Leakage Current / Output Current Accuracy / Changes in Constant Output current dependent on Vcc

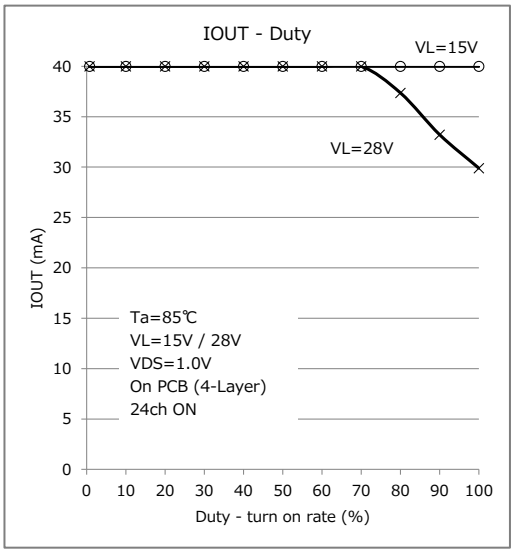


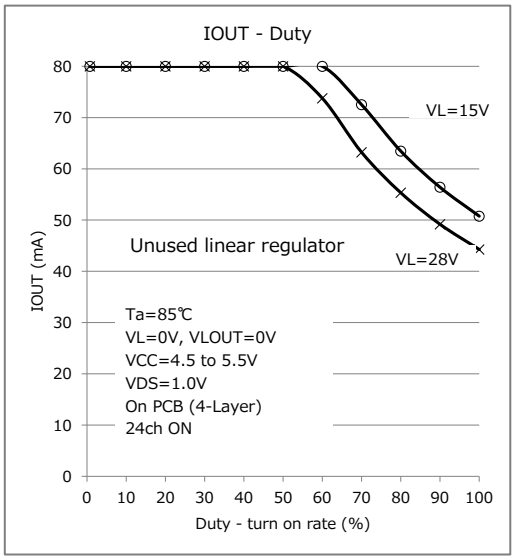
Output current - derating (illuminating rate) graph

Board condition: Material: FR-4 (Compliant with JEDEC 4 layers board), Board size: 114.3×76.2mm, t=1.6 mm
When the pulse width is 25 ms or more, it is regarded as DC.

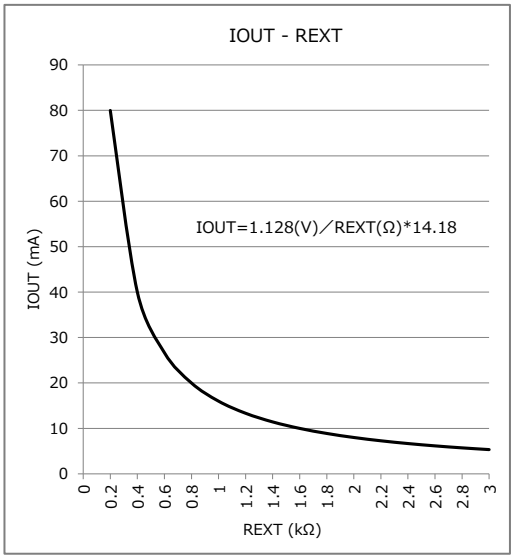




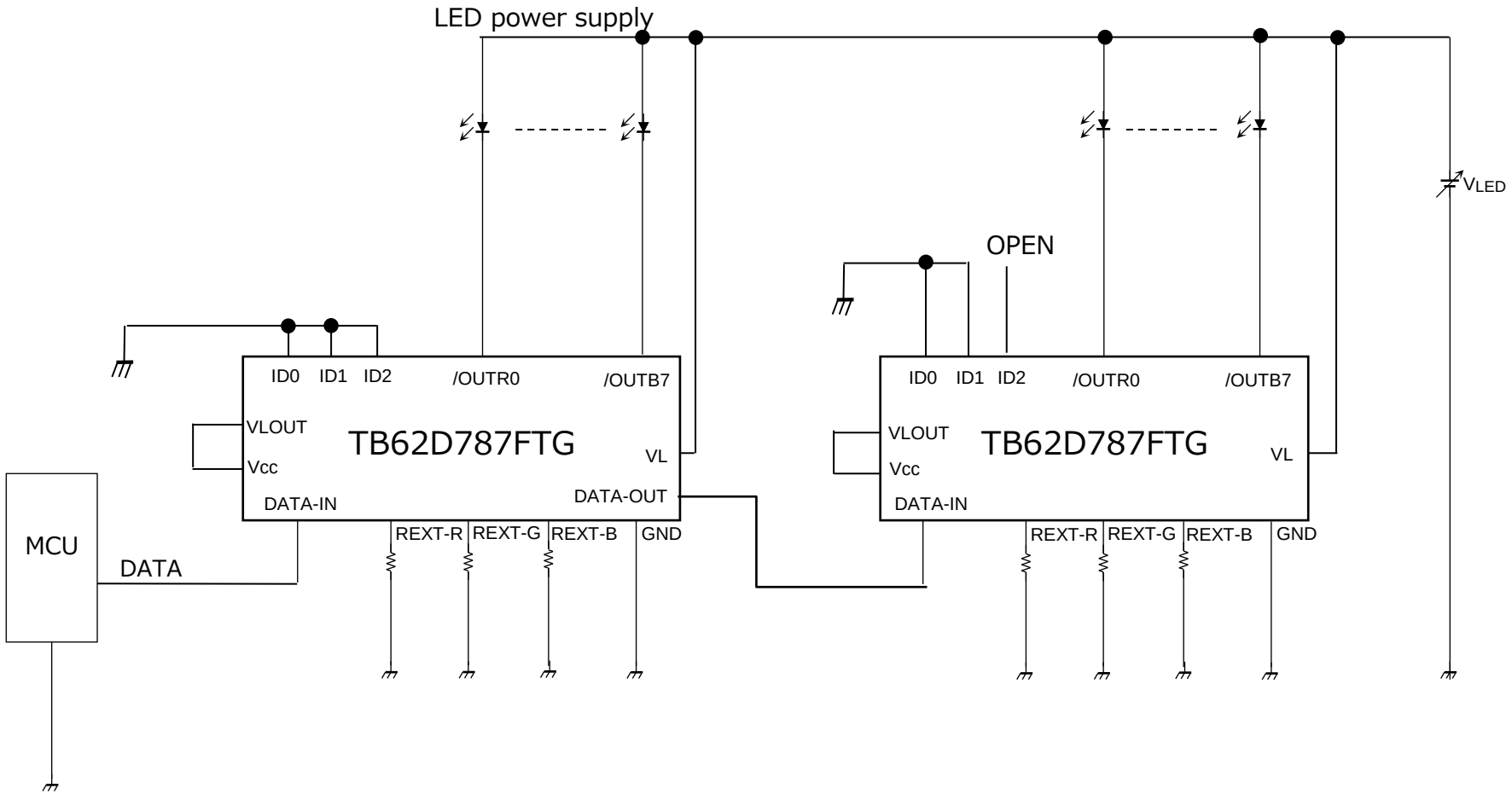




Output current - external resistance characteristic (typ.)



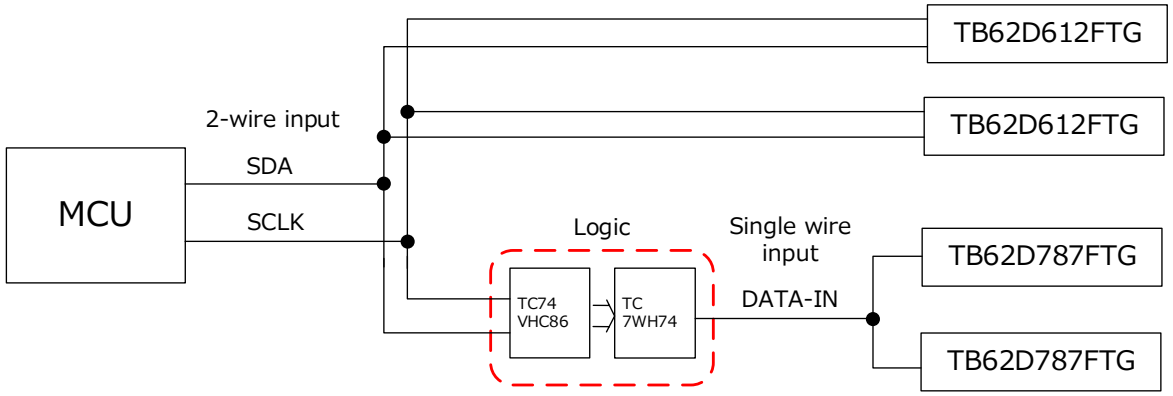
Example of application circuit 1



Example of application circuit 2

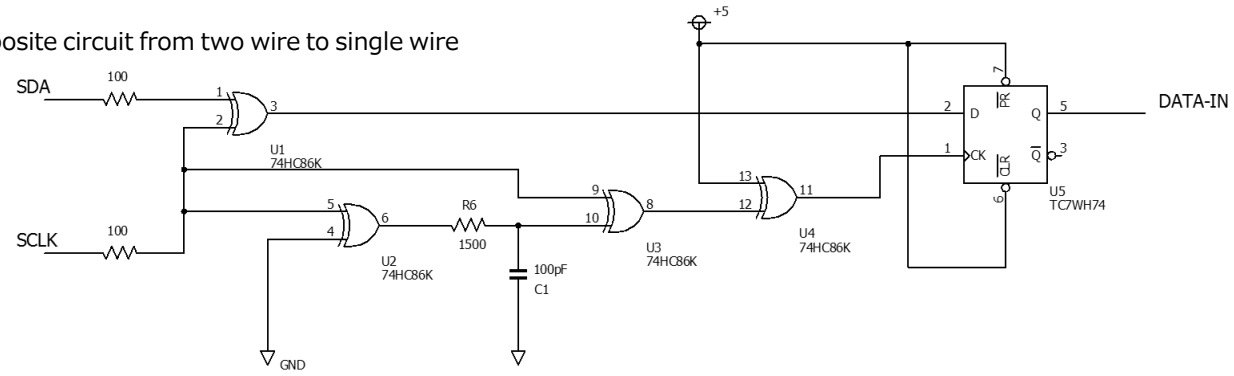
When it controls from the same ports of TB62D612FTG, which is 2-wire input control LED driver and the MCU, connect the Exclusive-OR gate (TC74VHC86) and D-Flip/Flop to preceding phase of the input of this product as shown below.
At this time, the DATA and CLOCK of the interval period should be set to High level.
Since phase differences between DATA from MCU outputting and clock may occur, confirm the operation enough with the following configuration.

● System configuration

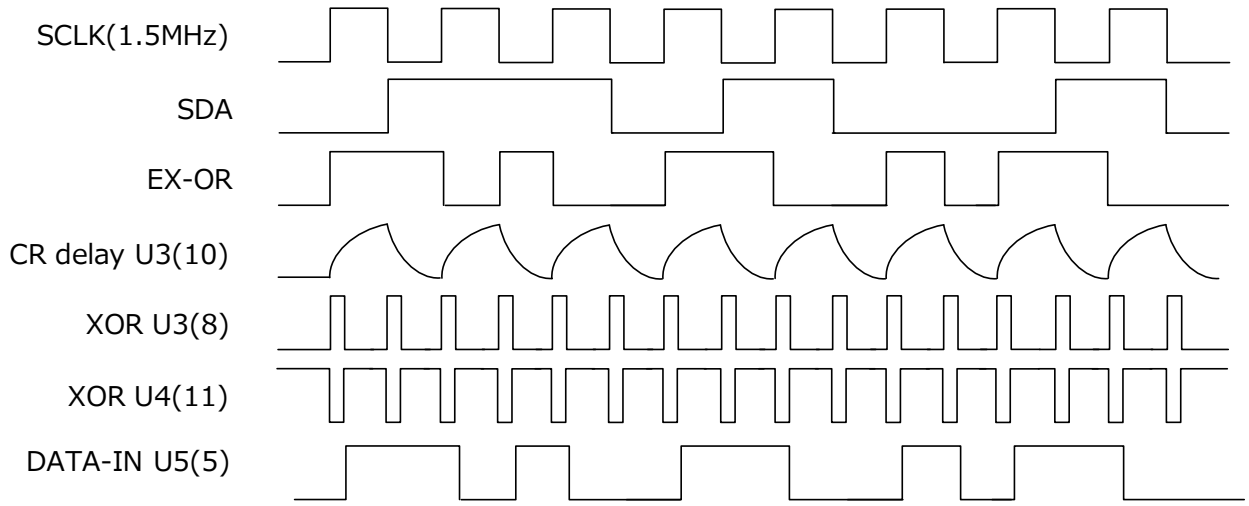


● Logic

Composite circuit from two wire to single wire



● Timing charts

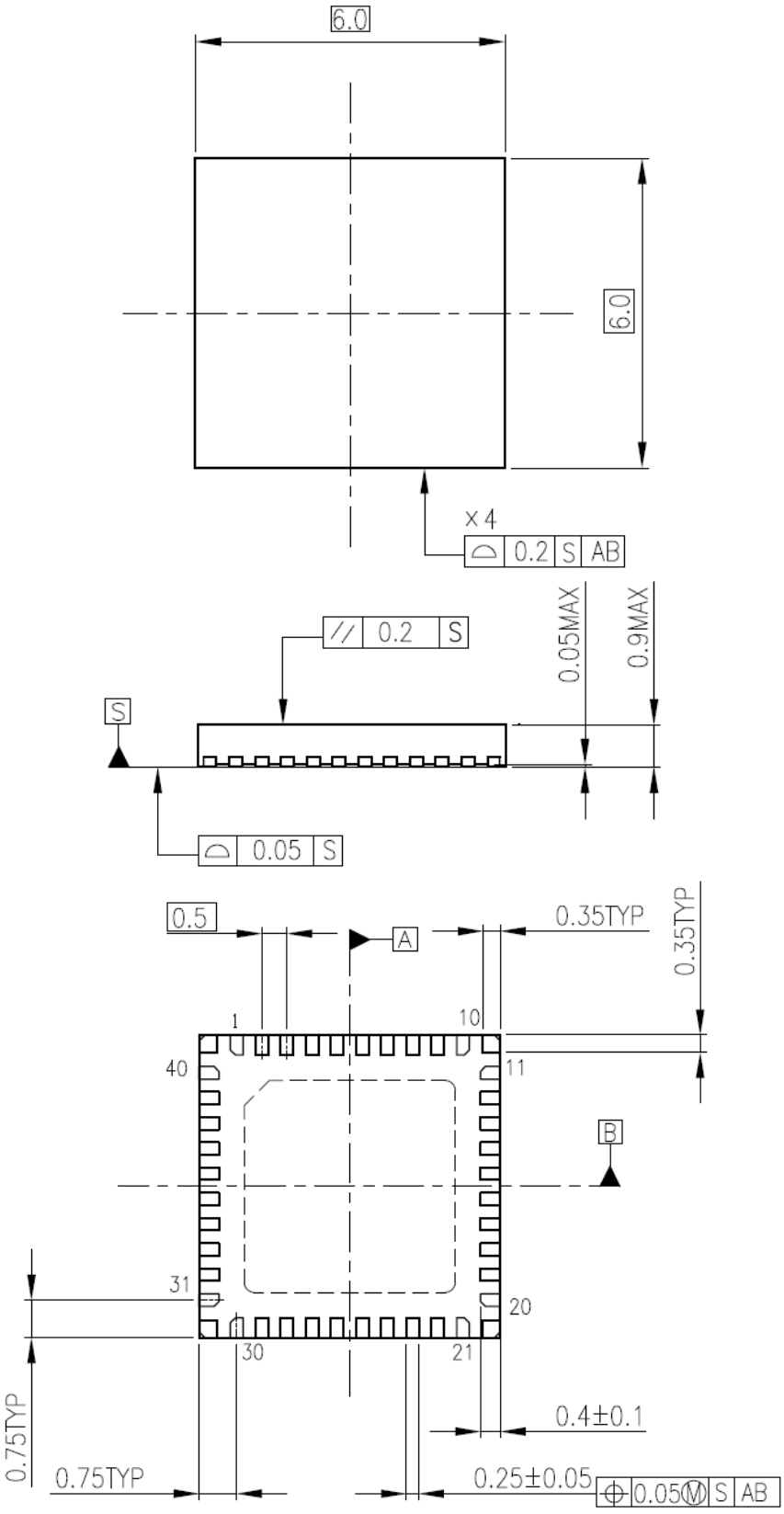


Note: When this circuit is used, the interval period should be fixed to SDA=SCLK=High.

Package Dimensions

P-VQFN40-0606-0.50-001

Unit: mm



Weight: 0.097g (Typ.)

Notes of Contents

1. Block diagram

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing charts

Timing charts may be simplified for explanatory purposes.

4. Application circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Providing these application circuit examples does not grant a license for industrial property rights.

5. Test circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(3) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**