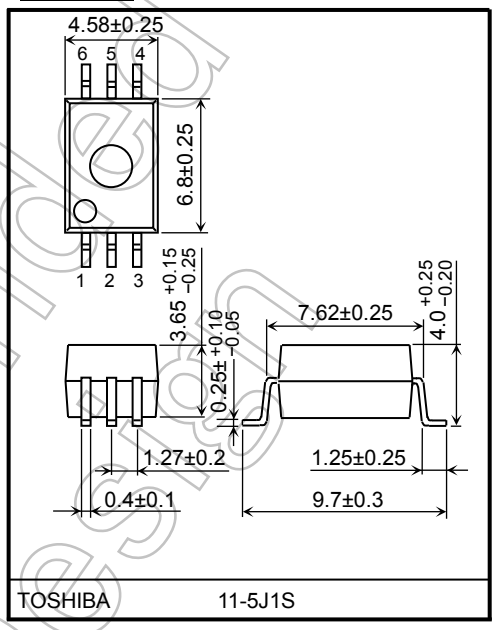
TLP708, TLP708F

Factory Automation (FA)
Home Electrical Appliances
Operates at high ambient temperature up to 125°C

TLP708

Unit: mm



Weight: 0.26 g (typ.)

The Toshiba TLP708 consists of an infrared emitting diode and an integrated high-gain, high-speed photodetector. The TLP708 is housed in the SDIP6 package. Compared to the standard DIP8 package, TLP708 is smaller in size, yet comes with international safety standards under a reinforced isolation category. As such, it is possible to reduce the mounting footprint for applications that require certifications for safety standards.

The photodetector has an open-collector output stage, and an internal Faraday shield that provides a guaranteed common-mode transient immunity of ±15 kV/μs. As TLP708 is also able to operate up to 125℃, it is suitable for use in applications like industrial equipments where it is necessary to operate under high ambient temperature.

TLP708F is of a long creepage distance and clearance distance type.

- Input threshold current : I_{FHL} = 5mA (max)
- Switching time (t_{pHL}/t_{pLH}): 75ns (max)
- Data transfer rate: 15 MBd (typ.)
- Guaranteed Performance over temperature: -40 to 125 ℃
- Power supply voltage: 4.5 to 5.5 V
- Common mode transient immunity: ±15 kV /μs (min)
- Isolation voltage: 5000 V_{rms} (min)
- Construction mechanical rating

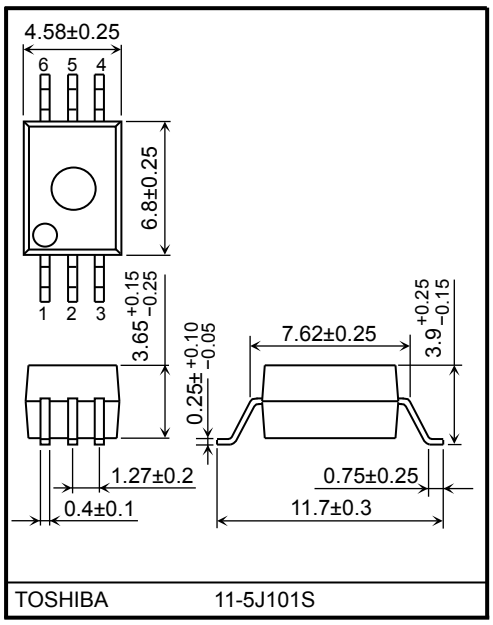
	7.62 mm Pitch TLP708 Type	10.16 mm Pitch TLP708F Type
Creepage distance	7.0 mm (min)	8.0 mm (min)
Clearance distance	7.0 mm (min)	8.0 mm (min)
Insulation thickness	0.4 mm (min)	0.4 mm (min)

- UL-recognized: UL 1577, File No. E67349
- cUL-recognized: CSA Component Acceptance Service No.5A, File No. E67349
- VDE-approved: EN 60747-5-5, EN 62368-1 (Note 1)

Note 1 : When a VDE approved type is needed, please designate the **Option (D4)**.

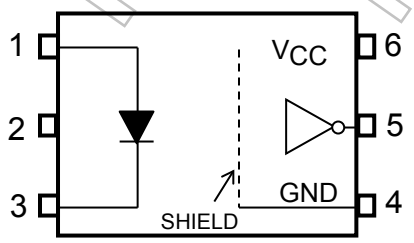
TLP708F

Unit: mm



Weight: 0.26 g (typ.)

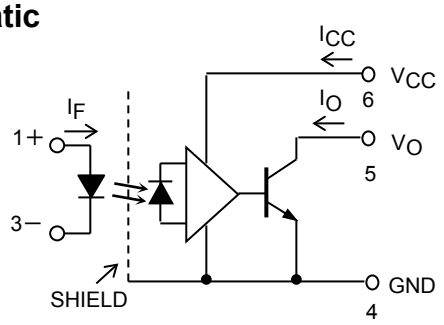
Pin Configuration (Top View)



1:ANODE
2:N.C.
3:CATHODE
4:GND
5:V_O(Output)
6:V_{CC}

Start of commercial production
2010-06

Schematic



Note: A 0.1μF bypass capacitor must be connected between pins 6 and 4.

Truth Table

Input	Output
H	L
L	H

Absolute Maximum Ratings (Ta = 25℃)

Characteristics			Symbol	Rating	Unit
LED	Forward Current	(Ta < 110℃)	I_F	25	mA
	Forward Current Derating	(Ta ≥ 110℃)	ΔI_F/℃	-0.67	mA/℃
	Pulse Forward Current (Note 1)	(Ta < 110℃)	I_{FP}	50	mA
	Pulse Forward Current Derating	(Ta ≥ 110℃)	ΔI_{FP}/℃	-1.34	mA/℃
	Reverse Voltage		V_R	5	V
	Input Power Dissipation	(Ta < 110℃)	P_D	40	mW
	Input Power Dissipation Derating	(Ta ≥ 110℃)	ΔP_D/℃	-1.0	mW/℃
DETECTOR	Output Current	(Ta ≤ 125℃)	I_O	25	mA
	Output Voltage		V_O	6	V
	Supply Voltage		V_{CC}	6	V
	Output Power Dissipation	(Ta < 110℃)	P_O	80	mW
	Output Power Dissipation Derating	(Ta ≥ 110℃)	ΔP_O/℃	-2.0	mW/℃
Operating Temperature Range			T_{opr}	−40 to 125	℃
Storage Temperature Range			T_{stg}	−55 to 150	℃
Lead solder Temperature (10 s)			T_{sol}	260	℃
Isolation voltage (Note 2)			BV_S	5000	V_{rms}

Note: Using continuously under heavy loads (e.g. an application of high temperature/current/voltage and a significant change in temperature, etc.) may cause this product to decrease in reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc)

Note 1: Pulse width ≤ 1ms, duty = 50 %

Note 2: R.H. ≤ 60 %, Ta = 25 ℃, AC 60 s
This device is regarded as a two-terminal device: pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Recommended Operating Condition

Characteristics	Symbol	Min	Typ.	Max	Unit
'L' level input voltage	V_{FL}	0	—	0.8	V
'H' level input current	I_{FH}	7.5	—	15	mA
Supply voltage*	V_{CC}	4.5	—	5.5	V
Operating temperature range	T_{opr}	-40	—	125	°C

* This item denotes operating ranges, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. In addition, each item is an independent guideline. In developing designs using this product, please confirm the specified characteristics shown in this document.

Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 125°C, V_{CC} = 4.5 to 5.5V)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ.*	Max	Unit
Input forward current	V_F	—	I_F = 10 mA, Ta = 25 °C	1.40	1.57	1.80	V
Temperature coefficient of forward voltage	$\Delta V_F / \Delta Ta$	—	I_F = 10 mA	—	−1.8	—	mV/°C
Input reverse current	I_R	—	V_R = 5 V, Ta = 25 °C	—	—	10	μA
Input capacitance	C_T	—	V_F = 0 V, f = 1 MHz, Ta = 25 °C	—	60	—	pF
"H" level output current	I_{OH}	1	V_F = 0.8 V, V_O = 5.5 V	—	—	250	μA
			V_F = 0.8 V, V_O = 5.5 V Ta = 25 °C		0.5	10	
"L" level output voltage	V_{OL}	2	I_F = 10 mA, I_{OL} = 13 mA (sink)	—	0.3	0.6	V
Input threshold current	I_{FHL}	—	I_{OL} = 13 mA (sink), V_O < 0.6 V	—	1.5	5.0	mA
"H" level supply current	I_{CCH}	3	I_F = 0 mA	—	1.5	5.0	mA
"L" level supply current	I_{CCL}	4	I_F = 10 mA	—	1.4	5.0	mA

*All typical values are at Ta = 25 °C, V_{CC} = 5 V unless otherwise specified.

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Capacitance input to output	C_S	V_S = 0 V, f = 1 MHz	—	0.8	—	pF
Isolation resistance	R_S	R.H. ≤ 60 %, V_S = 500 V	10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC,60 s	5000	—	—	V_{rms}

Note :This device is regarded as a two-terminal device: pins 1, 2 and 3 are shorted together,and pins 4, 5 and 6 are shorted together.

Switching Characteristics

(Unless otherwise specified, Ta = -40 to 125°C, V_{CC} = 4.5 to 5.5 V)

Characteristic	Symbol	Test Circuit	Test Conditions		Min	Typ.*	Max	Unit
Propagation delay time to logic low output	t_{pHL}	5	I_F = 0→7.5 mA	R_L = 350 Ω, C_L = 15 pF (Note 4)	—	35	75	ns
Propagation delay time to logic high output	t_{pLH}		I_F = 7.5→0 mA		—	35	75	ns
Switching time dispersion between ON and OFF	$\|t_{pHL}-t_{pLH}\|$		I_F = 0↔7.5 mA	R_L = 350 Ω, C_L = 15 pF (Note 4)	—	12	35	ns
Propagation delay skew (Note 5)	t_{psk}				-50	—	50	ns
Output fall time (90-10%)	t_f		I_F = 0→7.5 mA	R_L = 350 Ω, C_L = 15 pF (Note 4)	—	6	—	ns
Output rise time (10−90%)	t_r		I_F = 7.5→0 mA		—	18	—	ns
Common mode transient immunity at high level output	CM_H	6	V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{CC} =5 V, Ta = 25 °C		+15	—	—	kV/μs
Common mode transient immunity at low level output	CM_L		V_{CM} = 1000 V_{p-p}, I_F = 10 mA, V_{CC} = 5 V, Ta = 25 °C		−15	—	—	kV/μs

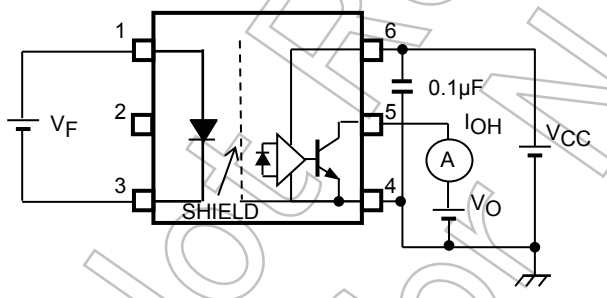
*All typical values are at Ta=25°C

Note 3: A ceramic capacitor (0.1 μF) should be connected from pin 6 (V_{CC}) to pin 4 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property. The total lead length between the capacitor and coupler should not exceed 1 cm.

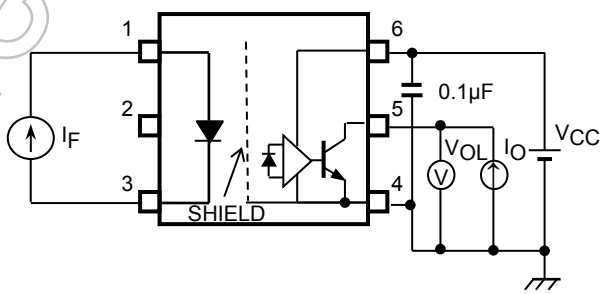
Note 4: f = 5 MHz, duty=50 %, input current t_r = t_f = 4.5 ns,
C_L is less than 15 pF which includes probe and jig/stray wiring capacitance.

Note 5 Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. t_{pHL} or t_{pLH}) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

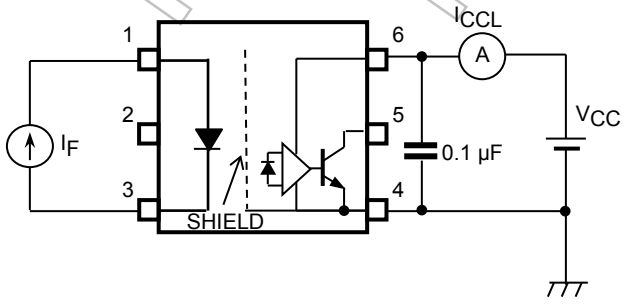
TEST CIRCUIT 1: I_{OH} Test Circuit



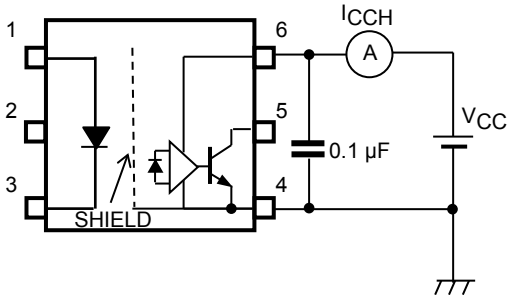
TEST CIRCUIT 2: V_{OL} Test Circuit



TEST CIRCUIT 3: I_{CCL} Test Circuit

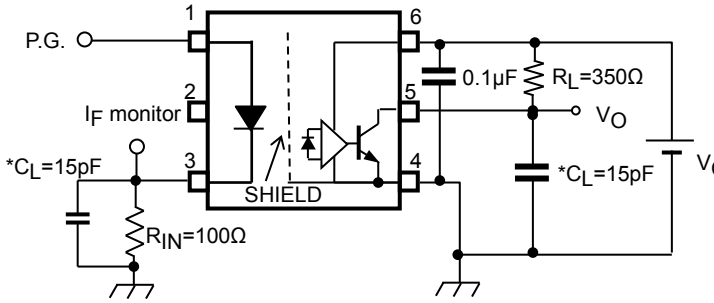


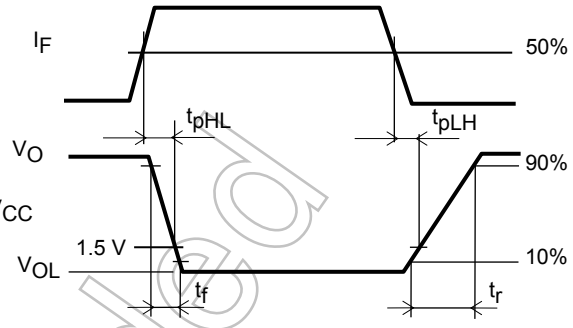
TEST CIRCUIT 4: I_{CCH} Test Circuit



TEST CIRCUIT 5: t_{pHL}, t_{pLH} Test Circuit

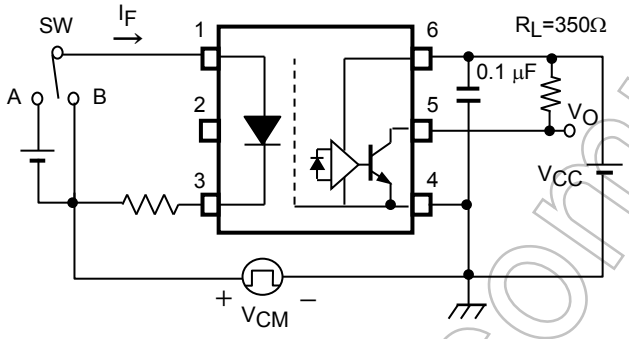
I_F=7.5mA(P.G.)
(f=5MHz, duty=50%, t_r=t_f=4.5ns)

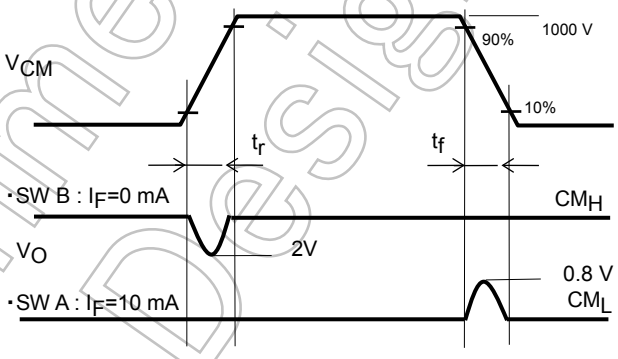




C_L includes probe and stray capacitance.
P.G.: Pulse generator

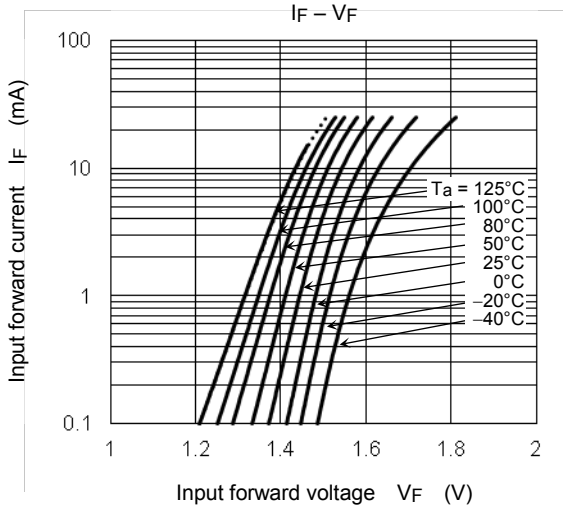
TEST CIRCUIT 6: Common-Mode Transient Immunity Test Circuit



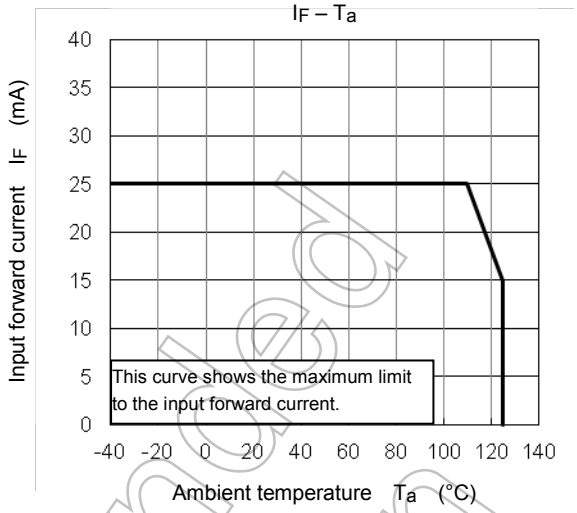


$$CM_H = \frac{800(V)}{t_r(\mu s)} \qquad CM_L = -\frac{800(V)}{t_f(\mu s)}$$

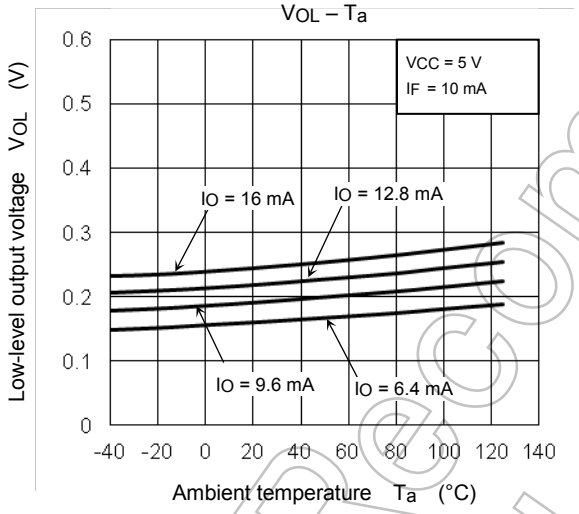
$I_F - V_F$



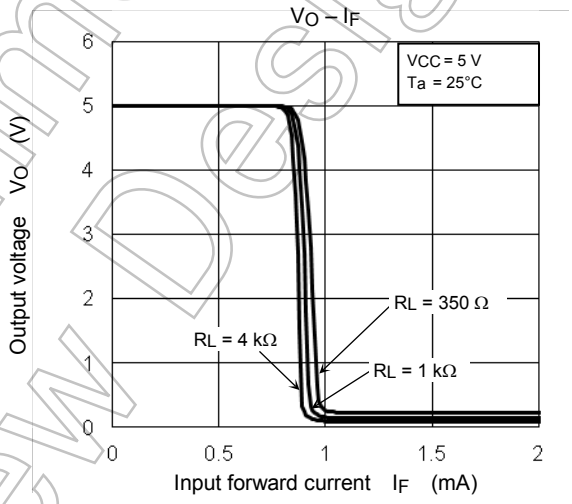
$I_F - T_a$



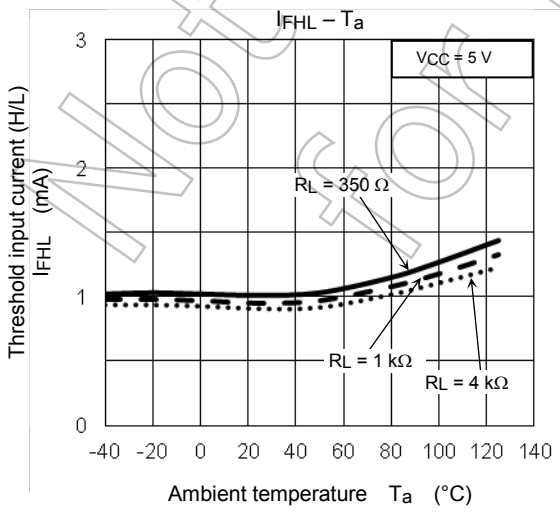
$V_{OL} - T_a$



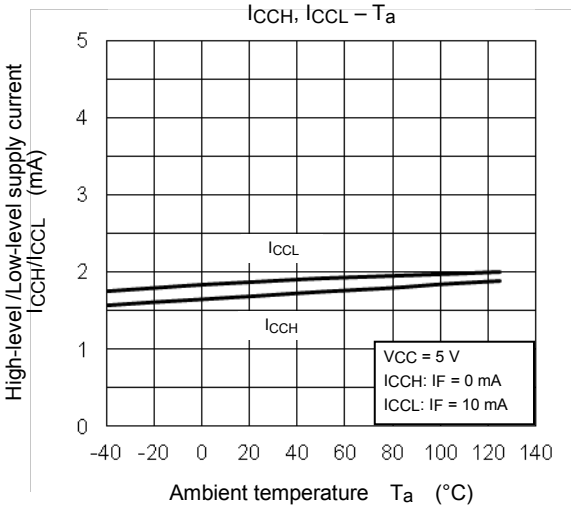
$V_O - I_F$



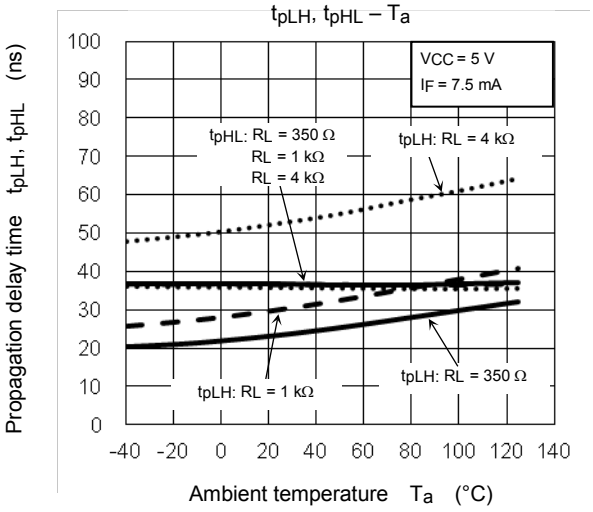
$I_{FHL} - T_a$

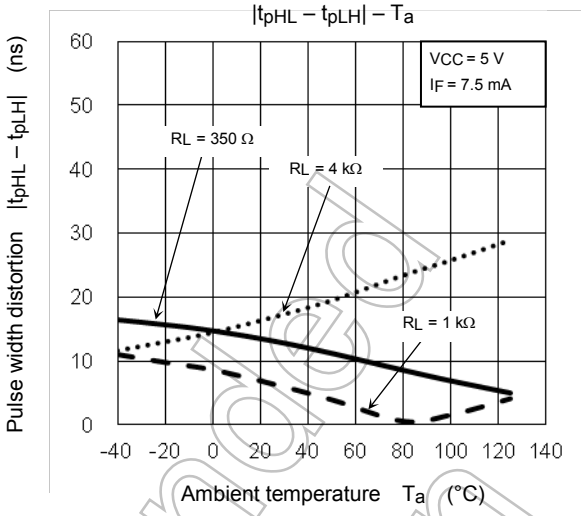


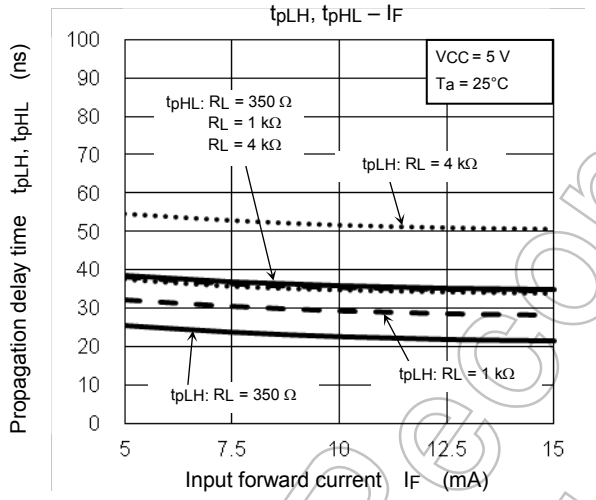
$I_{CCH}, I_{CCL} - T_a$

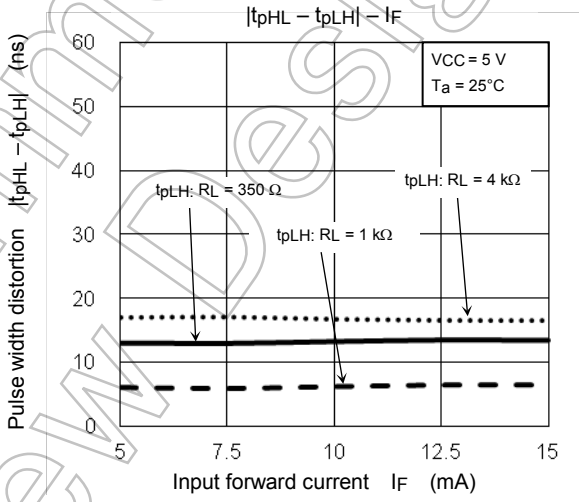


NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.









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Soldering and Storage

(1) Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

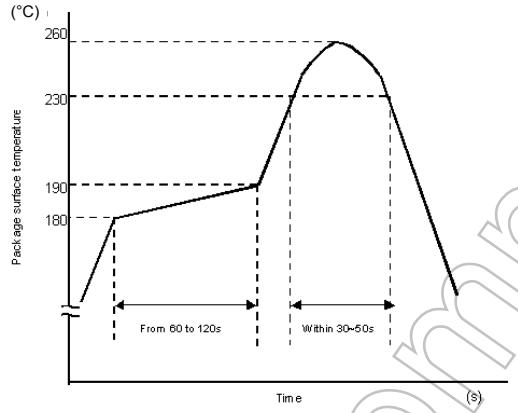
1) When Using Soldering Reflow

The soldering temperature profile is based on the package surface temperature.

(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.
The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

- An example of a temperature profile when lead(Pb)-free solder is used:



This profile is based on the device's maximum heat resistance guaranteed value.
Set the preheat temperature/heating temperature to the optimum temperature corresponding to the solder paste type used by the customer within the described profile.

2) When using soldering flow

- Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
- Mounting condition of 260 °C within 10 seconds is recommended.
- Flow soldering must be performed once

3) When using soldering Iron

- Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C.
- Heating by soldering iron must be only once per 1 lead

(2) Precautions for General Storage

1) Do not store devices in places where they will be exposed to moisture or direct sunlight.

2) During transportation or storage of devices, follow the cautions indicated on the carton box.

3) The storage area temperature should be kept within a temperature range of 5°C to 35°C, and the relative humidity should be maintained between 45% and 75%.

4) Do not store devices in the presence of harmful (especially corrosive) gases, or under dusty conditions.

5) Use storage areas where there is minimal temperature fluctuation. The solderability of the leads will be degraded as rapid temperature changes can cause condensation to form on the stored devices, resulting in lead oxidation or corrosion.

6) When repacking devices, use anti-static containers.

7) Do not apply any external force or load directly to devices when they are in storage.

8) If devices have been stored for more than two years, it is recommended that their solderability be tested before they are used even if the above precautions have been followed.

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