TOSHIBA
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Product Types

TOSHIBA Microcontroller TX00 Series
TMPM066, TMPM067, TMPM068

Additional cautions on use TSPI of datasheet

With regard to TOSHIBA microcontrollers listed above, we would like to inform customers the additional cautions on use TSPI of datasheet. If you have any questions or require any further information, please contact your local sales office.

1. Additional informations

A part of caution about communication control were not described.

Current description

15.3.3 TSPIxCR1 (TSPI Control Register 1)

Bit	Bit Symbol	Type	Function
31-15	–	R	Read as "0".
14	TRXE	R/W	Communication control (Note) 0 : Communication stops 1 : Communication is enabled. Full duplex mode/transmission mode If valid data exists in the transmit FIFO or shift register, transmission starts. If valid data does not exist in the transmit FIFO or shift register, transmission does not start. To start communications, write data to transmit FIFO or write transmit data when communications are enabled. If this bit is set as disable during transmission, the transmission will stop after the ongoing frame will complete and the setting will become disable. Receive mode : Once this bit is enabled, reception immediately starts. If this bit is set to disable during reception, reception will stop after the ongoing frame is complete and the setting is becomes disable.
13	TSPIMS	R/W	Communication mode selection 0 : SPI mode
			1 : Reserved.
7-0	FC[7:0]	R/W	Sets number of transfer frames 0 : Prohibited 1 : Single transfer 2 to 255 : Burst transfer

Note:<TRXE> is not cleared to "0" as long as CPU write "0" in single transfer. However, in the case of burst transfer, <TRXE> is automatically cleared to "0" after the specified numbers of burst transfers are complete. If burst transfer is executed again, check if TSPIxSR<TSPISUE> bit returns to "0" then write "1" to <TRXE>.

After description added

15.3.3 TSPIxCR1 (TSPI Control Register 1)

Bit	Bit Symbol	Type	Function
31-15	–	R	Read as "0".
14	TRXE	R/W	Communication contro (Note1),(Note2) 0 : Communication stops 1 : Communication is enabled. Full duplex mode/transmission mode If valid data exists in the transmit FIFO or shift register, transmission starts. If valid data does not exist in the transmit FIFO or shift register, transmission does not start. To start communications, write data to transmit FIFO or write transmit data when communications are enabled. If this bit is set as disable during transmission, the transmission will stop after the ongoing frame will complete and the setting will become disable. Receive mode : Once this bit is enabled, reception immediately starts. If this bit is set to disable during reception, reception will stop after the ongoing frame is complete and the setting is becomes disable.
13	TSPIMS	R/W	Communication mode selection 0 : SPI mode
			1 : Reserved.
7-0	FC[7:0]	R/W	Sets number of transfer frames 0 : Prohibited 1 : Single transfer 2 to 255 : Burst transfer

Note1: <TRXE> is not cleared to "0" as long as CPU write "0" in single transfer. However, in the case of burst transfer, <TRXE> is automatically cleared to "0" after the specified numbers of burst transfers are complete. If burst transfer is executed again, check if TSPIxSR<TSPISUE> bit returns to "0" then write "1" to <TRXE>.

Note2: In the slave operation, TSPI modify status flag TSPIxSR<TSPISUE> is not cleared to “0”, even if writes <TRXE> to "0" (disable communication) before actual communication (on master side) is not started after <TRXE> wrote to "1" (enable communication). When in spite of enabled communication on slave device, the communication on the master device is not started, please performs software reset by TSPIxCR0<SWRST> in a slave device, and re-set it up.