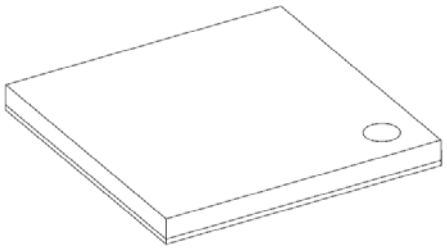
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90193SBG

Video signal processing IC for small LCD

1. Overview

TC90193SBG is a video processing IC for small LCD panel (QVGA to WVGA).
Analog (CVBS) input and digital (RGB / YUV) input are possible, and it performs video signal processing to the selected input signal, and outputs digital RGB signal and panel control signal.
In addition, it has OSD function using built-in SRAM font and line drawing function for car parking.



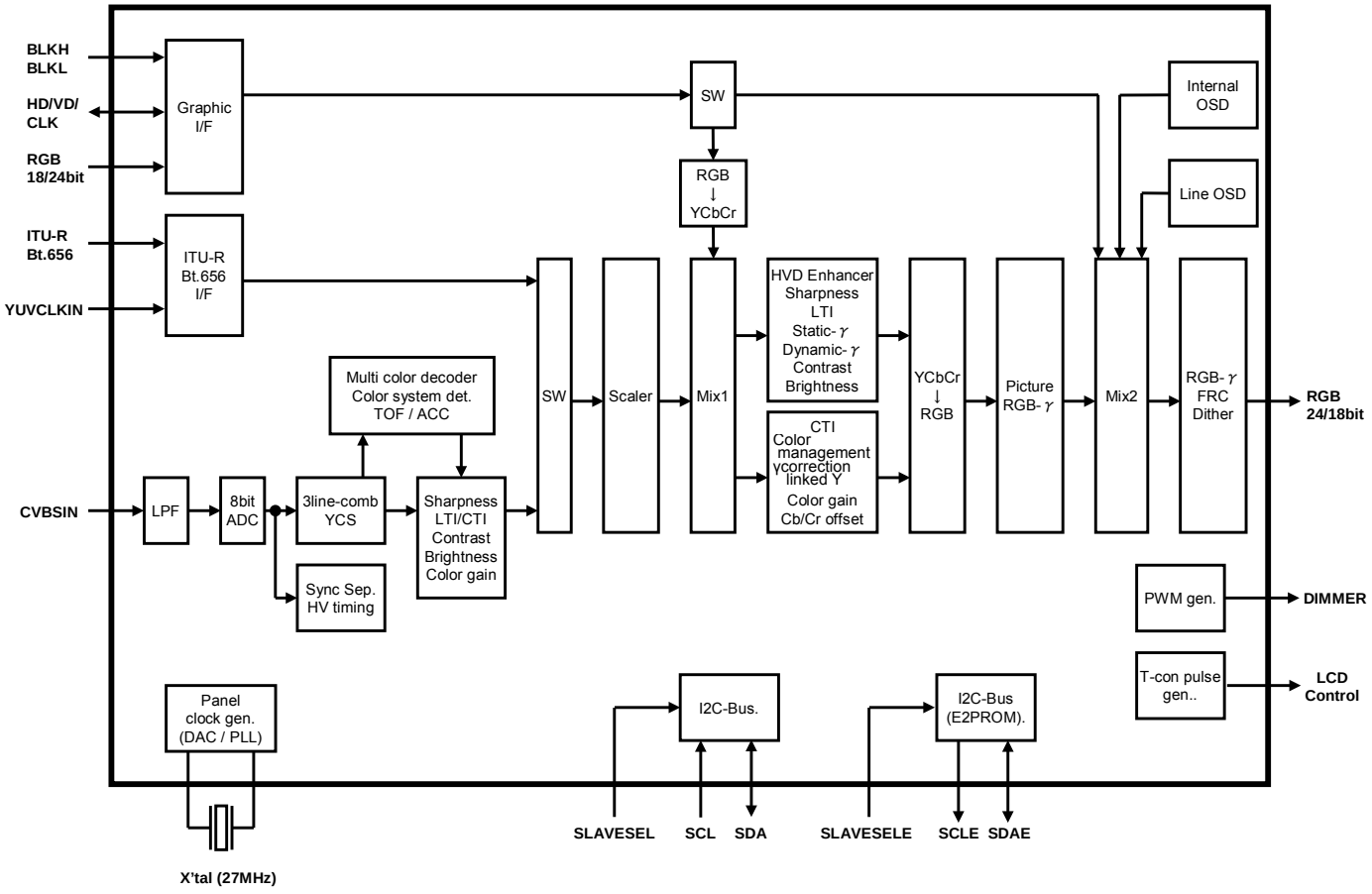
P-FBGA228-1515-0.80A5

Weight : 0.50g(Typ.)

1.1 Features

1. Video signal input
   Analog CVBS(NTSC/PAL)/ITU-R BT.656(digital YUV)
   Digital RGB signal (6bit × 3 or 8bit × 3)
2. 8bit ADC, Pre-filter(LPF) for input analog video signal
3. 3Line YC separation
4. Multi color system Decoder
5. Digital RGB signal output (24bit)
   QVGA(320x240)
   WQVGA(400x234, 400x240, 480x234, 480x240, 480x272)
   VGA(640x480)
   WVGA(800x480)
6. Timing control pulse output for LCD panel
7. Scaling function
   Horizontal aberration correction
   Horizontal compressed function
   Horizontal/Vertical over-scan
8. Picture Quality Improvement function
   <Y signal process>
   -HVD Enhancer
   -Sharpness, LTI, Noise reducer
   -Static Y-gamma correction
   -Dynamic Y-gamma correction
   -Contrast, Brightness
   <C signal process>
   -CTI, Noise reducer
   -C gain correction with Y-gamma characteristic
   -Color management
   -Color gain, Cb/Cr offset adjustment
   <RGB signal process>
   -Offset adjustment, Gain adjustment
   -RGB-gamma correction
   -Dither, FRC (Frame Rate Control)
9. PWM signal output
10. Font OSD built-in
11. Line drawing OSD
12. Superimposed D-RGB signal input (Internal sync-signal synchronous)
13. I^2C-BUS control
14. Package: P-FBGA228-1515-0.80A5
15. Power Supply: 3.3V, 2.5V, 1.5V
16. Operating temperature: -40°C to 85°C

2. Block Diagram



3. Pin Layout

Package TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	BLKL	BLKH	DINCLK	PTH	BOUT0	VDDIO	BOUT3	BOUT5	DVDD	DVDD	GOUT0	GOUT2	VDDIO	VDDIO	GOUT6	ROUT0	ROUT2	A
B	DIN1	DIN0	DINHD	DINVD	OSDCLK	BOUT1	BOUT2	BOUT4	BOUT6	BOUT7	GOUT1	GOUT3	GOUT4	GOUT5	GOUT7	ROUT1	ROUT3	B
C	DIN3	DIN2	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	ROUT4	ROUT5	C
D	DIN5	DIN4	DVSS	–	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	–	DVSS	ROUT6	VDDIO	D
E	VDDIO	DIN6	DVSS	DVSS	–	–	–	–	–	–	–	–	–	DVSS	DVSS	ROUT7	LOAD	E
F	DIN8	DIN7	DVSS	DVSS	–	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	–	–	DVSS	DVSS	DIMMER	ENABLE	F
G	DIN10	DIN9	DVSS	DVSS	–	DVSS	DVSS	–	–	–	–	DVSS	–	DVSS	DVSS	STH	HCOM	G
H	DVDD	DIN11	DVSS	DVSS	–	DVSS	–	–	–	–	–	DVSS	–	DVSS	DVSS	GOE	DVDD	H
J	DVDD	DIN12	DVSS	DVSS	–	DVSS	–	–	–	–	–	DVSS	–	DVSS	DVSS	STV2	DVDD	J
K	DIN13	DIN14	DVSS	DVSS	–	DVSS	–	–	–	–	–	DVSS	–	DVSS	DVSS	CPH	STV1	K
L	DIN15	DIN16	DVSS	DVSS	–	DVSS	–	–	–	–	–	DVSS	–	DVSS	DVSS	CPV	VLOAD	L
M	DIN17	DIN18	DVSS	DVSS	–	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	–	DVSS	DVSS	VCOM2	VCOM1	M
N	VDDIO	DIN19	DVSS	DVSS	–	–	–	–	–	–	–	–	–	AVSS	DVSS	UD	VDDIO	N
P	DIN20	DIN21	DVSS	–	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	XVSS	DAVSS	DAVSS	–	AVSS	AVSS	AVSS	P
R	DIN22	DIN23	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	XVSS	DAVSS	DAVSS	DAVSS	AVSS	BIAS	CVBSIN	R
T	DIN24	DIN25	SDA	SDAE	SCLE	SLVSEL	SGSEL	TEST3	TEST2	TEST1	XI	PLL1IN	DAVSS	PLL1FIL	DACOUT	AVSS	VRB	T
U	YUVCLKIN	PANELSELECT	SCL	VDDIO	SLVSELE	RESET	MUTEIN	DVDD	DVDD	TEST0	XO	XVDD	DAVSS	DAVDD	AVDD	VRT	AVSS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

4. Pin Description

Pin No.	Pin Name	Block	IO	Function	Standard withstand voltage[V]
A1	BLKL	Digital	I	OSD Blanking control input (For halftone)	3.3
B1	DIN1	Digital	I	R1<8bit> input / R1<6ibt> input	3.3
C1	DIN3	Digital	I	R3<8bit> input / R3<6bit> input	3.3
D1	DIN5	Digital	I	R5<8bit> input / R5<6bit> input	3.3
E1	VDDIO	Power	-	3.3V power supply for I/O block	-
F1	DIN8	Digital	I	G0<8bit> input / G2<6bit> input	3.3
G1	DIN10	Digital	I	G2<8bit> input / G4<6bit> input	3.3
H1	DVDD	Power	-	1.5V power supply for internal logic	-
J1	DVDD	Power	-	1.5V power supply for internal logic	-
K1	DIN13	Digital	I	G5<8bit> input / B1<6bit> input	3.3
L1	DIN15	Digital	I	G7<8bit> input / B3<6bit> input	3.3
M1	DIN17	Digital	I	B1<8bit> input / B5<6bit> input	3.3
N1	VDDIO	Power	-	3.3V power supply for I/O block	-
P1	DIN20	Digital	I	B4<8bit> input / ITU-R Bt.656[2] input	3.3
R1	DIN22	Digital	I	B6<8bit> input / ITU-R Bt.656[4] input	3.3
T1	DIN24	Digital	I	connect GND / ITU-R Bt.656[6] input	3.3
U1	YUVCLKIN	Digital	I	connect GND / ITU-R Bt.656[clock] input	3.3
A2	BLKH	Digital	I	OSD Blanking control input	3.3
B2	DIN0	Digital	I	R0<8bit> input / R0<6bit> input	3.3
C2	DIN2	Digital	I	R2<8bit> input / R2<6bit> input	3.3
D2	DIN4	Digital	I	R4<8bit> input / R4<6bit> input	3.3
E2	DIN6	Digital	I	R6<8bit> input / G0<6bit> input	3.3
F2	DIN7	Digital	I	R7<8bit> input / G1<6bit> input	3.3
G2	DIN9	Digital	I	G1<8bit> input / G3<6bit> input	3.3
H2	DIN11	Digital	I	G3<8bit> input / G5<6bit> input	3.3
J2	DIN12	Digital	I	G4<8bit> input / B0<6bit> input	3.3
K2	DIN14	Digital	I	G6<8bit> input / B2<6bit> input	3.3
L2	DIN16	Digital	I	B0<8bit> input / B4<6bit> input	3.3
M2	DIN18	Digital	I	B2<8bit> input / ITU-R Bt.656[0] input	3.3
N2	DIN19	Digital	I	B3<8bit> input / ITU-R Bt.656[1] input	3.3
P2	DIN21	Digital	I	B5<8bit> input / ITU-R Bt.656[3] input	3.3
R2	DIN23	Digital	I	B7<8bit> input / ITU-R Bt.656[5] input	3.3
T2	DIN25	Digital	I	connect GND / ITU-R Bt.656[7] input	3.3
U2	PANELSELECT	Digital	I	Setup polarity of GOE signal output	3.3
A3	DINCLK	Digital	I	RGB Clock signal input	3.3
B3	DINHD	Digital	I/O	RGB HD input(Default) / OSD HD output	3.3
C3	DVSS	Power	-	Digital GND	-
D3	DVSS	Power	-	Digital GND	-
E3	DVSS	Power	-	Digital GND	-
F3	DVSS	Power	-	Digital GND	-
G3	DVSS	Power	-	Digital GND	-
H3	DVSS	Power	-	Digital GND	-
J3	DVSS	Power	-	Digital GND	-
K3	DVSS	Power	-	Digital GND	-
L3	DVSS	Power	-	Digital GND	-
M3	DVSS	Power	-	Digital GND	-
N3	DVSS	Power	-	Digital GND	-
P3	DVSS	Power	-	Digital GND	-
R3	DVSS	Power	-	Digital GND	-
T3	SDA	Digital	I/O	I^2C-BUS SDA	5
U3	SCL	Digital	I	I^2C-BUS SCL	5

Pin No.	Pin Name	Block	IO	Function	Standard withstand voltage[V]
A4	PTH	Digital	I	Mask area control for picture improve process	3.3
B4	DINVD	Digital	I/O	RGB VD input(Default) / OSD VD output	3.3
C4	DVSS	Power	-	Digital GND	-
D4	-	-	-	Not connect (No ball)	-
E4	DVSS	Power	-	Digital GND	-
F4	DVSS	Power	-	Digital GND	-
G4	DVSS	Power	-	Digital GND	-
H4	DVSS	Power	-	Digital GND	-
J4	DVSS	Power	-	Digital GND	-
K4	DVSS	Power	-	Digital GND	-
L4	DVSS	Power	-	Digital GND	-
M4	DVSS	Power	-	Digital GND	-
N4	DVSS	Power	-	Digital GND	-
P4	-	-	-	Not connect (No ball)	-
R4	DVSS	Power	-	Digital GND	-
T4	SDAE	Digital	I/O	I^2C-BUS SDA for E2PROM control	5
U4	VDDIO	Power	-	3.3V power supply for I./O block	-
A5	BOUT0	Digital	O	Digital RGB output(B0)	3.3
B5	OSDCLK	Digital	O	OSD clock output	3.3
C5	DVSS	Power	-	Digital GND	-
D5	DVSS	Power	-	Digital GND	-
E5	-	-	-	Not connect (No ball)	-
F5	-	-	-	Not connect (No ball)	-
G5	-	-	-	Not connect (No ball)	-
H5	-	-	-	Not connect (No ball)	-
J5	-	-	-	Not connect (No ball)	-
K5	-	-	-	Not connect (No ball)	-
L5	-	-	-	Not connect (No ball)	-
M5	-	-	-	Not connect (No ball)	-
N5	-	-	-	Not connect (No ball)	-
P5	DVSS	Power	-	Digital GND	-
R5	DVSS	Power	-	Digital GND	-
T5	SCLE	Digital	O	I^2C-BUS SCL for E2PROM control	5
U5	SLVSELE	Digital	I	Slave address select for E2PROM	3.3
A6	VDDIO	Power	-	3.3V power supply for I/O block	-
B6	BOUT1	Digital	O	Digital RGB output(B1)	3.3
C6	DVSS	Power	-	Digital GND	-
D6	DVSS	Power	-	Digital GND	-
E6	-	-	-	Not connect (No ball)	-
F6	DVSS	Power	-	Digital GND	-
G6	DVSS	Power	-	Digital GND	-
H6	DVSS	Power	-	Digital GND	-
J6	DVSS	Power	-	Digital GND	-
K6	DVSS	Power	-	Digital GND	-
L6	DVSS	Power	-	Digital GND	-
M6	DVSS	Power	-	Digital GND	-
N6	-	-	-	Not connect (No ball)	-
P6	DVSS	Power	-	Digital GND	-
R6	DVSS	Power	-	Digital GND	-
T6	SLVSEL	Digital	I	I^2C-BUS Slave address select	3.3
U6	RESET	Digital	I	Reset	5

Pin No.	Pin Name	Block	IO	Function	Standard withstand voltage[V]
A7	BOUT3	Digital	O	Digital RGB output(B3)	3.3
B7	BOUT2	Digital	O	Digital RGB output(B2)	3.3
C7	DVSS	Power	-	Digital GND	-
D7	DVSS	Power	-	Digital GND	-
E7	-	-	-	Not connect (No ball)	-
F7	DVSS	Power	-	Digital GND	-
G7	DVSS	Power	-	Digital GND	-
H7	-	-	-	Not connect (No ball)	-
J7	-	-	-	Not connect (No ball)	-
K7	-	-	-	Not connect (No ball)	-
L7	-	-	-	Not connect (No ball)	-
M7	DVSS	Power	-	Digital GND	-
N7	-	-	-	Not connect (No ball)	-
P7	DVSS	Power	-	Digital GND	-
R7	DVSS	Power	-	Digital GND	-
T7	SGSEL	Digital	I	CVBS input/Digital input select (H:Digital/L:Foced CVBS)	3.3
U7	MUTEIN	Digital	I	External forced mute	3.3
A8	BOUT5	Digital	O	Digital RGB output(B5)	3.3
B8	BOUT4	Digital	O	Digital RGB output(B4)	3.3
C8	DVSS	Power	-	Digital GND	-
D8	DVSS	Power	-	Digital GND	-
E8	-	-	-	Not connect (No ball)	-
F8	DVSS	Power	-	Digital GND	-
G8	-	-	-	Not connect (No ball)	-
H8	-	-	-	Not connect (No ball)	-
J8	-	-	-	Not connect (No ball)	-
K8	-	-	-	Not connect (No ball)	-
L8	-	-	-	Not connect (No ball)	-
M8	DVSS	Power	-	Digital GND	-
N8	-	-	-	Not connect (No ball)	-
P8	DVSS	Power	-	Digital GND	-
R8	DVSS	Power	-	Digital GND	-
T8	TEST3	Digital	I	TEST	3.3
U8	DVDD	Power	-	1.5V power supply for internal logic	-
A9	DVDD	Power	-	1.5V power supply for internal logic	-
B9	BOUT6	Digital	O	Digital RGB output(B6)	3.3
C9	DVSS	Power	-	Digital GND	-
D9	DVSS	Power	-	Digital GND	-
E9	-	-	-	Not connect (No ball)	-
F9	DVSS	Power	-	Digital GND	-
G9	-	-	-	Not connect (No ball)	-
H9	-	-	-	Not connect (No ball)	-
J9	-	-	-	Not connect (No ball)	-
K9	-	-	-	Not connect (No ball)	-
L9	-	-	-	Not connect (No ball)	-
M9	DVSS	Power	-	Digital GND	-
N9	-	-	-	Not connect (No ball)	-
P9	DVSS	Power	-	Digital GND	-
R9	DVSS	Power	-	Digital GND	-
T9	TEST2	Digital	I	TEST	3.3
U9	DVDD	Power	-	1.5V power supply for internal logic	-

Pin No.	Pin Name	Block	IO	Function	Standard withstand voltage[V]
A10	DVDD	Power	-	1.5V power supply for internal logic	-
B10	BOUT7	Digital	O	Digital RGB output(B7)	3.3
C10	DVSS	Power	-	Digital GND	-
D10	DVSS	Power	-	Digital GND	-
E10	-	-	-	Not connect (No ball)	-
F10	DVSS	Power	-	Digital GND	-
G10	-	-	-	Not connect (No ball)	-
H10	-	-	-	Not connect (No ball)	-
J10	-	-	-	Not connect (No ball)	-
K10	-	-	-	Not connect (No ball)	-
L10	-	-	-	Not connect (No ball)	-
M10	DVSS	Power	-	Digital GND	-
N10	-	-	-	Not connect (No ball)	-
P10	DVSS	Power	-	Digital GND	-
R10	DVSS	Power	-	Digital GND	-
T10	TEST1	Digital	I	TEST	3.3
U10	TEST0	Digital	I	TEST	3.3
A11	GOUT0	Digital	O	Digital RGB output(G0)	3.3
B11	GOUT1	Digital	O	Digital RGB output(G1)	3.3
C11	DVSS	Power	-	Digital GND	-
D11	DVSS	Power	-	Digital GND	-
E11	-	-	-	Not connect (No ball)	-
F11	DVSS	Power	-	Digital GND	-
G11	-	-	-	Not connect (No ball)	-
H11	-	-	-	Not connect (No ball)	-
J11	-	-	-	Not connect (No ball)	-
K11	-	-	-	Not connect (No ball)	-
L11	-	-	-	Not connect (No ball)	-
M11	DVSS	Power	-	Digital GND	-
N11	-	-	-	Not connect (No ball)	-
P11	XVSS	Power	-	X'tal GND	-
R11	XVSS	Power	-	X'tal GND	-
T11	XI	XTAL	I	Input pin of X'tal circuit	-
U11	XO	XTAL	O	Output pin of X'tal circuit	-
A12	GOUT2	Digital	O	Digital RGB output(G2)	3.3
B12	GOUT3	Digital	O	Digital RGB output(G3)	3.3
C12	DVSS	Power	-	Digital GND	-
D12	DVSS	Power	-	Digital GND	-
E12	-	-	-	Not connect (No ball)	-
F12	-	-	-	Not connect (No ball)	-
G12	DVSS	Power	-	Digital GND	-
H12	DVSS	Power	-	Digital GND	-
J12	DVSS	Power	-	Digital GND	-
K12	DVSS	Power	-	Digital GND	-
L12	DVSS	Power	-	Digital GND	-
M12	DVSS	Power	-	Digital GND	-
N12	-	-	-	Not connect (No ball)	-
P12	DAVSS	Analog Power	-	DAC/PLL1 GND	-
R12	DAVSS	Analog Power	-	DAC/PLL1 GND	-
T12	PLL1IN	Analog IN	I	PLL1 input	-
U12	XVDD	Power	-	2.5V power supply for X'tal	-

Pin No.	Pin Name	Block	IO	Function	Standard withstand voltage[V]
A13	VDDIO	Power	-	3.3V power supply for I/O block	-
B13	GOUT4	Digital	O	Digital RGB output(G4)	3.3
C13	DVSS	Power	-	Digital GND	-
D13	DVSS	Power	-	Digital GND	-
E13	-	-	-	Not connect (No ball)	-
F13	-	-	-	Not connect (No ball)	-
G13	-	-	-	Not connect (No ball)	-
H13	-	-	-	Not connect (No ball)	-
J13	-	-	-	Not connect (No ball)	-
K13	-	-	-	Not connect (No ball)	-
L13	-	-	-	Not connect (No ball)	-
M13	-	-	-	Not connect (No ball)	-
N13	-	-	-	Not connect (No ball)	-
P13	DAVSS	Analog Power	-	DAC/PLL1 GND	-
R13	DAVSS	Analog Power	-	DAC/PLL1 GND	-
T13	DAVSS	Analog Power	-	DAC/PLL1 GND	-
U13	DAVSS	Analog Power	-	DAC/PLL1 GND	-
A14	VDDIO	Power	-	3.3V power supply for I/O block	-
B14	GOUT5	Digital	O	Digital RGB output(G5)	3.3
C14	DVSS	Power	-	Digital GND	-
D14	-	-	-	Not connect (No ball)	-
E14	DVSS	Power	-	Digital GND	-
F14	DVSS	Power	-	Digital GND	-
G14	DVSS	Power	-	Digital GND	-
H14	DVSS	Power	-	Digital GND	-
J14	DVSS	Power	-	Digital GND	-
K14	DVSS	Power	-	Digital GND	-
L14	DVSS	Power	-	Digital GND	-
M14	DVSS	Power	-	Digital GND	-
N14	AVSS	Analog Power	-	ADC GND	-
P14	-	-	-	Not connect (No ball)	-
R14	DAVSS	Analog Power	-	DAC/PLL1 GND	-
T14	PLL1FIL	Analog Bias	O	Filter pin for PLL1	-
U14	DAVDD	Analog Power	-	2.5V power supply for DAC/PLL1	-
A15	GOUT6	Digital	O	Digital RGB output(G6)	3.3
B15	GOUT7	Digital	O	Digital RGB output(G7)	3.3
C15	DVSS	Power	-	Digital GND	-
D15	DVSS	Power	-	Digital GND	-
E15	DVSS	Power	-	Digital GND	-
F15	DVSS	Power	-	Digital GND	-
G15	DVSS	Power	-	Digital GND	-
H15	DVSS	Power	-	Digital GND	-
J15	DVSS	Power	-	Digital GND	-
K15	DVSS	Power	-	Digital GND	-
L15	DVSS	Power	-	Digital GND	-
M15	DVSS	Power	-	Digital GND	-
N15	DVSS	Power	-	Digital GND	-
P15	AVSS	Analog Power	-	ADC GND	-
R15	AVSS	Analog Power	-	ADC GND	-
T15	DACOUT	Analog OUT	O	DAC output	-
U15	AVDD	Analog Power	-	2.5V power supply for ADC	-

Pin No.	Pin Name	Block	IO	Function	Standard withstand voltage[V]
A16	ROUT0	Digital	O	Digital RGB output (R0)	3.3
B16	ROUT1	Digital	O	Digital RGB output (R1)	3.3
C16	ROUT4	Digital	O	Digital RGB output (R4)	3.3
D16	ROUT6	Digital	O	Digital RGB output (R6)	3.3
E16	ROUT7	Digital	O	Digital RGB output (R7)	3.3
F16	DIMMER	Digital	O	PWM signal output	3.3
G16	STH	Digital	O	Control signal for LCD (Start signal of H)	3.3
H16	GOE	Digital	O	Reset signal for LCD panel GOE is controlled by “Panel select” U2 terminal	3.3
J16	STV2	Digital	O	Control signal for LCD (Start signal for V Gate 2)	3.3
K16	CPH	Digital	O	Control signal for LCD (Source clock signal of H)	3.3
L16	CPV	Digital	O	Control signal for LCD (Gate clock signal of V)	3.3
M16	VCOM2	Digital	O	Control signal for LCD (Common voltage output 2)	3.3
N16	UD	Digital	O	Control signal for LCD (Scanning direction control)	3.3
P16	AVSS	Analog Power	-	ADC GND	-
R16	BIAS	Analog Bias	-	Bias pin of ADC	-
T16	AVSS	Analog Power	-	ADC GND	-
U16	VRT	Analog Bias	-	Reference top voltage pin of ADC	-
A17	ROUT2	Digital	O	Digital RGB output(R2)	3.3
B17	ROUT3	Digital	O	Digital RGB output(R3)	3.3
C17	ROUT5	Digital	O	Digital RGB output(R5)	3.3
D17	VDDIO	Power	-	3.3V power supply for I/O block	-
E17	LOAD	Digital	O	Control signal for LCD (Latch signal of H direction)	3.3
F17	ENABLE	Digital	O	Control signal for LCD (Data Enable)	3.3
G17	HCOM	Digital	O	Control signal for LCD (Invert signal for each dot.)	3.3
H17	DVDD	Power	-	1.5V power supply for internal logic	-
J17	DVDD	Power	-	1.5V power supply for internal logic	-
K17	STV1	Digital	O	Control signal for LCD (Start signal for V Gate 1)	3.3
L17	VLOAD	Digital	O	Control signal for LCD (Latch signal of V direction)	3.3
M17	VCOM1	Digital	O	Control signal for LCD (Common voltage output 1)	3.3
N17	VDDIO	Power	-	3.3V power supply for I/O block	-
P17	AVSS	Analog Power	-	ADC GND	-
R17	CVBSIN	Analog IN	I	Analog CVBS signal input	-
T17	VRB	Analog Bias	-	Reference bottom voltage pin of ADC	-
U17	AVSS	Analog Power	-	ADC GND	-

5. Function

5.1 Video signal input

TC90193SBG will be able to input the analog CVBS signal of one route and the digital YUV signal of one route (ITU-R Bt.656) and one route of digital RGB signal, a total of three.
The digital RGB is 8bit.
When the analog CVBS signal input and digital YUV signal input are selected, by inputting the digital RGB signal synchronized with the synchronous signal output (HD, VD, clock) from the TC90193SBG, Digital RGB signals can be overlaid on analog CVBS signal and digital YUV signal.
(Notes: When selecting digital YUV signal, digital RGB signal is inputted only 6bit.)
When digital RGB input is selected, it is available to display the digital RGB by inputting the HD, VD and CLK signals synchronized with the digital RGB.
The effective number of pixels can be selected from the table below by internal register settings.

<Effective pixels of digital RGB signal>

Resolution type	Horizontal effective pixels	Vertical effective pixels
QVGA	320	234
WQVGA	400	234
WQVGA	400	240
WQVGA	480	234
WQVGA	480	240
WQVGA	480	272
VGA	640	480
WVGA	800	480

Also, if you don't use a digital YUV signal input, digital RGB signal will be able input 8bit.

< Relation between the main picture of TC90193SBG and digital RGB (OSD) input>

Main input signal	Digital RGB(OSD)
CVBS	O (8bit/6bit)
D-YUV(ITU-R Bt.656)	O (6bit)
D-RGB	X (disabled)

5.1.1 Analog CVBS signal input

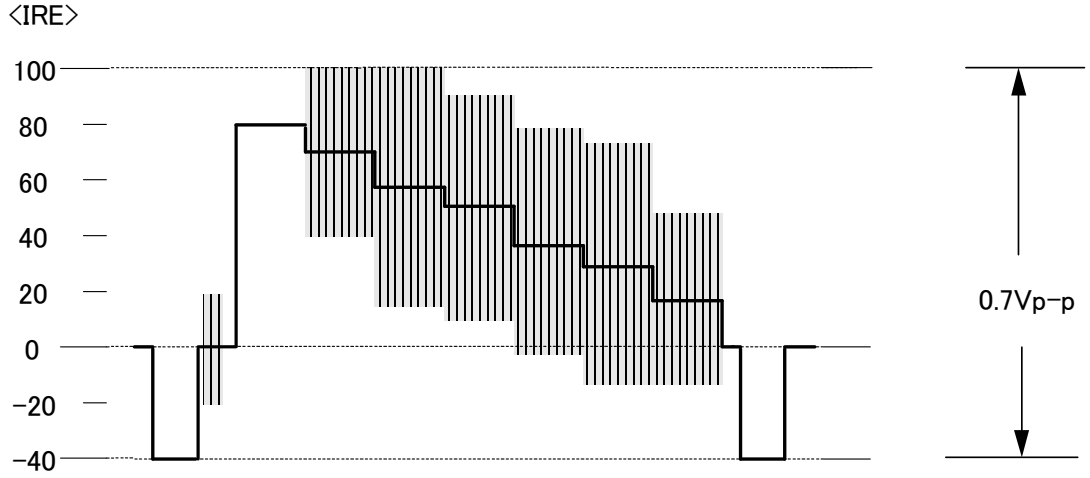
5.1.1.1. About input signal

TC90193SBG has 8bit ADC for analog CVBS signal input.
Dynamic range of ADC is designed in AVDD*0.4. The normal input dynamic range is 1.0Vp-p (AVDD = 2.5V).
Recommended standard input amplitude: 0.7 Vp-p (0.7 times) at 140 IRE input.

The clamp process for CVBS signal is pedestal clamp of sync-feed-back type.
And, TC90193SBG has digital clamp process after ADC process.

5.1.1.2. Reference input level for analog CVBS signal

Reference input level for analog CVBS signal when100% white



5.1.1.3. LPF function

LPF for anti-aliasing is built-in before ADC.
It is the selectable of "LPF through" or "via the LPF".

5.1.2 Terminal of digital signal input

Terminals of digital signal input are assigned as follows.

●Input and Output signal

OSD CLK out :Clock output for superimposing RGB(OSD), the signal synchronized inside the IC
OSD HD out :HD output for superimposing RGB(OSD), the signal synchronized inside the IC
OSD VD out :VD output for superimposing RGB(OSD), the signal synchronized inside the IC

RGB CLK in : Clock signal input for digital RGB(OSD) input
RGB HD in : HD signal input for digital RGB(OSD) input
RGB VD in : VD signal input for digital RGB(OSD) input

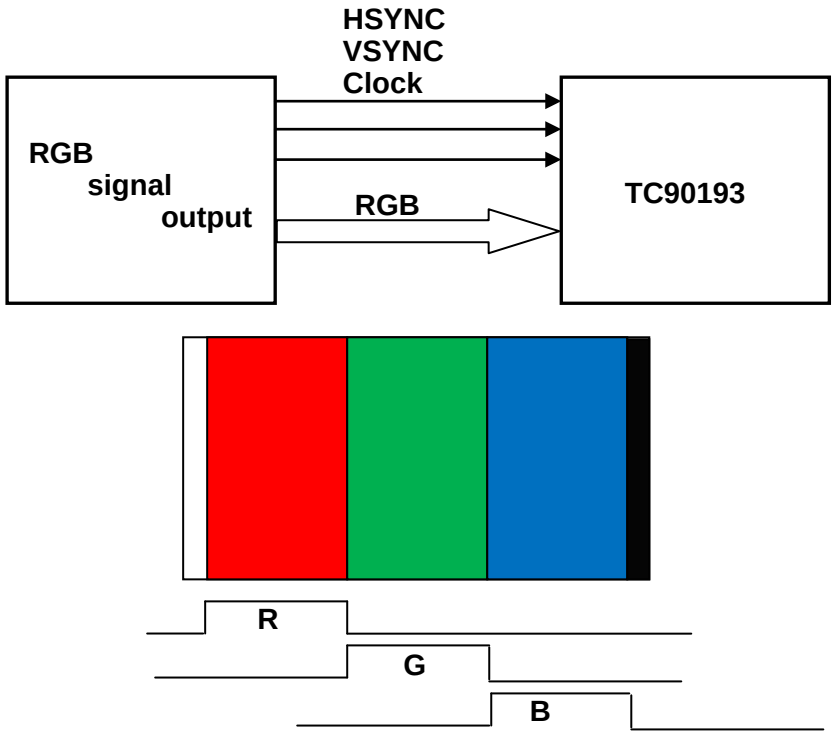
656CLK in : The clock for ITU-R Bt.656 input.

Terminal No.	Terminal name	I/O	Terminal description	Mode 1 D-RGB input only.	Mode 2 Main picture is D-YUV(656) input and D-RGB input is OSD.	Mode 3 Main picture Is CVBS input and D-RGB input is OSD.
B5	OSDCLK	O	OSD Clock output	Low out	OSD CLK out	OSD CLK out
A3	DINCLK	I	Digital RGB clock input	RGB CLK in	-	-
B4	DINVD	I/O	RGB VD in/OSD VD out	RGB VD in	OSD VD out	OSD VD out
B3	DINHD	I/O	RGB HD in/OSD HD out	RGB HD in	OSD HD out	OSD HD out
B2	DIN0	I	R0 in / R2 in	R0 in	R2 in	R0 in
B1	DIN1	I	R1 in / R3 in	R1 in	R3 in	R1 in
C2	DIN2	I	R2 in / R4 in	R2 in	R4 in	R2 in
C1	DIN3	I	R3 in / R5 in	R3 in	R5 in	R3 in
D2	DIN4	I	R4 in / R6 in	R4 in	R6 in	R4 in
D1	DIN5	I	R5 in / R6 in	R5 in	R7 in	R5 in
E2	DIN6	I	R6 in / G2 in	R6 in	G2 in	R6 in
F2	DIN7	I	R7 in / G3 in	R7 in	G3 in	R7 in
F1	DIN8	I	G0 in / G4 in	G0 in	G4 in	G0 in
G2	DIN9	I	G1 in / G5 in	G1 in	G5 in	G1 in
G1	DIN10	I	G2 in / G6 in	G2 in	G6 in	G2 in
H2	DIN11	I	G3 in / G7 in	G3 in	G7 in	G3 in
J2	DIN12	I	G4 in / B2 in	G4 in	B2 in	G4 in
K1	DIN13	I	G5 in / B3 in	G5 in	B3 in	G5 in
K2	DIN14	I	G6 in / B4 in	G6 in	B4 in	G6 in
L1	DIN15	I	G7 in / B5 in	G7 in	B5 in	G7 in
L2	DIN16	I	B0 in / B6 in	B0 in	B6 in	B0 in
M1	DIN17	I	B1 in / B7 in	B1 in	B7 in	B1 in
M2	DIN18	I	B2 in / 656[0] in	B2 in	656[0] in	B2 in
N2	DIN19	I	B3 in / 656[1] in	B3 in	656[1] in	B3 in
P1	DIN20	I	B4 in / 656[2] in	B4 in	656[2] in	B4 in
P2	DIN21	I	B5 in / 656[3] in	B5 in	656[3] in	B5 in
R1	DIN22	I	B6 in / 656[4] in	B6 in	656[4] in	B6 in
R2	DIN23	I	B7 in / 656[5] in	B7 in	656[5] in	B7 in
T1	DIN24	I	VSS fixed / 656[6] in	-	656[6] in	-
T2	DIN25	I	VSS fixed / 656[7] in	-	656[7] in	-
U1	YUVCLKIN	I	VSS fixed / 656CLK in	-	656CLK in	-

5.1.3 Digital RGB signal input

5.1.3.1. Normal mode (Mode1)

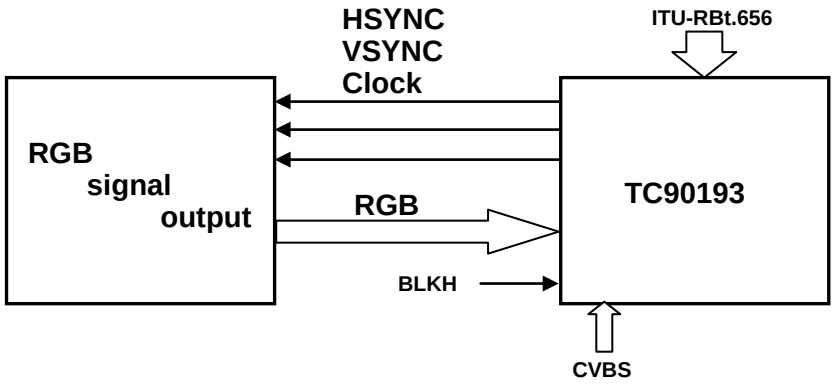
In normal mode (mode 1) only displays digital RGB input.
In normal mode, input of HD, VD and CLK is necessary.
(Seg:0x00,Sub:0x00, D7D6:1∗).
And, horizontal and vertical back porch (The width to the start of the valid from the front edge of sync signal) must be a fixed value.
The Width of HD pulse is necessary more than 300ns. If less than 300ns, input signal is judged as no-signal.



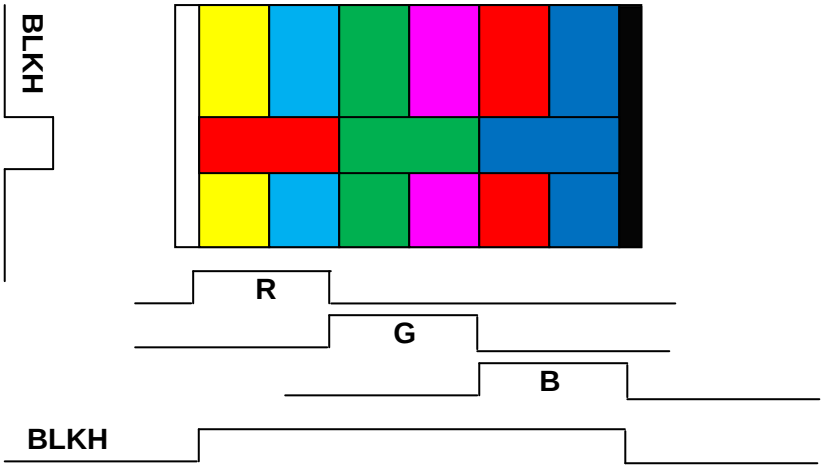
RGB inputs and picture image

5.1.3.2. Synchronized mode (Mode 2, Mode 3)

In this mode, digital RGB signal is overlaid on analog CVBS signal or ITU-R Bt.656 signal.
(Digital RGB is used for OSD overlay.)
Set the SGSEL pin to High and set the Seg:0x00,Sub:0x00,D7D6:00 to becomes CVBS input mode.
Also, it becomes 656 input mode in D7D6: 01 setting.
In this synchronous mode, the digital RGB signal synchronized with the signal(HD, VD, clock) output from TC90193 is input again to TC90193.The setting is Seg:0x00,Sub:0x50,D7:1.



CVBS(or 656) is a Color Bar, when RGB(OSD) is overlaid



CVBS or 656 input and RGB (OSD) image

TC90193 has 2 overlay mode of synchronized RGB signal input.

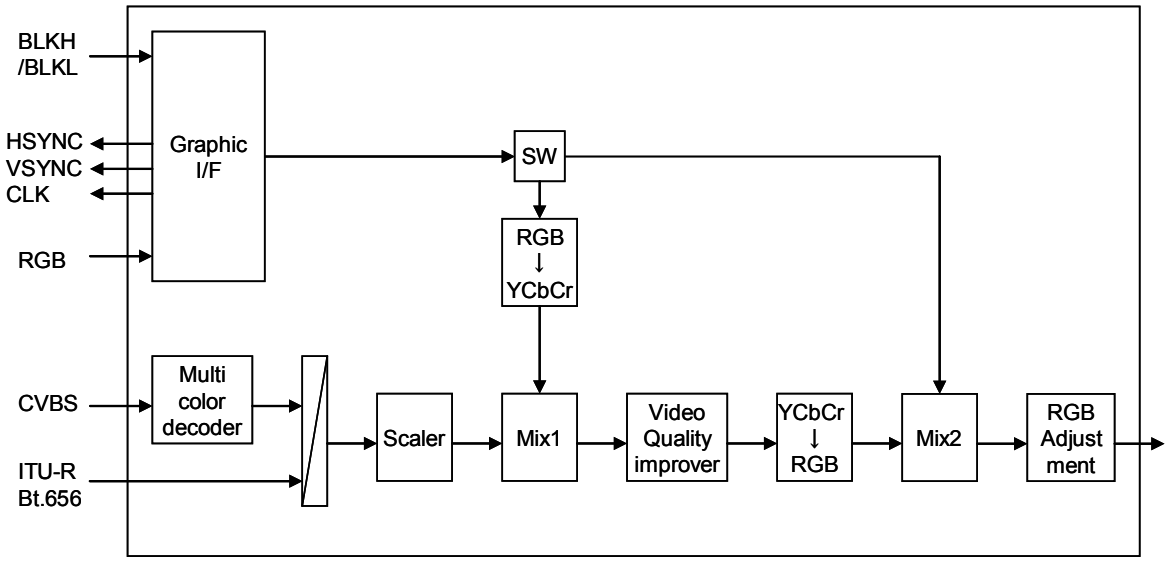
1. Mix1 (Seg:0x00,Sub:0x56,D3:0)

   Digital RGB signal is converted to YCbCr, and overlaid on CVBS picture or ITU-R Bt.656 picture.
   For digital RGB signal, function of video quality improver is available.
   However, half tone process on overlay process is not available.

2. Mix2 (Seg:0x00,Sub:0x56,D3:1)

   It overlays the digital RGB signal on the CVBS or ITU-R Bt.656 after the scaler processing in the state of RGB. Also, Halftone process on overlay is available.
   Halftone processing can be set with the BLKH and BLKL pins and registers.

   The Mix position is shown in the following block diagram.



5.2 Video signal output

It outputs digital RGB of the resolution, described in following list.
When digital RGB input, TC90193SBG outputs digital RGB signal of the resolution same as input signal.

Resolution type	Horizontal effective pixels	Vertical effective pixels
QVGA	320	234
WQVGA	400	234
WQVGA	400	240
WQVGA	480	234
WQVGA	480	240
WQVGA	480	272
VGA	640	480
WVGA	800	480

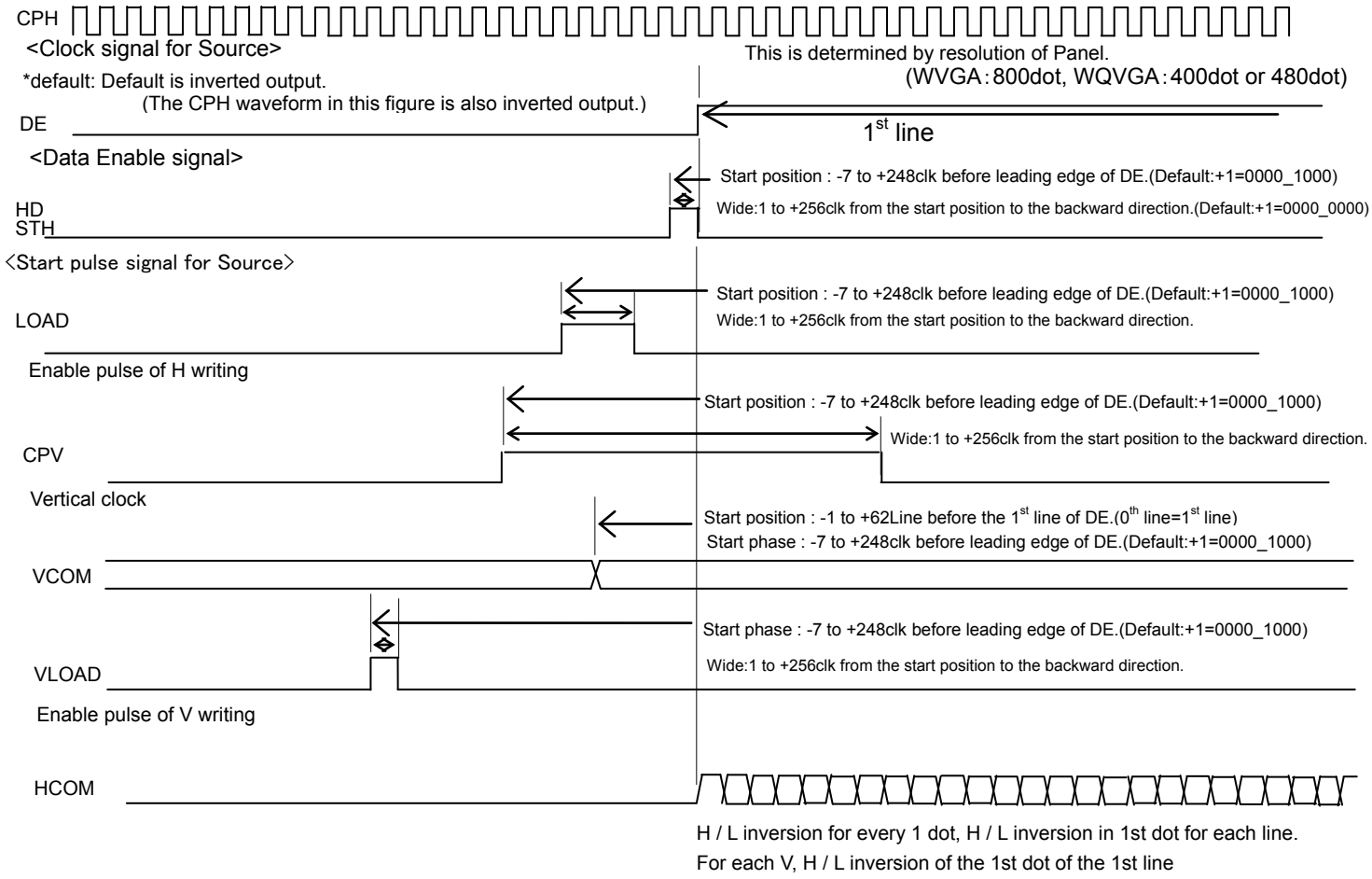
5.3 Control signals for LCD panel

The Control signals for LCD use the leading edge of output active period as a reference point.
There are output possible position setting limitations, when setting output in the forward direction from the front edge of the data enable period.

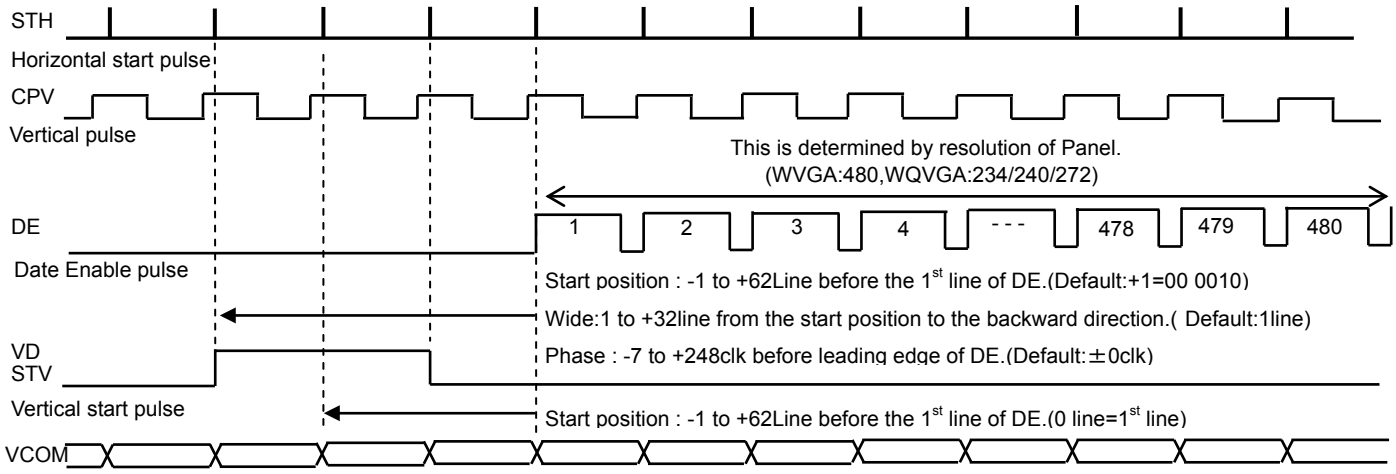
< Horizontal >
The horizontal start phase for panel control signals is limited to width of horizontal back porch for D-RGB input setting.
Output horizontal back porch = input back porch -1 [clk]

< Vertical >
The vertical start phase for panel control signals is limited to width of vertical back-porch for D-RGB input setting.
Output vertical back porch = input back porch +1 [line]

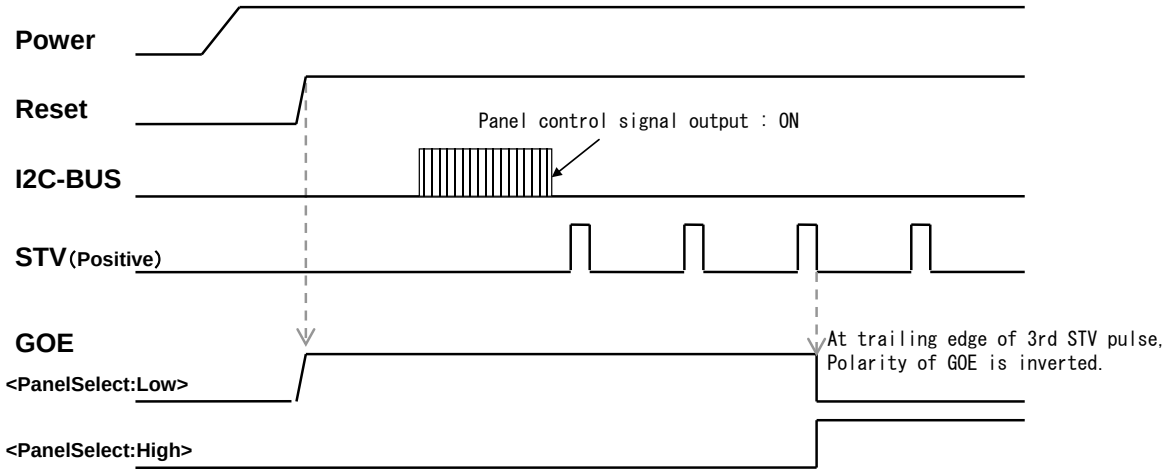
<Horizontal>


CPH
<Clock signal for Source>
*default: Default is inverted output.
(The CPH waveform in this figure is also inverted output.)
This is determined by resolution of Panel.
(WVGA:800dot, WQVGA:400dot or 480dot)
DE
1st line
<Data Enable signal>
Start position : -7 to +248clk before leading edge of DE.(Default:+1=0000_1000)
HD
STH
Wide:1 to +256clk from the start position to the backward direction.(Default:+1=0000_0000)
〈Start pulse signal for Source〉
Start position : -7 to +248clk before leading edge of DE.(Default:+1=0000_1000)
LOAD
Wide:1 to +256clk from the start position to the backward direction.
Enable pulse of H writing
Start position : -7 to +248clk before leading edge of DE.(Default:+1=0000_1000)
Wide:1 to +256clk from the start position to the backward direction.
CPV
Vertical clock
Start position : -1 to +62Line before the 1st line of DE.(0th line=1st line)
Start phase : -7 to +248clk before leading edge of DE.(Default:+1=0000_1000)
VCOM
Start phase : -7 to +248clk before leading edge of DE.(Default:+1=0000_1000)
Wide:1 to +256clk from the start position to the backward direction.
VLOAD
Enable pulse of V writing
HCOM
H / L inversion for every 1 dot, H / L inversion in 1st dot for each line.
For each V, H / L inversion of the 1st dot of the 1st line

<Vertical>



<Power on and start sequence>



6. Absolute Maximum Rating

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the absolute maximum rating may result in destruction, degradation or other damage to the IC and other components.

When designing applications for this IC, be sure that none of the absolute maximum rating values will ever be exceeded.

Item	Corresponding terminal	Symbol	Rating	Unit
Power voltage (1.5V system)	A9,A10,H1,H17,J1,J17, U8,U9	VDD1	-0.3 to VSS+2.0	V
Power voltage (2.5V system)	U12,U14,U15	VDD2	-0.3 to VSS+3.5	V
Power voltage (3.3V system)	A6,A13,A14,D17,E1,N1, N17,U4	VDD3	-0.3 to VSS+3.9	V
Input voltage (3.3V system)	A1,A2,A3,A4,B1,B2,B3, B4,C1,C2,D1,D2,E2,F1, F2,G1,G2,H2,J2,K1,K2, L1,L2,M1,M2,N2,P1,P2, R1,R2,T1,T2,T6,T7,U1, U2,U5,U7	VIN3	-0.3 to VDD3+0.3	V
Input voltage (3.3V system, 5V withstand voltage)	T3,T4,T5,U3,U6	VIN4 (note 1)	-0.3 to VSS+5.5	V
Potential difference between power pins (between 1.5V system power pins)	A9,A10,H1,H17,J1,J17, U8,U9	ΔVDG1 (note 2)	0.3	V
Potential difference between power pins (between 2.5V system power pins)	U12,U14,U15	ΔVDG2 (note 3)	0.3	V
Potential difference between power pins (between 3.3V system power pins)	A6,A13,A14,D17,E1,N1, N17,U4	ΔVDG3 (note 4)	0.3	V
Power dissipation		PD (note 5)	2777	mW
Storage temperature		Tstg	-55 to 125	°C

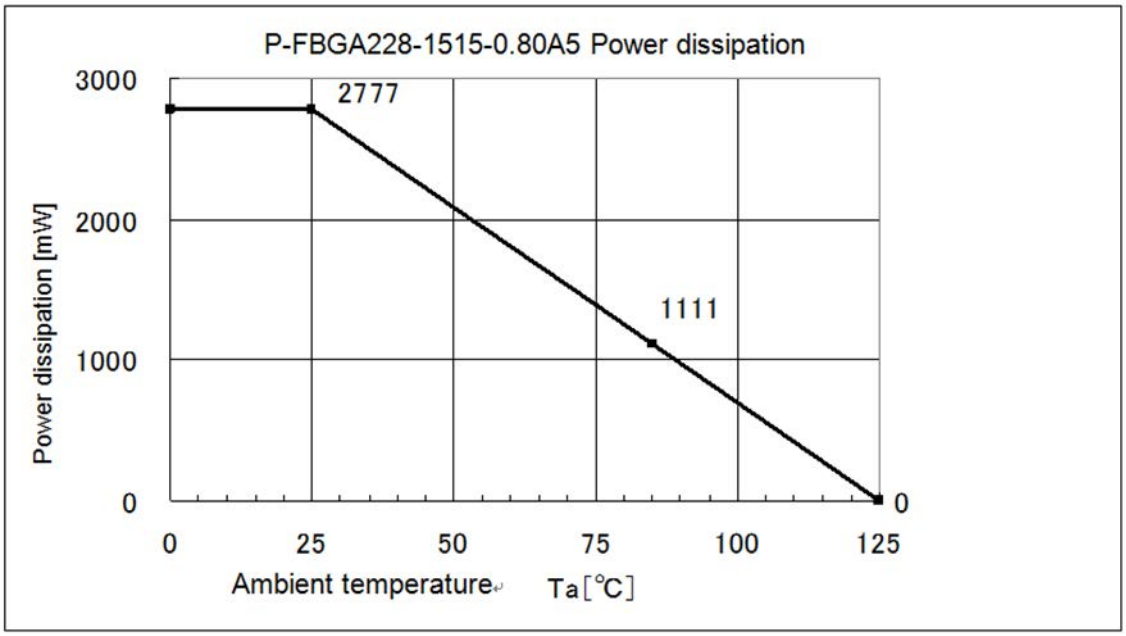
Note1: The withstand voltage for pins(SCL, SDA, SCLE, SDAE, RESET) is 5V.

Note2: With the 1.5 VDD terminal group connected (shorted) at the same potential, The maximum potential difference between with the other VDD pin groups should not exceed the rated value. And, keep the maximum potential difference between all V_{SS} pins within 0.01 V.

Note3: With the 2.5 VDD terminal group connected (shorted) at the same potential, The maximum potential difference between with the other VDD pin groups should not exceed the rated value. And, keep the maximum potential difference between all VSS pins within 0.01 V.

Note4: With the 3.3 VDD terminal group connected (shorted) at the same potential, The maximum potential difference between with the other VDD pin groups should not exceed the rated value. And, keep the maximum potential difference between all VSS pins within 0.01V.

Note5: If using a temperature higher than Ta = 25°C, reduce by 27.77mW per 1°C increase. (When Ta = 85°C, maximum power dissipation is 1111mW)


P-FBGA228-1515-0.80A5 Power dissipation
3000
2000
1000
0
Power dissipation [mW]
2777
1111
0
0
25
50
75
100
125
Ambient temperature
Ta [°C]

7. Operation Condition

Cannot guarantee operation of TC90193SBG, when the recommendation power supply voltage range (1.4V-1.6V, 2.3-2.7V, 3.0V-3.6V) is exceeded.
Please use within the specified operating conditions.
Once it returns from the outside of voltage range, it differs from a previous condition.
Therefore, it need to be powered off, and then be powered on again.

Item	Corresponding terminal	Symbol	Min	Typ.	Max	Unit
Power voltage of digital block	A9, A10, H1, H17, J1, J17, U8, U9	VDD-D	1.4	1.5	1.6	V
Power voltage of XO block (note1)	U12	VDD-XO	2.3	2.5	2.7	V
Power voltage of PLL/DAC block (note1)	U14	VDD-DA	2.3	2.5	2.7	V
Power voltage of analog (ADC) block (note1)	U15	VDD-AD	2.3	2.5	2.7	V
Power voltage of I/O block	A6, A13, A14, D17, E1, N1, N17, U4	VDD-IO	3.0	3.3	3.6	V
Operating temperature	-	Topr	-40	-	85	°C

Note1: Please make sure that the power-voltage of three systems (VDD-XO, VDD-DA, VDD-AD) are supplied same electrical potential.

8. Electrical characteristic

8.1 DC characteristic

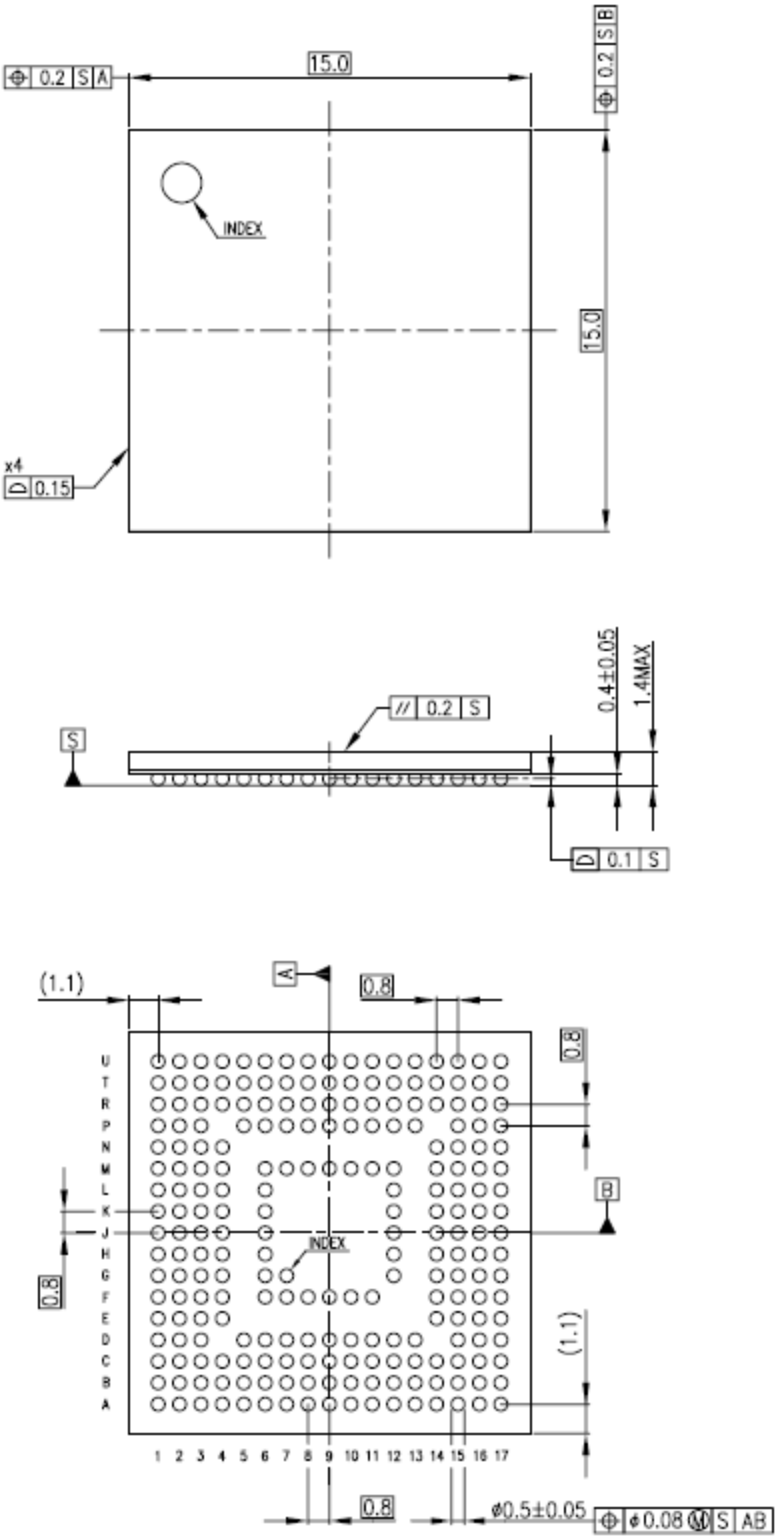
(Ta=25°C, VDD1=1.50±0.1V, VDD2=2.50±0.2V, VDD3=3.30±0.3V)

Item	Terminal No.	Symbol	Min	Typ.	Max	Unit	Note
Power supply current	A9,A10,H1,H17,J1, J17,U8,U9	IDD1	-	-	150	mA	1.5V system
	U12,U14,U15	IDD2	-	-	75	mA	2.5V system
	A6,A13,A14,D17,E1, N1,N17,U4	IDD3	-	-	100	mA	3.3V system Note.1
Input voltage	A1,A2,A3,A4,B1,B2, B3,B4,C1,C2,D1,D2, E2,F1,F2,G1,G2,H2, J2,K1,K2,L1,L2,M1, M2,N2,P1,P2,R1,R2, T1,T2,T6,T7,U1,U2, U5,U7	VIH	VDD3x0.8	-	VDD3	V	I/O input terminal of 3.3V system
	T3,T4,T5,U3,U6						I/O input terminal of 5V system
	A1,A2,A3,A4,B1,B2, B3,B4,C1,C2,D1,D2, E2,F1,F2,G1,G2,H2, J2,K1,K2,L1,L2,M1, M2,N2,P1,P2,R1,R2, T1,T2,T6,T7,U1,U2, U5,U7	VIL	VSS	-	VDD3x0.2	V	I/O input terminal of 3.3V system
	T3,T4,T5,U3,U6						I/O input terminal of 5V system
Input current	A1,A2,A3,A4,B1,B2, B3,B4,C1,C2,D1,D2, E2,F1,F2,G1,G2,H2, J2,K1,K2,L1,L2,M1, M2,N2,P1,P2,R1,R2, T1,T2,T6,T7,U1,U2, U5,U7	IIH	-10	-	10	μA	I/O input terminal of 3.3V system
	T3,T4,T5,U3,U6						I/O input terminal of 5V system
	A1,A2,A3,A4,B1,B2, B3,B4,C1,C2,D1,D2, E2,F1,F2,G1,G2,H2, J2,K1,K2,L1,L2,M1, M2,N2,P1,P2,R1,R2, T1,T2,T6,T7,U1,U2, U5,U7	IIL	-10	-	10	μA	I/O input terminal of 3.3V system
	T3,T4,T5,U3,U6						I/O input terminal of 5V system

Note.1 : The power supply current of 3.3V systems depends on the load capacity of the LCD panel connected with this IC.
When the load capacity of the LCD panel is large value, the power supply current of 3.3V systems may exceed the above described maximum value.

Item	Terminal No.	Symbol	Min	Typ.	Max	Unit	Note
Output voltage	A5,A7,A8,A11,A12, A15,A16,A17,B5, B6,B7,B8,B9,B10, B11,B12,B13,B14, B15,B16,B17,C16, C17,D16,E16,E17, F16,F17,G16,G17, H16,J16,K17,L16, L17,M16,M17,N16	V_{OH}	VDD3-0.6	-	VDD3	V	I/O output terminal of 3.3V system when load current 4mA
	K16		VDD3-0.6	-	VDD3	V	I/O output terminal of 3.3V system when load current 8mA
	A5,A7,A8,A11,A12, A15,A16,A17,B5, B6,B7,B8,B9,B10, B11,B12,B13,B14, B15,B16,B17,C16, C17,D16,E16,E17, F16,F17,G16,G17, H16,J16,K17,L16, L17,M16,M17,N16	V_{OL}	VSS	-	0.4	V	I/O output terminal of 3.3V system when load current 4mA
	T3,T4,T5,U3		VSS	-	0.4	V	I/O output terminal of 5V system
	K16		VSS	-	0.4	V	I/O output terminal of 3.3V system when load current 8mA
Level potential difference between input and output terminal	T3,T4 T5,U3	ΔV_{IOL}	+0.3	-	+0.6	V	Voltage level difference between T3(SDA) and T4(SDAE) or U3(SCL) and T5(SCLE) ,when accessing E2PROM through TC90193SBG. (at the low-level input and output.)

9. Package



Unit: mm

10. Revision History

Revision	Date	Description
1.00	2016/12/01	First edition

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